A fuzzy-logic-based approach to accurate modeling of a double gate MOSFET for nanoelectronic circuit design

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Abstract: The double gate (DG) silicon MOSFET with an extremely short-channel length has the appropriate features to constitute the devices for nanoscale circuit design. To develop a physical model for extremely scaled DG MOSFETs, the drain current in the channel must be accurately determined under the application of drain and gate voltages. However, modeling the transport mechanism for the nanoscale structures requires the use of overkill methods and models in terms of their complexity and computation time (self-consistent, quantum computations, …). Therefore, new methods and techniques are required to overcome these constraints. In this paper, a new approach based on the fuzzy logic computation is proposed to investigate nanoscale DG MOSFETs. The proposed approach has been implemented in a device simulator to show the impact of the proposed approach on the nanoelectronic circuit design. The approach is general and thus is suitable for any type of nanoscale structure investigation problems in the nanotechnology industry.

Key words: nanoscale circuit; DG MOSFET; fuzzy modelling; computational cost; circuit design

1. Introduction

As transistor feature size moves into the nanoscale region, to realise better device performance and a higher package density, the characteristics of a conventional MOSFET degrade due to the hot-carrier and short channel effects (SCEs). Recently, the importance of multi-gate MOSFETs, particularly double gate (DG) MOSFETs, is rising in nanoscale CMOS circuit design. This is mainly due to the superior control of short channel effects (SCEs) because of the reduced influence of the drain voltage on the channel charge. The advantages advocated for DG MOSFET, shown in Fig. 1, include: an ideal subthreshold slope; light doping of the channel reducing the mobility degradation due to the elimination of impurity scattering; good control of short channel effects; ideal subthreshold swing due to the elimination of substrate doping; etc[1−3]. Although the operation of DG MOSFET is similar to the conventional MOSFET, the physics of this type of MOSFET are more complicated. Moreover, physical phenomena, such as the quantum mechanical and short channel effects, have to be considered. Therefore, simulation tools which can be explored to design nanoscale CMOS circuits require new theories and modeling techniques that capture the physics of quantum transport accurately to guide the design for nanoelectronic circuits.

The aggressive scaling scenarios set by the ITRS (International Technology Roadmap for Semiconductors)[4] make the accurate simulation of nanoscale transistors a challenging objective of modeling activity. Previous works which studied the DG MOSFETs include numerical and analytical modeling[1−3, 5−10]. The accurate modeling of the nanoscale DG MOSFET requires the solution of Schrödinger and Poisson equations based on the non-equilibrium Green's function (NEGF) formalism, assuming quantum effects are to be fully accounted for[10]. But from the nanoscale CMOS circuit design point of view even a 2-D solution of numerical NEGF is an overkill approach in terms of both complexity and computational cost[10]. Moreover, the nanoscale DG MOSFET introduces challenges to the analytical compact modeling associated with the enhanced coupling between the electrodes (source, drain, and gate), quantum confinement, ballistic transport, gate tunnelling current, etc[5−7, 9]. However, in these compact models, the quantum confinements for a very thin silicon channel (less than 5 nm) have not been taken into account. Therefore, models are obtained by a simplification of the full physical model (quantum effects, short-channel-effects, etc.). Accurate analytical models are required to be utilized in nanoscale circuit simulators and circuit design tools. In this context, in order to achieve the required accuracy and model simplicity, we present the applicability of the fuzzy logic (FL) computation approach to develop an analytical drain current model using the well known SPICE level 3 model[11, 12], which has been widely used to simulate the conventional bulk MOSFETs, for the nanoscale CMOS circuit design. Finally, the FL-based model of the DG MOSFET was used as a subcircuit in the SIMULINK software for the modeling and simulation of the nanoscale circuits.

2. Modeling methodology

The basic structure of the DG MOSFET investigated in this study is shown in Fig. 1. As the MOSFET feature size moves into a nanoscale regime, canonical carrier transport theories are no longer capable of describing the carrier transport accurately. The canonical theories are basically derived from the Boltzmann transport equation (BTE), with more or fewer approximations being made[13]. These models focus on
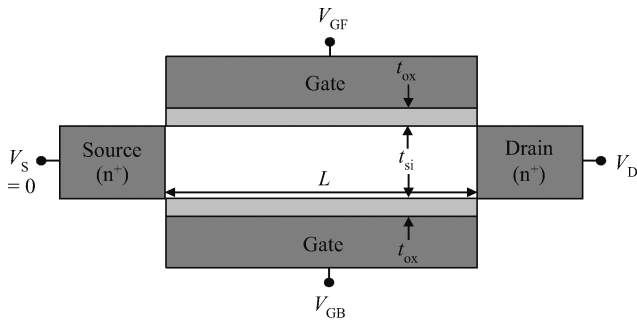
Fig. 1. Schematic sketch of a symmetrical DG MOSFET ($V_{GF} = V_{GB}$) structure investigated in this study with channel doping $N_A = 10^{16}$ cm^{-3}.

scattering-dominant transport, which typically occurs in long channel devices. However, transistors operate in ballistic or quasi-ballistic transport regimes. Simulations using conventional models may either under predict or over predict the electrical device behavior[10, 13, 14].

To simulate nanoscale transistors, the non-equilibrium Green's function formalism (NEGF) provides one of the best frameworks available[10]. Under ballistic conditions, the Green's Function method is mathematically equivalent to solving, numerically, the Schrödinger equation with open boundary conditions[10]. Based on the efficiency proven by NEGF for the modeling of nanoscale DG MOSFETs and the difficulty imposed at the moment by the constraints of the nanotechnology to form an experimental database, we have used the NEGF formalism to form the database which will be used to optimize the SPICE Level 3 model using a FL-based computation approach that has several advantages over conventional computing methods.

2.1. Fuzzy-logic computation

Among control techniques, the one that is especially easy to use is the one based on verbal rules that control the behavior of the system, which is called fuzzy control[15]. It is based on the theory of fuzzy sets and fuzzy logic[15]. References [15–17] offer extensive introductions to the fundamentals of FL and its wide range of applications. The input–output behavior of a fuzzy system is programmable using a linguistic information in the form of IF (preconditions) THEN (postconditions) rules, describing an approximate or qualitative knowledge of an observed process. FL is a superset of conventional Boolean logic that has been extended to include the concept of partial truth-truth-values between 'completely true' and 'completely false'. Due to its simple mechanism and high performance for behavior modeling, FL can be applied to study the nanoscale devices.

The first step of our approach consists of the compact SPICE Level 3 model for conventional bulk MOSFETs. This model is similar to the power-lane model[11] that introduces smoothing functions for the various transition regions. This allows the use of the following single equation to model the drain current for all operation regions.

$$I_{DSF} = \frac{\beta}{1 + \theta(V_{GS} - V_T)} \left[(V_{GS} - V_T) V_{DS} - \frac{\alpha}{2} V_{DS}^2 \right]$$
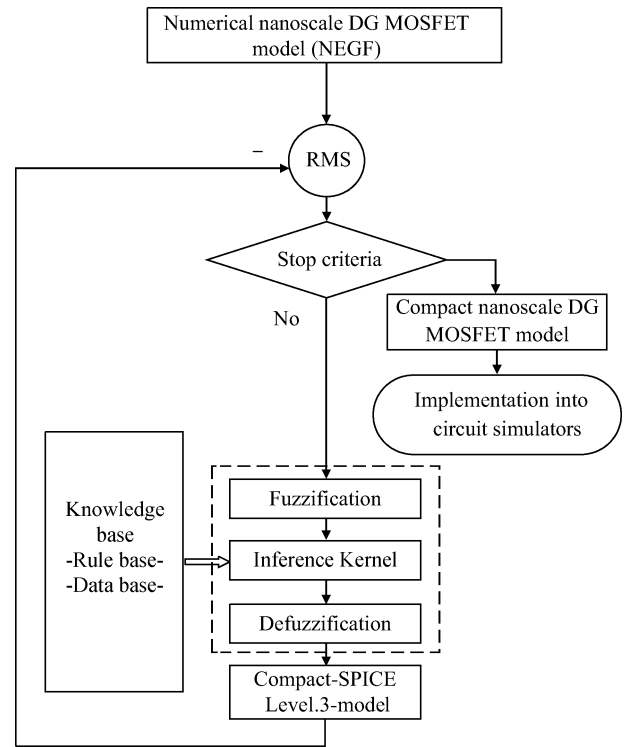$$\times [1 + \lambda (V_{DS} - V_{DSsat})], \tag{1}$$

Fig. 2. Flowchart of our Fuzzy-based computation approach.

where V_{GS} and V_{DS} represent the applied gate and drain voltages, respectively. V_{DSsat} is the saturation drain voltage given as

$$V_{DSsat} = \frac{V_{GS} - V_T}{\alpha}. \tag{2}$$

The model parameters are: V_T (threshold voltage), β (gain factor), α (saturation factor), θ (mobility reduction factor), and λ (channel length modulation factor).

To extend the above equation to subthreshold and saturation regions, the gate and drain bias are replaced with two modified expressions, V_{GSX} and V_{DSX}:

$$V_{GSX} = F(V_{GS}, V_T, \delta_1), \tag{3}$$

where $F(V_{GS}, V_T, \delta_1)$ is smoothing function[11] given by

$$F_0(x, y, \delta) = \frac{1}{2} \left(x - y + \delta - \sqrt{(x - y + \delta)^2 + 4\delta x} \right). \tag{4}$$

The parameter δ is an empirical smoothing parameter used to describe the rate at which V_{GSX} goes to V_{GS} or zero.

The expression for V_{DSX} is similar:

$$V_{DSX} = V_{DSsat} - F(V_{DS}, V_T, \delta_2). \tag{5}$$

Parameter V_{DSsat} in Eq. (1) is also replaced by V_{DSX} to remove the channel length modulation term in the triode region.

With these changes the drain current expression becomes

$$I_{DSF} = \frac{\beta}{1 + \theta V_{GSX}} \left(V_{GSX} V_{DSX} - \frac{\alpha}{2} V_{DSX}^2 \right)$$
$$\times [1 + \lambda (V_{DS} - V_{DSX})]. \tag{6}$$

This is a very simple expression that is useful for our purposes in order to develop a compact model to study the

Table 1. Fuzzy associate memory table (FAM) for the fuzzy V_T controller.

		Er_P (Principal error)				
		NL	NM	Z	PM	PL
Er_S secondary error	N	NL	NM	NS	PS	PM
	Z	NM	NM	Z	PM	PM
	P	NM	NS	PS	PM	PL

nanoscale MOSFETs using an FL-based computation. The flowchart of our proposed approach is detailed in Fig. 2.

To define the fuzzy associative memory, we need some knowledge about how each of these parameters affects the behavior of the $I{-}V$ curves:

(1) V_T shifts the whole $I_{DS}{-}V_{GS}$ curve.

(2) θ describes the curvature of $I_{DS}{-}V_{DS}$ as V_{GS} increases.

(3) β provides a scale factor.

(4) α establishes the relation between V_{GS} and V_{DSsat}.

(5) λ controls the slope of the $I_{DS}{-}V_{DS}$ characteristics in saturation.

Based on the effect of each parameter on the $I{-}V$ characteristics, we can define the following rules in order to develop our knowledge base (Fig. 2) for each design parameter:

(1) If the calculated curve $I_{DS}{-}V_{GS}$ is to the right of the numerical data, then decrease V_T, and vice versa.

(2) If the calculated curve $I_{DS}{-}V_{GS}$ is more curved than the numerical data, then decrease θ, and vice versa.

(3) If the calculated curve $I_{DS}{-}V_{GS}$ is over the numerical data, then decrease β and vice versa.

(4) If the $I_{DS}{-}V_{DS}$ calculated curve saturates too soon, decrease α, and vice versa.

(5) If the slope of the calculated $I_{DS}{-}V_{DS}$ curve is too small, then increase λ, and vice versa.

In order to implement the above rules, we have used the triangular fuzzy sets, while defuzzification is done through the method of centre of area (COA). The input and output parameters are normalized using the numerical curves as a reference. The linguistic variables chosen for this FL-based controller are the principal and secondary errors (Er_P and Er_S) for each parameter of the compact SPICE Level 3 model (Eq. (6)). These errors can be calculated for each parameter from:

$$\text{Er\_P} = \frac{I_{DS\text{-}N}(V_{GS} \approx V_T)}{\text{Max}(I_{DS\text{-}N})} - \frac{I_{DS\text{-}F}(V_{GS} \approx V_T)}{\text{Max}(I_{DS\text{-}F})}, \quad (7)$$

$$\text{Er\_S} = \frac{I_{DS\text{-}N}(V_{GS} = V_M)}{\text{Max}(I_{DS\text{-}N})} - \frac{I_{DS\text{-}F}(V_{GS} = V_M)}{\text{Max}(I_{DS\text{-}F})}, \quad (8)$$

where $I_{DS\text{-}N}$ and $I_{DS\text{-}F}$ represent the 2D numerical drain current simulation and FL-based drain current model, respectively. V_M is the medium voltage given by $V_M = \frac{V_T + V_{DD}}{2}$ while V_{DD} represents the supply voltage.

Both errors are the input linguistic variable and the drain current is the finale output linguistic variable. In this work, the principal error of each parameter represents the drain current deviation affected, only, by the main parameter, and the secondary one is the drain current deviation affected by a combination of several parameters (mutual effect). Each of the input and output fuzzy variables is assigned seven linguistic fuzzy
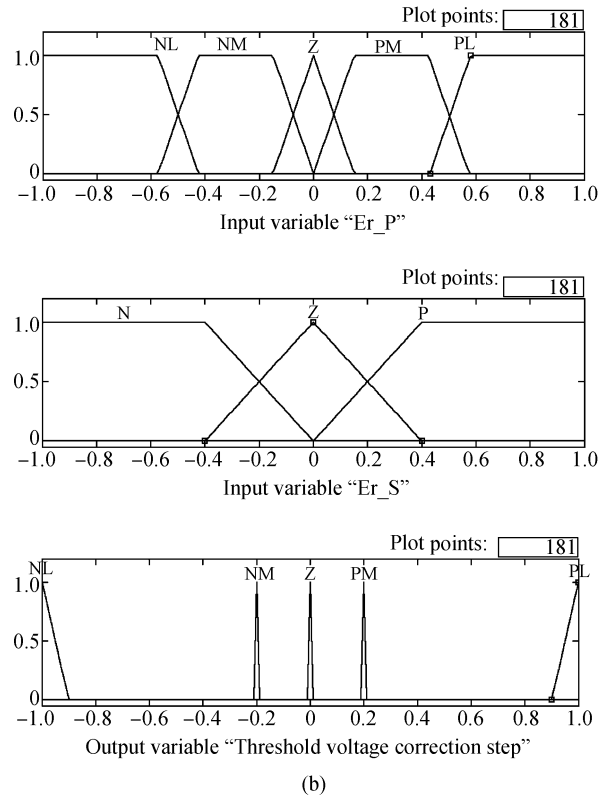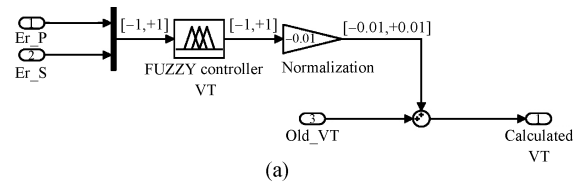

(a)

(b)

Fig. 3. (a) MATLAB- SIMILINK fuzzy V_T controller diagram. (b) Membership functions of the linguistic variables for the fuzzy V_T controller.

subsets varying from negative large (NL) to positive big (PL). Each subset is associated with a triangular membership function to form a set of seven membership functions for each fuzzy variable. The fuzzy controller diagram and the membership functions for each linguistic variable, in the case of the fuzzy V_T controller, are given in Figs. 3(a) and 3(b). The linguistic terms chosen for this controller are seven. They are negative large (NL), negative medium (NM), negative small (NS), zero (Z), positive small (PS), positive medium (PM) and positive large (PL). After assigning the input and output ranges to define fuzzy sets, mapping each of the possible five input fuzzy values of principal error (Er_P), three input fuzzy values of secondary error (Er_S) to the seven output fuzzy values is done through a rule base. Therefore, the fuzzy associative memory (FAM), for the fuzzy V_T controller, comes into the picture. The rules are framed keeping in mind the nature of the system performance and using common sense. Table 1 shows the fuzzy associate memory table of the fuzzy V_T controller.

It is noted that the development of the fuzzy controller for each parameter is carried out by following the same steps, which have been used to develop the fuzzy V_T controller.

Table 2. Comparison between the various approaches of modeling the DG MOSFET.

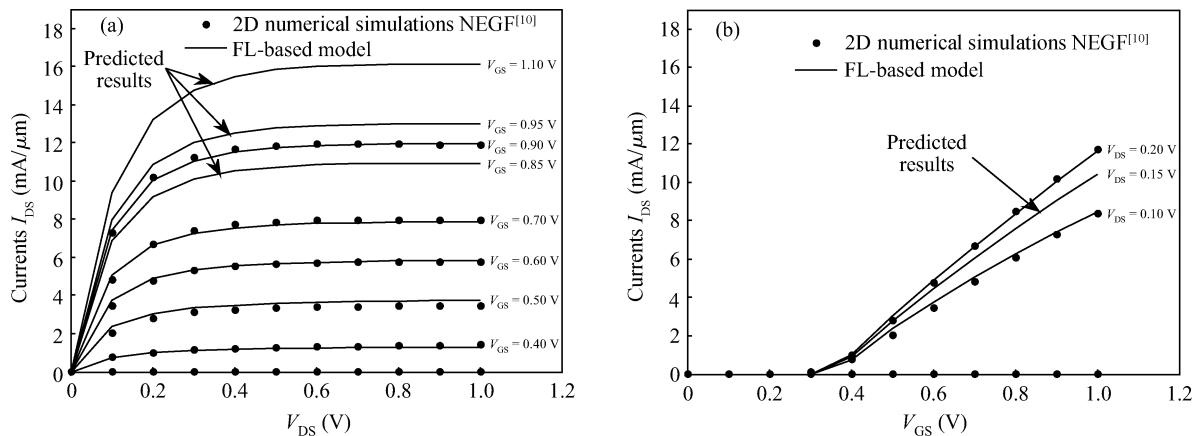| Model performance	Taur[5]	Smit[18]	Moldovan[19]	Kolberg[20]	Reyboz[21]	Fossum[6]	Djeffal[13]	FL-based model
Model simplicity	+	−	+	+/−	+	−	+	+
Explicit form	+/−	+	+	+	+	−	−	+
Short-channel-effect included	+	+	+	+	+	+	+	+
Dynamical behavior included	+	+	+	+	+	+	−	+
Quantum effects included	−	+	+	−	−	+	+	+
Validation range L (nm)	≥ 70	≥ 30	≥ 70	≥ 70	≥ 30	≥ 50	≥ 10	≥ 10
Validation range t_{si} (nm)	≥ 5	≥ 5	≥ 5	≥ 5	≥ 5	≥ 5	≥ 2	≥ 2
Computational time	+/−	−	+/−	+/−	+	−	+	+
Implementation into circuit simulators	+	−	+	+/−	+	−	+/−	+

Fig. 4. Current–voltage characteristics (I–V) calculated from the FL-based compact model (solid lines), compared with numerical results (symbols) for $L = 20$ nm, $t_{\text{si}} = 5$ nm and $t_{\text{ox}} = 1.5$ nm. (a) I_{DS}–V_{DS}. (b) I_{DS}–V_{GS}.

3. Results and discussion

Once all the parameters have been estimated, the method will then iterate from an initial point (a set of parameters) until a stopping condition is found (Fig. 2). For each iteration, new values for the parameters will be calculated by the fuzzy controller. The global RMS (root mean square) error between the numerical and calculated curves, considering all points on the curve, will be updated. In our case, we have used a stopping condition of a global RMS error of less than 5%. Figure 4 shows good agreement between the numerical and predicted results for the nanoscale DG MOSFETs. Our simulations were carried out for a wide range of nanoscale channel lengths, where we found that the RMS errors are within 5%. This last observation shows the applicability of the FL-based approach to study the nanoscale DG MOSFETs.

In order to validate the performance property of the proposed approach, numerical and analytical sets were compared to the FL-based drain current model. Table 2 gives a comparison of the performance properties for the simulated nano-DG MOSFET with various approaches where the FL-based model performance should be compared to the order of magnitude increase in computation time and the characteristics of more rigorous drain current models, such as those based on the analytical and numerical computations. The obtained results can be explained by the fact that the FL-based model is characterized as a computational model based on the parallel distributed processing of data. Hence, the FL-based model provides a practical insight into the nanoscale device modeling without the uncertain accuracy or meticulous tuning effort that face more rigorous nanoscale DG MOSFET models. The FL-based modeling is a step towards a new generation of simulation tools that will allow device and material engineers to explore new classes of electronic devices. It is noted that our FL-based model is valid for a channel length more than 10 nm due to the transport and mobility models considered is this study (the NEGF formal-
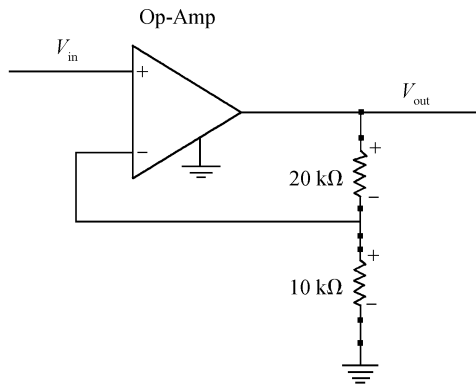
(a)
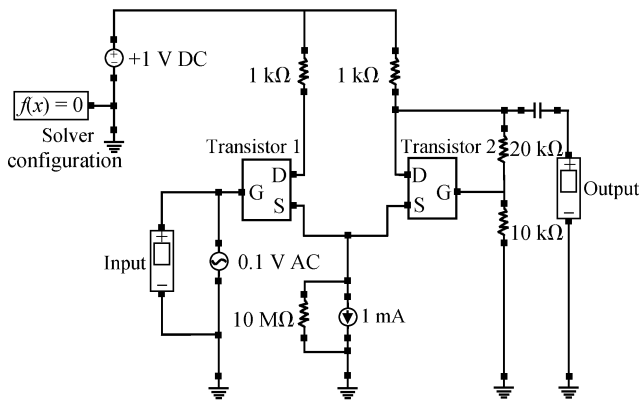
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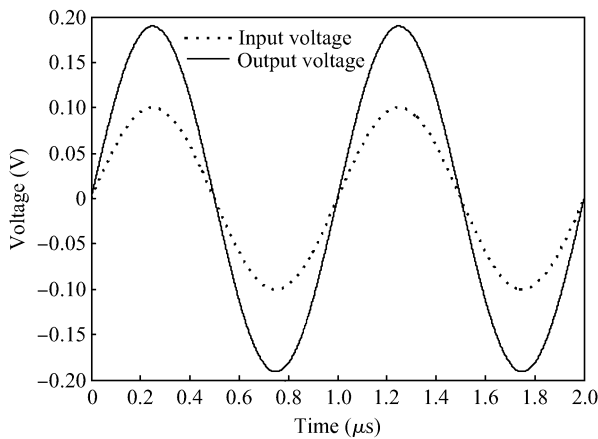
(c)

Fig. 5. Voltage amplifier. (b) FL-based voltage amplifier. (c) SPICE input and output signals of our FL-based voltage amplifier.

ism). For deep nanoscale transistors ($L < 10$ nm), new transport and mobility mechanisms (ballistic transport, modulation length ...) should be taken into account in our numerical simulations.

In order to show the impact of our approach on the nanoscale circuit design, we propose the simulation of the analog nanoscale CMOS amplifier (Fig. 5) and digital NAND gate (Fig. 6), which are considered as the most basic elements of analog and digital VLSI circuits[22]. Each circuit consists of several nanoscale DG MOSFETs. The I–V characteris-

Table 3. Computational cost for the analysed circuits.

Model	FL-based model	NEGF-based model[10]
Voltage amplifier	3.2 s	Several hours
Digital NAND gate	5.1 s	Several hours

tics of each transistor were predicted using an ABM (analog behavioural modeling) FL-based DG MOSFET model. The parameters used for simulation are as follows: $L = 10$ nm, $t_{ox} = 1$ nm and $t_{si} = 3$ nm. The proposed circuit has been implemented in a standard electronic simulator (SIMSCAPE-SIMULINK) as shown in Fig. 6. In order to prove the effectiveness of the proposed approach for nanoscale low power and high frequency applications, the supply voltage is fixed at 1 V for both circuits and the input voltage frequency is fixed at 1 GHz for the digital gate circuit. The purpose of this simulation is to study the electrical behavior, time computation and evolution of output voltages for both circuits.

Figure 7 shows the input and output voltages for both investigated circuits. This figure clearly shows the obtained analog voltage gain ($G_v = 2$) for the first circuit and the digital operation (NAND) carried out by the second one. It is important to note that our FL-based DG MOSFET model can be realistically extended to study other complex practical nanoelectronic circuits like nanoprocessors and memory cells.

The forgoing simulation results show that the FL-based DG MOSFET model makes it feasible to include quantum effects accurately and generally in nanoelectronic circuit simulations. In this section, we go further to show that the proposed FL-based DG MOSFET model is in fact quite efficient in accomplishing this. In particular, we calculate the computational cost of the FL-based DG MOSFET circuits for the simulations carried out in this section. For the purpose of the simulation of the circuits shown in Fig. 5, routines and programs for FL computation were developed using MATLAB 7.7 and all simulations are carried out on a computer with a 2.5 GHz CORE (TM) I3 CPU and 4 GB RAM. Table 3 gives a comparison of the CPU (central processing unit) time requirements for simulating FL-based DG MOSFET circuits with a numerical NEGF-based approach. Obtained results can be explained by the fact that the FL is characterized as a computational model based on behavioral and parallel distributed processing of data. Since the FL-based model is only moderately more computationally demanding than the associated numerical models, it can even be feasible to study other structures more complex than the DG MOSFET. Therefore, the FL-based modeling provides a practical insight into quantum effects in nanoscale electronic devices without the uncertain accuracy or meticulous tuning effort that face more rigorous numerical quantum models.

4. Conclusion

In this paper, we showed the applicability of the FL approach to the nanoscale CMOS circuit simulation problem. The use of 2D NEGF-based numerical simulations enabled us to build the required knowledge database in order to evaluate and optimize our nanoscale DG MOSFET compact model. The behavior modeling process was completed in a relatively short time, with no need for user intervention during the computa-
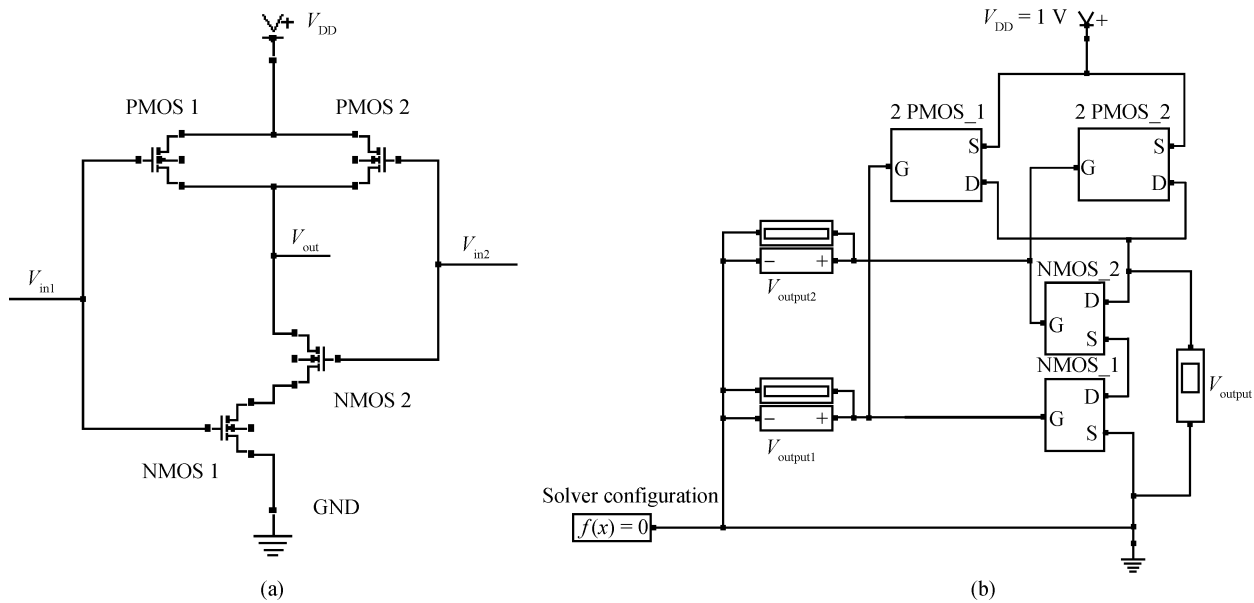
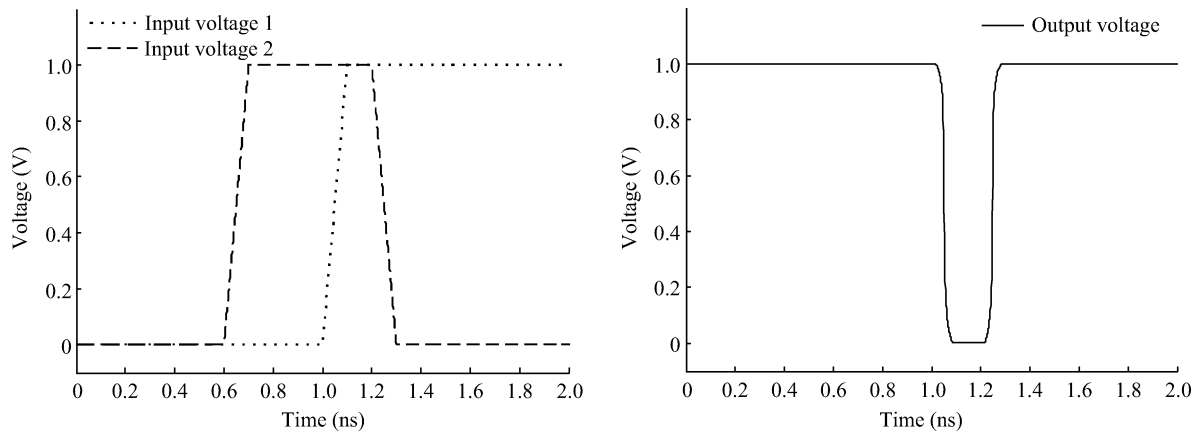Fig. 6. (a) NAND gate. (b) FL-based NAND gate.

Fig. 7. SPICE input and output signals of our FL-based NAND gate.

tion. The proposed approach was tested in two different circuits: in a low power voltage amplifier and in a nanoscale NAND gate. It is noted that the proposed approach can be extended to include other complex phenomena in nanoscale regimes like: hot-carriers, aging phenomena and length modulation in the nanoscale domain, which cannot be modeled using a conventional analytical approach. The obtained results have indicated that the developed FL-based approach is particularly suitable to be incorporated in electronic device simulators to study the nanoscale CMOS circuits. Therefore, the FL-based modeling is a step towards a new generation of simulation tools that will allow device and circuit engineers to explore new classes of nanoscale electronic devices.

References

[1] Colinge J P. Multiple-gate SOI MOSFETs. Solid-State Electron, 2004, 48: 897

[2] Djeffal F, Bendib T, Abdi M A. A two-dimensional semi-analytical analysis of the subthreshold-swing behavior including free carriers and interfacial traps effects for nanoscale double-gate MOSFETs. Microelectron J, 2011, 42: 1391

[3] Barin N, Braccioli M, Fiegna C, et al. Analysis of scaling strategies for sub-30 nm double-gate SOI N-MOSFETs. IEEE Trans Nanotechnol, 2007, 6: 421

[4] International Technology Roadmap for Semiconductors (ITRS). Published online at http://public.itrs.net, 2009

[5] Taur Y, Liang X, Wang W, et al. Continuous, analytic drain-current model for DG MOSFETs. IEEE Electron Device Lett, 2004, 25: 107

[6] Fossum J G, Ge L, Chiang M H. Speed superiority of scaled double-gate CMOS. IEEE Trans Electron Devices, 2002, 49: 808

[7] Abdi M A, Djeffal F, Arar D, et al. Numerical analysis of double-gate and GAA MOSFETs with trap states. J Mater Sci: Mater Electron, 2008, 19: 248

[8] Venugopal R, Ren Z, Datta S, et al. Simulating quantum transport in nanoscale MOSFETs: real vs mode space approaches. J Appl Phys, 2002, 92: 253

[9] Munteanu D, Autran J L, Loussier X, et al. Quantum short-channel compact modeling of drain current in double-gate MOS-FET. Solid-State Electron, 2006, 50: 680

[10] Ren Z, Venugopal R, Goasguen S, et al. NanoMOS 2.5: a

two-dimensional simulator for quantum transport in double-gate MOSFETs. IEEE Trans Electron Devices, 2003, 50: 1914

[11] Foty D. MOSFET modeling with SPICE: principles and practice. Prentice Hall PTR, 1997

[12] Picos R, Calvo O, Iniguez B, et al. Optimized parameter extraction using fuzzy logic. Solid-State Electron, 2007, 51: 683

[13] Djeffal F, Chahdi M, Benhaya A, et al. An approach based on neural computation to simulate the nanoscale CMOS circuits: application to the simulation of CMOS inverter. Solid-State Electron, 2007, 51: 26

[14] Djeffal F, Abdi M A, Dibi Z, et al. A neural approach to study the scaling capability of the undoped double-gate and cylindrical gate all around MOSFETs. Mater Sci Eng B, 2008, 147: 239

[15] Yager R R, Zadeh L A. An introduction to fuzzy logic applications in intelligent systems. Norwell, MA: Kluwer, 1991

[16] Mishra K, Sarma I G, Swamy K N. Performance evaluation of two fuzzy-logic-based homing guidance schemes. J Guid Control Dyna, 1994, 17: 1389

[17] Esposito M, Pietro G D. An ontology-based fuzzy decision support system for multiple sclerosis. Engineering Applications of Artificial Intelligence, 2011, 24: 1340

[18] Smit G D J, Scholten A J, Curatola G, et al. PSP-based scalable compact FinFet model. NSTI-Nanotech, 2007, 3: 520

[19] Moldovan O, Jimenez D, Guitart J R, et al. Explicit analytical charge and capacitance models of undoped double-gate MOSFETs. IEEE Trans Electron Devices, 2007, 54: 1718

[20] Kolberg S, Borli H, Fjeldly T A. Modeling, verification and comparison of short-channel double gate and gate-all-around MOSFETs. Mathematics and Computers in Simulation, 2008, 79: 1107

[21] Reyboz M, Martin P, Poiroux T, et al. Continuous model for independent double gate MOSFET. Solid-State Electron, 2009, 53: 504

[22] Taur Y, Ning T H. Fundamentals of modern VLSI devices. Cambridge (UK): Cambridge University Press, 1998