High-speed through-silicon via filling method using Cu-cored solder balls*

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Abstract: A novel low-cost and high-speed via filling method using Cu-cored solder balls was investigated for through-silicon via manufacture. Cu-cored solder balls with a total diameter of 100 μm were used to fill 150 μm deep, 110 μm wide vias in silicon. The wafer-level filling process can be completed in a few seconds, which is much faster than using the traditional electroplating process. Thermo-mechanical analysis of via filling using solder, Cu and Cu-cored solder was carried out to assess the thermo-mechanical properties of the different filling materials. It was found that the vias filled with Cu-cored solder exhibit less thermal-mechanical stresses than solder-filled vias, but more than Cu-filled vias.

Key words: microsystem packaging; through-silicon vias; filling method; metallization; thermal-mechanical properties

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1. Introduction

3D integration using through-silicon vias (TSVs) has become a wide research topic for the advanced integration of heterogeneous materials and devices[1,2], promising shorter vertical interconnects and associated potential benefits of higher performance, smaller form factor and lower cost. However, the cost of TSVs fabrication is one of the impediments limiting the application of TSVs.

The desired attributes of TSV fabrication are reliability, low cost and high yield, while achieving high speed and density with low parasitics and cross talk in well-designed applications. Normally, the traditional TSV manufacturing process includes via forming, insulation, barrier/seed layer deposition and via filling. Copper via filling is subject to the formation of undesirable voids, which may contain plating fluid. The formation of void-free TSVs is a persistent challenge. Other conducting via filling materials, notably, tungsten and highly doped polycrystalline silicon, are the subject of sporadic investigation. In addition to voiding, copper filling of vias is subject to other unwanted characteristics, among which are: (1) a thin or missing seed layer[3]; (2) long plating times, especially in filling vias with larger diameters, and tailoring the plating overburden non-uniform thickness to match the chemical mechanical planarization (CMP) non-uniform removal rate[4]; (3) a long CMP process and expensive consumable utilization[5].

Recently, via filling using molten solder materials has been proposed for high-speed and low-cost processes[6–8]. Molten solder fills the via holes under the force generated by a controlled pressure difference. The filling can be completed in several seconds. Unfortunately the coefficient of thermal expansion (CTE) mismatch between silicon and solder is very large, and can cause serious reliability issues during thermal cycling. Additionally, the conductivity of solder is low and may limit electrical performance. Finally, the solder filling process needs to employ vacuum or pressure to overcome the resisting forces, which adds more difficulties to handling thin wafers.

In this study, a novel wafer-level filling method using Cu-cored solder balls is developed for a high-speed, low-cost via filling process that only takes a few seconds to complete. Compared with solder filling processes that use vacuum or pressurized N_2 gas, the ball filling method is performed in ambient air. Thermo-mechanical analysis of TSVs filled with different materials was carried out to assess their thermo-mechanical properties.

2. Experimental and finite element analysis

The new via filling method using Cu-cored solder balls is shown in Fig. 1. First of all, blind vias with a depth of 150 μm and a diameter of 110 μm were formed on a 4-inch silicon wafer by using deep reactive ion etching (DRIE). Then, a SiO_2 layer (1000 nm) was formed by thermal oxidation on the wafer surface and the sidewall and bottom surface of the vias. As a wetting layer, Ti/Au (200 nm/100 nm) films were then sputtered onto the sidewall and the bottom surface of the vias. Subsequently, Cu-cored solder balls (provided by Hitachi Metals, Ltd.) with a diameter of 100 μm were placed into the vias. The diameter of the Cu core was 80 ± 3 μm. The Cu core coatings were 2 μm thick Ni and 8 μm thick Sn-3.0Ag-0.5Cu (wt.%). The wafer-level Cu-cored solder ball placement could be completed in 30 seconds for a hundred thousand vias, with a minimum diameter of 60–80 μm and a minimum pitch of 120 μm, using the ball placing system, e.g., a Minami MK-BP2000 ball placer. After placement, the solder balls were reflowed at 238 ℃ in ambient air. Solder reflow was completed in

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Table 1. Material properties.

Material	Young' modulus (GPa)	Poisson ratio	CTE (ppm/K)	Plastic properties (MPa)
Si	130.5 @ 200 K	0.28	1.4 @ 200 K	
	128.9 @ 300 K		2.62 @ 300 K	
	128.9 @ 400 K		3.26 @ 400 K	
SiO_2	70	0.16	0.6	
Solder	54.43 @ −40 ℃	0.35	24.5	
	41.73 @ 25 ℃			
	36.84 @ 50 ℃			
	22.19 @ 125 ℃			
Cu	132.9 @ 200 K	0.34	15.2 @ 200 K	240 @ 0ε
	128.9 @ 300 K		16.7 @ 300 K	250 @ 0.003ε
	124.5 @ 400 K		17.5 @ 400 K	255 @ 0.007ε
				255 @ 0.009ε
				250 @ 0.017ε

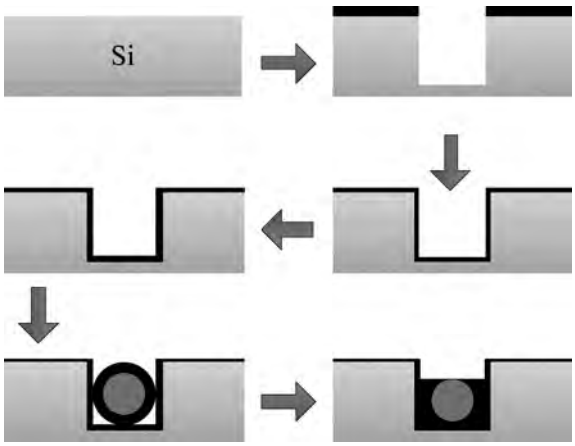

Fig. 1. Schematic illustrations of the via filling method using Cu-cored solder balls.

just a few seconds after reaching the reflow temperature. As the solder melted, the vias were filled. This via filling method can be used for interposer fabrication. Further processing, such as wafer temporary bonding, wafer thinning, redistribution layer (RDL) formation, bumping, and wafer de-bonding followed ball placement and reflow.

Samples were prepared for microstructural characterization. Diced samples were polished with 1.0 μm diamond and buffed in 0.05 μm silica suspensions. Energy dispersive X-ray (EDX) analysis was used to obtain the composition at various positions.

In order to assess the thermo-mechanical properties, 2D axis-symmetric finite element analysis (FEA) models of a silicon interposer with a via filled with solder, copper, and Cu-cored solder were analyzed, respectively. To determine the thermal stress in the TSVs, various assumptions were made[9]. The Cu-cored solder filled TSVs were assumed to be symmetric about the plane across the center of the Cu core and parallel to the wafer surface. Since the wetting layer is much thinner than the dielectric layer, its effect is negligible. Static temperature ramp-down analysis from 125 to –40 ℃ was carried out to simulate the maximum thermal stress state. The silicon interposer with TSVs was assumed to be stress-free at 125 ℃. The material properties used are shown in Table 1.

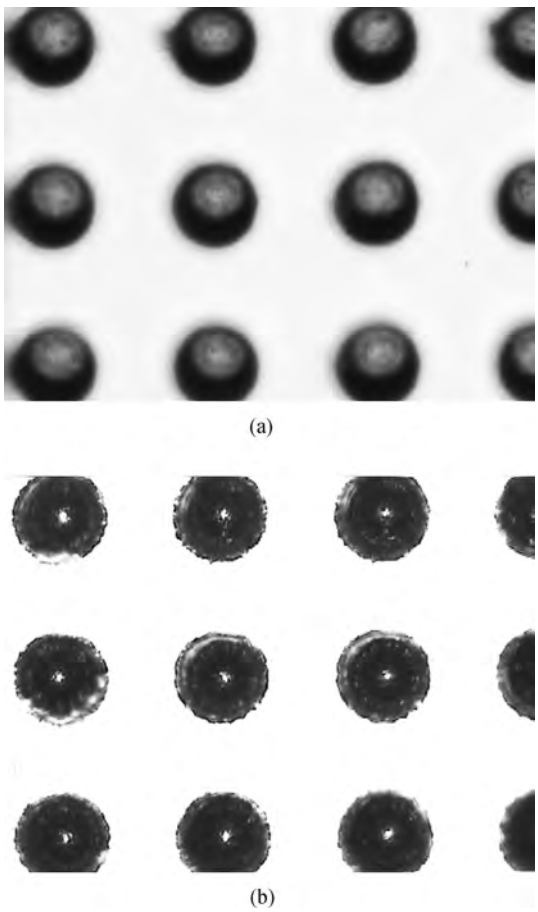

Fig. 2. Optical images of (a) empty vias and (b) after ball placement.

3. Results and discussions

Optical images of the vias before and after the placement of Cu-cored solder balls are shown in Fig. 2. The straight via depth and diameter are 150 μm and 110 μm, respectively, and the total diameter of a Cu-cored solder ball is 100 μm. One Cu-cored solder ball filled each via. The initial result for via filling with Cu-cored solder is shown in Fig. 3. It can be seen that there were no voids at the wetting interface. According to EDX analysis, the solder composition hardly changed because Ni and Ti are good barrier layers for Sn based solder materials

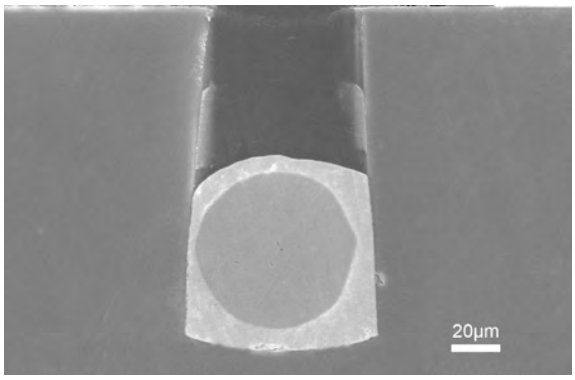

Fig. 3. A solder coated copper ball after solder reflow.

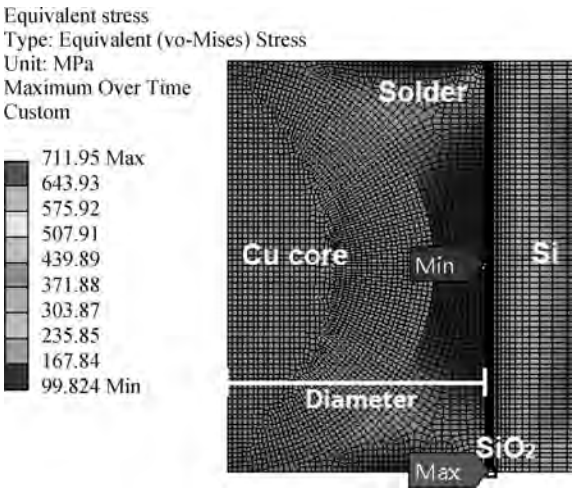

Fig. 4. Distribution of equivalent (von-Mises) stresses in Cu-cored solder TSVs structure. The via depth and diameter are 80 μm and 110 μm, respectively, and the Cu core diameter is 80 μm.

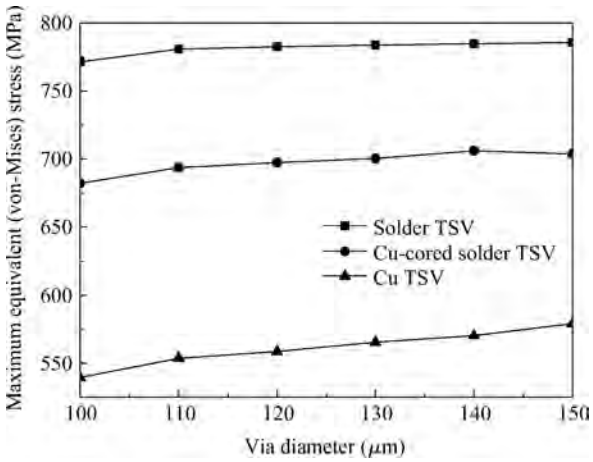

Fig. 5. Maximum equivalent (von-Mises) stresses in the TSVs for different filling materials and different via diameters. The via depth is 80 μm, and the Cu core diameter is 80 μm. The solder quantity increases as the via diameter increases.

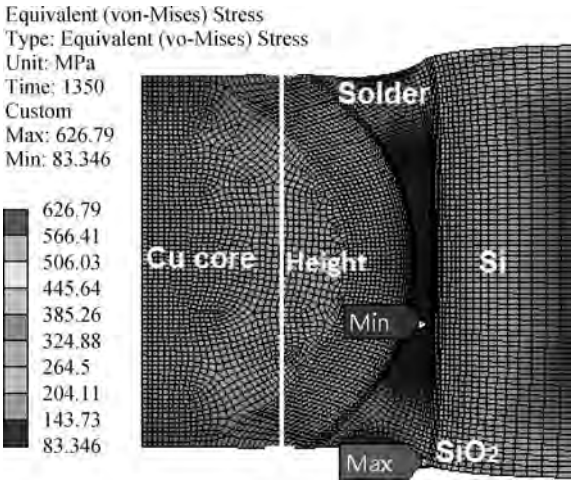

Fig. 6. Distribution of equivalent (von-Mises) stresses in Cu-cored solder TSVs structure. The via diameter is 110 μm, and the Cu core diameter is 100 μm. The TSV is assumed to be ground and polished from both sides.

and the reflow process was so short.

In order to understand the thermal-mechanical stress state of the Cu-cored solder filled TSV structures, the distribution of equivalent (von-Mises) stress due to the thermal load in the TSVs was analyzed using FEA simulation, as shown in Fig. 4. It can be seen that the maximum equivalent stress occurred at the corner of the SiO_2/Si interface and the stresses at the interface of Cu core and solder were relatively low. Reliability issues, such as delamination, were more likely to happen at the SiO_2/Si interface rather than the Cu/solder interface. The relationship between the thermal-mechanical stresses and the diameter of the TSVs was analyzed using the same FEA model shown in Fig. 4. The relationship between maximum von-Mises stresses and via diameter for different filling materials is shown in Fig. 5. It is observed that the maximum von-Mises stress of Cu-cored solder filled TSVs was much smaller than that of solder filled TSVs, but larger than that of Cu filled TSVs. In the cases of TSVs with a relatively large diameter, the thermal stresses in the solder filled TSVs were extremely large, which could introduce serious reliability issues and restrict their application. In the case of a 100 μm diameter, the maximum von-Mises stress of a Cu-cored solder filled TSV is about 12% smaller than that of a solder filled TSV. The Cu-cored solder filling method can improve the thermal-mechanical reliability and is potentially useful for the fast fabrication of TSVs with large diameters (typically 60–250 μm), as in the cases of image sensors and MEMS packaging.

The distribution of von-Mises stress due to thermal load in the Cu-cored solder filled TSVs after wafer thinning is shown in Fig. 6. The TSV was assumed to be ground and polished from both the front and back side. It can be seen that the maximum von-Mises stress occurred at the corner of the SiO_2/Si interface. The stresses at the interface of Cu core and solder are relatively low. The effects of the via depth on the thermal–mechanical stresses of TSV structures was analyzed using the same FEA model shown in Fig. 6. The relationship between maximum von-Mises stresses and via depths for different filling materials is shown in Fig. 7. It is found that the thermal stress increased with increasing via depth in the solder filled, Cu filled and Cu-cored solder filled TSV structures. When the via depth was 50 μm, the maximum von-Mises stress of the Cu-cored solder filled TSV was about 17% smaller than that

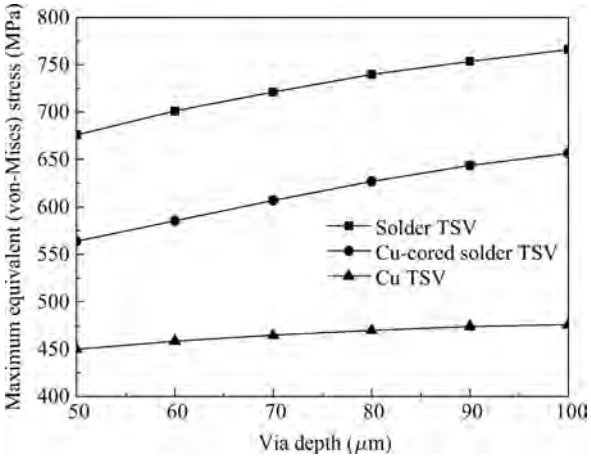

Fig. 7. Maximum equivalent (von-Mises) stresses in the TSVs for different filling materials and different via depths. The via diameter is 110 μm, and the Cu core diameter is 100 μm. The TSVs are assumed to be ground and polished from both sides.

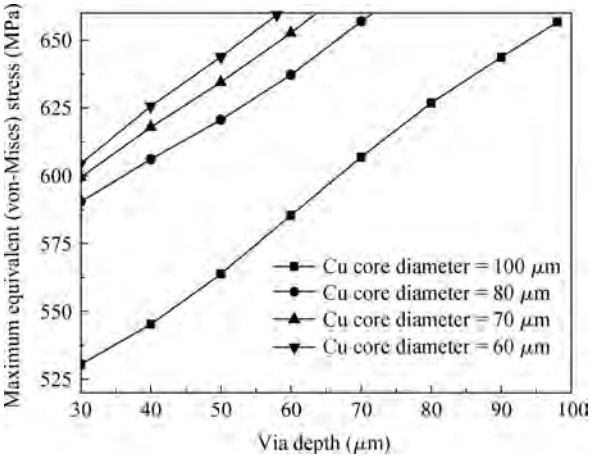

Fig. 8. Maximum equivalent (von-Mises) stresses in the Cu-cored solder filled TSVs for different Cu core diameters and different via depths. The diameter of the TSVs is 110 μm in all cases, and the Cu core diameter is 60 μm, 70 μm, 80 μm, and 100 μm, respectively.

of a solder filled TSV. We can see that Cu-cored solder filled TSVs with smaller depths can improve thermal reliability as compared with solder filled TSVs with larger depths.

In order to analyze the effects of the Cu core diameter on the thermal stresses of the TSV structure, different Cu core diameters varying from 60 to 100 μm were used in the FEA simulation. The solder quantity decreased as the Cu core diameter increased. The TSVs were assumed to be ground and polished from both sides. The relationship between maximum von-Mises stresses in the Cu-cored solder filled TSVs and Cu core diameters for different via depths are shown in Fig. 8. As expected, the maximum von-Mises stresses in the TSV structure decreased greatly with the increase of Cu core diameter. In the case of a 100 μm Cu core diameter, the maximum von-Mises stress was about 15% smaller than that of TSVs with a 60 μm Cu core diameter. This means that a larger Cu core diameter will provide higher thermal reliability.

Compared with existing via filling methods, such as Cu electroplating and molten solder filling, the Cu-cored solder filling method has several significant advantages: (1) the filling is fast, just 30 s for wafer-level ball placement and a few seconds for solder reflow, as compared to several hours for electroplating; (2) the process is simple and low cost; and (3) the thermal reliability of Cu-cored solder filled TSVs is better than that of the solder filled TSVs.

4. Conclusion

An innovative via filling method using Cu-cored solder balls was studied to offer a low-cost and high-fill-speed process for TSV fabrication. Via filling results show that void-free filling was achieved. Wafer-level Cu-cored solder ball placement can be completed in 30 s for a hundred thousand vias, and the reflow process can be completed in just a few seconds. FEA results indicate that the Cu-cored solder filled TSVs can provide higher thermal–mechanical reliability when compared with the solder filled TSVs. A larger Cu core diameter will provide higher thermal reliability.

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