A low power 14 bit 51.2 kS/s double-sampling extended counting ADC with a class-AB OTA*

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Abstract: A 14 bit 51.2 kS/s extended counting analog to digital converter (EC-ADC) is presented. Two techniques are utilized to reduce its power consumption. First, a double-sampling configuration based on a fully-floating bilinear integrator is proposed to reduce the clock frequency. Second, a class-AB operational transconductance amplifier (OTA) is designed to improve the power efficiency. In addition, the chopping technique is used to eliminate the OTA flicker noise effect. The proposed ADC is fabricated in 0.18 μm CMOS technology with a core area of 0.04 mm^2. At a 51.2 kS/s conversion rate, it achieves a 94 dB SFDR and an 11.6 bit ENOB, while consuming only 77 μW from a 1.8 V power supply. The figure of merit is only 0.48 pJ/step.

Key words: A/D converter; class-AB; double-sampling; low power

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1. Introduction

The extended counting analog to digital converter (EC-ADC) combines the accuracy of a $\Sigma\Delta$ modulation with the speed of an algorithm A/D conversion. Therefore, it becomes a competitive candidate for the application of high accuracy sensor readout circuits[1−4]. In applications such as large scale sensor arrays, a large number of ADCs are required[5]. To ensure the power consumption of the entire chip is limited to a reasonable value, each individual ADC should have an extremely low power budget. In this case, low power design becomes very important. At the same time, other advantages of EC-ADC such as high linearity and a small silicon area should not be affected by the power-saving techniques used.

In this paper, an EC-ADC with some low-power techniques is realized. At the system level, a double-sampling configuration for incremental $\Sigma\Delta$ modulators is proposed. It is based on a fully floating bilinear double-sampling integrator. By this configuration, the clock frequency of EC-ADC can be almost halved for the same conversion accuracy and rate. At the same time, the mismatch between sampling capacitors has no influence on the linearity and the total capacitor area is not increased. At circuit level, a class-AB operational-transconductor-amplifier (OTA) applicable for an EC-ADC is developed. This OTA has a higher power efficiency compared with the conventional class-A OTA. In addition, a chopping technique is used to eliminate the flicker noise effect.

2. Proposed ADC structure

2.1. Basic EC-ADC

The first order extended counting ADC is shown in Fig. 1. Two conversion modes work alternatively. At the first mode (counting mode), it works as a first order incremental $\Sigma\Delta$ modulator using a counter as decimation filter. An incremental $\Sigma\Delta$

modulator is almost same as a conventional $\Sigma\Delta$ modulator except for the reset operation[6]. The conversion of each sample V_{in} begins from the resetting of the integrator and counter. Then at phase 1, V_{in} is sampled to C_{s}; at phase 2, V_{in} and the feedback signal $d[i-1] \times V_{\text{ref}}$ are integrated to C_{f}. Assuming $C_{\text{s}} = C_{\text{f}}$, therefore

$$V[i] = V[i-1] + V_{\text{in}} - d[i-1] \times V_{\text{ref}}. \quad (1)$$

After N clock cycles,

$$V[N] = N \times V_{\text{in}} - \sum_{i=0}^{N-1} d[i] \times V_{\text{ref}}. \quad (2)$$

Then at $N+1$ clock cycle, V_{in} is not only integrated but the feedback $d[N] \times V_{\text{ref}}$ is added. So,

$$V[N+1] = N \times V_{\text{in}} - \sum_{i=1}^{N} d[i] \times V_{\text{ref}}. \quad (3)$$
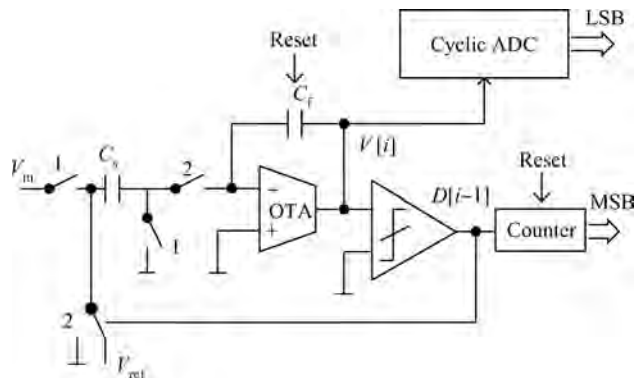
Equation (3) can be transformed to

Fig. 1. Basic first order extended counting ADC.

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$$V_{\text{in}} = \frac{\sum\limits_{i=1}^{N} d[i] \times V_{\text{ref}} + V[N+1]}{N}, \tag{4}$$

and

$$-V_{\text{ref}} < V[N+1] < V_{\text{ref}}. \tag{5}$$

From Eq. (4), the sample V_{in} is converted to digital and the output is $\sum_{i=1}^{N} d[i]$ which can be got from the counter. The residue is $V[N+1]$ which is stored at the integrator.

The first order incremental $\Sigma\Delta$ modulator is too slow. If the required resolution is n-bit, it needs 2^n clock cycles. To improve the conversion rate, the residue can be converted by a Nyquist rate ADC to get the LSB. This is the second conversion mode which is called the extended conversion. In Fig. 1, a cyclic ADC is used for extended conversion because of its simple structure. The cyclic ADC can reuse the hardware of the integrator because they don't work at the same time. After the extended conversion, the residue is converted:

$$V[N+1] = D_{\text{LSB}} \times V_{\text{ref}} + \varepsilon. \tag{6}$$

D_{LSB} is the LSB output and ε is the conversion error including quantization noise, circuit noise, nonlinearity, etc. Therefore,

$$V_{\text{in}} = \frac{\left(\sum\limits_{i=1}^{n} d[i] + D_{\text{LSB}}\right) \times V_{\text{ref}} + \varepsilon}{N}. \tag{7}$$

From Eq. (7), the error of the extended conversion is divided by N. So EC-ADC can be highly accurate. In addition, the speed improved a lot when compared with the first order incremental $\Sigma\Delta$ modulator. Assuming the required accuracy n is divided to $n_1 + n_2$ (n_1 bit MSB and n_2 bit LSB) and one clock cycle is needed to get one bit in an extended conversion, the clock cycle for converting one sample is

$$N_{\text{clock}} = 2^{n_1} + n_2. \tag{8}$$

This is a big improvement compared with 2^n.

2.2. Fully floating double sampling integrator configuration

Double sampling is a useful technique to reduce the power consumption of EC-ADC[7, 8]. If the double sampling technique is used in the modulator, two integration options can be accomplished in one clock cycle. Therefore, the exponential term in Eq. (8) will be halved, and the clock cycles needed for the conversion of each sample will be reduced. For the same conversion rate, the clock frequency is almost halved. The settling time for the OTA is doubled, resulting in smaller power consumption.

A straightforward double-sampling integrator is depicted in Fig. 2(a). Two sampling capacitors are used in this structure instead of one. During one clock phase, one sampling capacitor is used to sample the input while the other one is used to transfer charges to the integrating capacitor. During the other clock phase, the role of the two sampling capacitors is interchanged. Therefore, two integrating operations are accomplished in one clock cycle. However, the mismatch between the two sampling
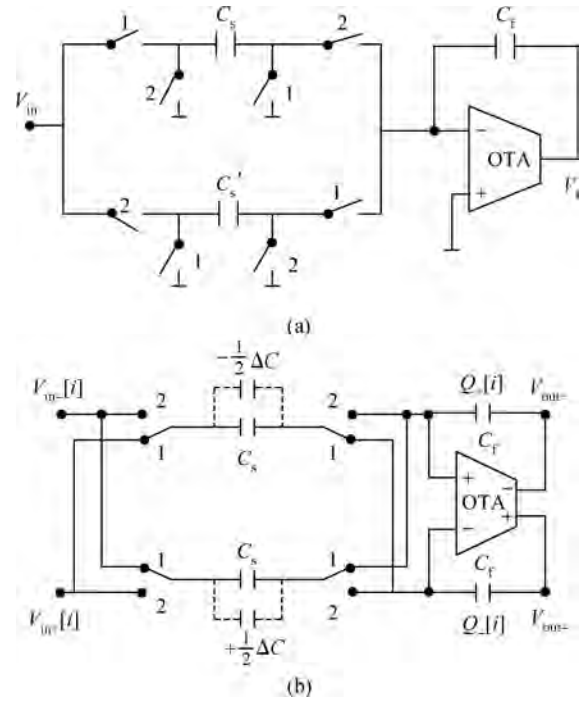

Fig. 2. Double sampling integrators. (a) Conventional double sampling structure. (b) Fully-floating double sampling structure.

capacitors in Fig. 2(a) may degrade the conversion accuracy. In addition, more capacitors are needed, resulting in a larger silicon area.

In this paper, a double sampling configuration based on the fully floating double sampling integrator is proposed. A fully floating integrator is sketched in Fig. 2(b). This integrator has a fully differential configuration. At each of the two clock phases, both sampling and integrating operations are accomplished. Therefore, the double-sampling function is achieved. In addition, at each phase, the integrator accumulates not only the sampling result of the current phase but also that of the previous phase, so it is actually a bilinear integrator. Assuming the input is a fully differential signal with 0 common mode voltage, the charges transferred to the integrating capacitors at ith step are

$$\begin{cases} Q_+[i] = -(V_{\text{in}-}[i] - V_{\text{in}+}[i-1]) \times \left(C_s + \dfrac{1}{2}\Delta C\right), \\[2mm] Q_-[i] = -(V_{\text{in}+}[i] - V_{\text{in}-}[i-1]) \times \left(C_s - \dfrac{1}{2}\Delta C\right). \end{cases} \tag{9}$$

As shown in Fig. 2(b), C_s is the average capacitance of the two sampling capacitors and ΔC is the difference between them. The differential charge is

$$Q_+[i] - Q_-[i] = (V_{\text{in, dm}}[i] + V_{\text{in, dm}}[i-1]) \times C_s. \tag{10}$$

The common-mode charge is

$$Q_+[i] + Q_-[i] = (V_{\text{in, dm}}[i] + V_{\text{in, dm}}[i-1]) \times \frac{1}{2}\Delta C. \tag{11}$$

In Eqs. (10) and (11), $V_{\text{indm}}[i] = V_{\text{in}+}[i] - V_{\text{in}-}[i]$. Equation (10) indicates that the differential output of the integrator is only dependent on the average capacitance C_s and
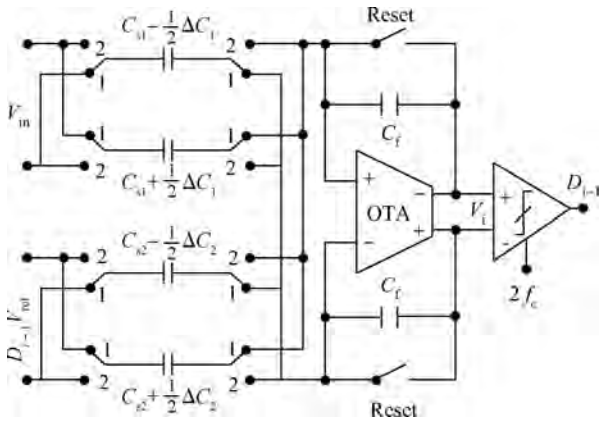
Fig. 3. Proposed first order incremental ΣΔ modulator.

Fig. 4. Chopping technique.

Fig. 5. Cyclic ADC realization. (a) Odd clock phase. (b) Even clock phase.

the error component ΔC has no impact on it. Therefore, the influence of the mismatch error on conversion accuracy is eliminated. Equation (11) indicates ΔC has small impact on common-mode charge of integrating capacitors. As a result, the common-mode input level of the OTA is influenced a little.

The fully floating integrator is able to eliminate the accuracy degeneration caused by capacitor mismatch. However, the main problem is that the input nodes of the OTA are always floating during the integrating process. As a consequence, the dc level of these nodes is not well-defined. When used as a building block, a proper phase is needed to decide the dc level of the floating nodes and recharge them frequently. In Ref. [7], only the sampling of the feedback signal uses the fully floating structure. The sampling of the input signal still uses conventional double sampling shown in Fig. 2(a) to set the dc level of the floating node. This method needs two more sampling capacitors.

In this paper, both input and the feedback are sampled by the fully floating technique. The dc level of the floating node is set during the reset phase of the incremental ΣΔ modulators. The integrators need to be reset before the conversion of each sample. Therefore the DC level of the floating nodes can be set periodically. The proposed structure of the first order incremental ΣΔ modulator is depicted in Fig. 3. Two pairs of fully floating sampling capacitors are used, one for the sampling of the input signal and the other for that of the feedback reference signal. During the reset phase of each conversion, the DC level of the floating nodes is set to ensure the OTA works properly. Because two integrating operations are accomplished during one clock cycle, the comparator works at a frequency of $2f_C$ (f_C is the clock frequency).

Fully floating double-sampling integrators are well suited for incremental ΣΔ modulators because the reset phase can be used to charge the floating nodes frequently. Although the proposed modulator (in Fig. 3) needs one more pair of sampling capacitors than the conventional single-sampling modulator, its total capacitance is kept unchanged. This is because of the bilinear integration characteristic of the fully floating integrator. Therefore, the value of the sampling capacitors is halved to keep the coefficient the same as that of the forward Eular or backward Eular integrators.
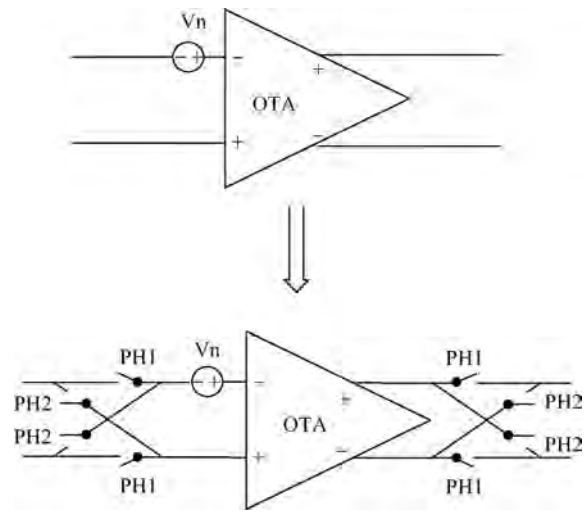
2.3. Chopping

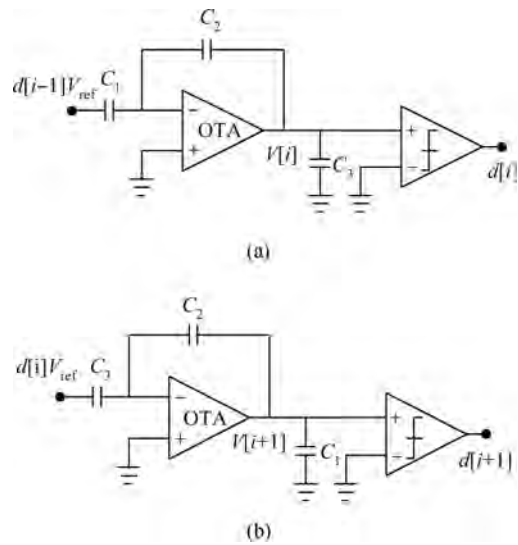For sensor readout applications, it is very important to eliminate the effect of transistor flicker noise. Auto-zeroing and chopping are two techniques used for this purpose. The auto-zeroing technique is not suitable for the double sampling integrator. Therefore, the chopping technique is used in this paper. The chopping scheme is shown in Fig. 4. By switching both input and output to the OTA, the polarity of the OTA noise is switched alternatively. Then the low frequency noise can be averaged out by the integration operation.

2.4. Extended conversion

A cyclic ADC is used for the extended conversion. Cyclic ADC has a very compact structure, so it fully reuses the hardware of the integrator. This hardware reuse technique reduces the silicon area.

The cyclic ADC scheme is shown in Fig. 5. A single-ended structure is sketched here for simplicity. A fully differential cir-

cuit is used when implementation. At the beginning of the ith step, C_1 is charged with $V[i-1]$. At the end of this step,

$$V[i] = V[i-1] + \frac{C_1}{C_2} \times (V[i-1] - d[i-1] \times V_{\text{ref}}). \quad (12)$$

At the $(i+1)$th step, the roles of the capacitors C_3 and C_1 are interchanged and the following equation is obtained:

$$V[i+1] = V[i] + \frac{C_3}{C_2} \times (V[i] - d[i] \times V_{\text{ref}}). \quad (13)$$

Capacitors C_1, C_2 and C_3 are nominally equal, as a result, the last two equations simplify to,

$$V[i] = 2 \times V[i-1] - d[i-1] \times V_{\text{ref}}. \quad (14)$$

So the cyclic conversion is realized[9]. The OTA, comparator and capacitors reuse the hardware of the integrator. Each conversion step needs only one clock phase. Therefore, two cyclic operations are accomplished in every clock cycle.

2.5. RSD technique

The redundant signed digit (RSD) technique is used in the cyclic ADC[9]. According to this technique two comparators are used to get a 1.5-bit digital output. Because of the RSD technique, the requirements of the comparator accuracy are relaxed. Therefore, dynamic comparators can be used for low power consumption.

EC-ADC is actually a two-step conversion structure. The residue of the first step (counting conversion) should be limited within the conversion range of the second sub-ADC (cyclic ADC). So the RSD technique is also beneficial to the counting conversion. Without the RSD technique, the residue of the counting conversion is bounded by $[-V_{\text{ref}}, V_{\text{ref}}]$, which is exactly the conversion range of the cyclic ADC. However, if the OTA or comparator has an offset error, the residue would exceed this range and lead to nonlinearity. With the use of the RSD technique, the nominal range of the residue is smaller so the offset error can be tolerated to some extent. Therefore, the RSD technique is also used during the counting conversion to relax the requirements of the comparator and OTA offset.

2.6. ADC structure

The analog part of the proposed ADC is shown in Fig. 6. Two comparators with different threshold voltages are used to get a 1.5-bit digital output (the RSD technique). V_B is the feedback reference signal and its value is dependent on the output of the comparators according to the following equation:

$$V_B = V_{B+} - V_{B-} = \begin{cases} +V_{\text{ref}}, & D_1 = D_0 = 1, \\ 0, & D_1 = 0, D_0 = 1, \\ -V_{\text{ref}}, & D_1 = D_0 = 0 \end{cases} \quad (15)$$

During the counting conversion, the circuit is configured as the proposed double-sampling incremental $\Sigma\Delta$ modulator shown in Fig. 3. During the extended conversion, the hardware is reconfigured as a cyclic ADC described above. The building blocks include one OTA, two comparators and eight capacitors with the same capacitance and the system is very compact.
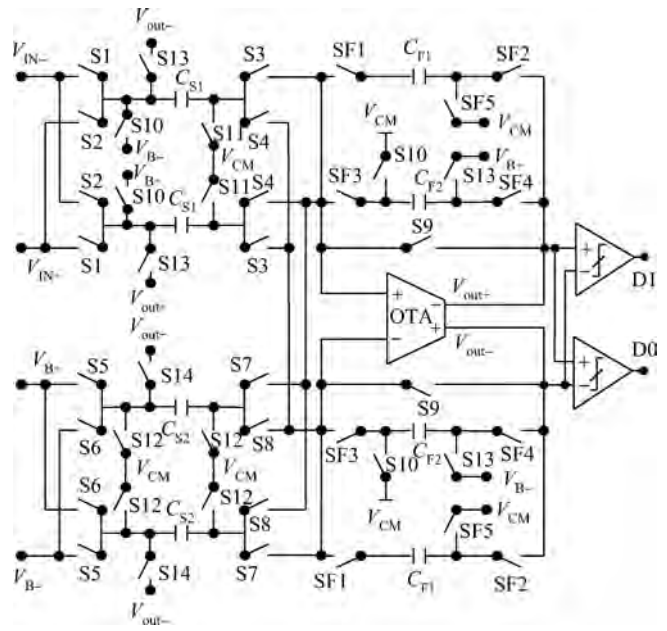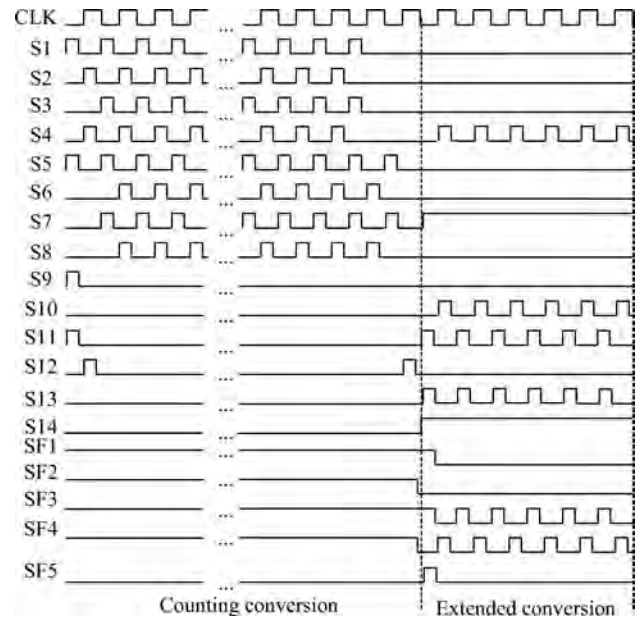

Fig. 6. ADC architecture.

Fig. 7. Timing diagram.

The timing diagram is depicted in Fig. 7. Assuming the capacitor mismatch limits the accuracy of the cyclic ADC to 10 bits, the resolution of the counting conversion is set to be 5 bits ($n_1 = 5$) to meet the accuracy requirement (14 bit) of the entire ADC while the remaining 1 bit accuracy is redundant. As shown in Fig. 7, the counting conversion needs 18 clock cycles. Because of the double-sampling technique, the actual oversampling ratio is 32 (2^5). The other four clock phases are used for resetting and adjusting the residue voltage to make it suitable for an extended conversion. The extended conversion occupies 6 clock cycles, and 12 cycling operations are accomplished. Therefore, the conversion of each sample needs 24 clock cycles. After the conversion, a 17-bit digital output is obtained. It can be truncated to 14 bit because the target reso-
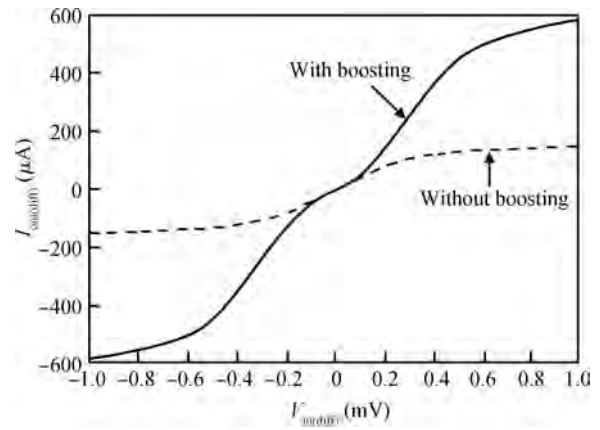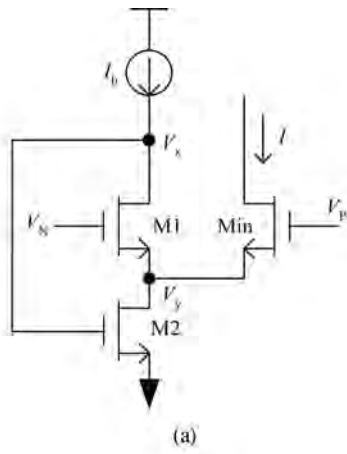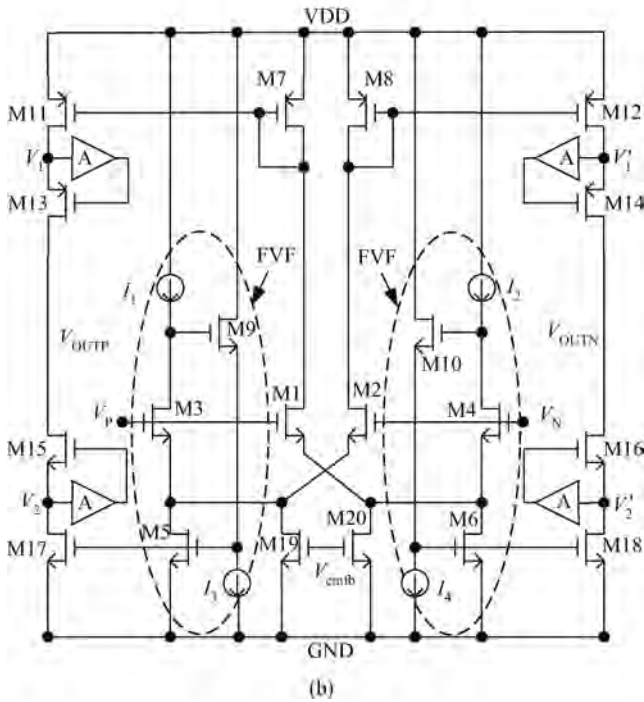
(a)

Fig. 9. DC transfer characteristics.

Fig. 8. Proposed class-AB OTA. (a) Basic flipped voltage follower. (b) OTA circuit.

lution is 14 bit.

3. Circuit implementation

3.1. Class-AB OTA

The power efficiency of a conventional class-A OTA is very low because its slew-rate is limited by a steady bias current. To increase the slew-rate, the constant current must be increased resulting in a large standby power consumption. Class-AB OTA consumes little static current during the steady state but has the ability to provide a large transient current during the settling process[10]. This characteristic makes a class-AB OTA a more power-efficient structure for the switched-capacitor integrator. In this paper, a high power-efficient class-AB OTA structure suitable for extended counting ADC is used.

The proposed class-AB OTA is based on a cell called a "flipped voltage follower" (FVF)[11]. As shown in Fig. 8(a), I_b,

M1 and M2 form a basic FVF cell. Because the current of M1 is held constant, V_y follows V_N. The negative feedback from V_x makes V_y a low impedance node which is able to sink a large current. When used in a class-AB OTA, Min is one input transistor. V_P and V_N are the differential input signals. Due to the non-limited sinking capability of V_y, the drain current of Min could keep increasing as long as the difference between V_P and V_N gets larger. If this current is used as the output current of an OTA, the slew rate would not be limited by a constant bias current.

The OTA is depicted in Fig. 8(b). It uses a similar structure to Ref. [10] except for the four gain boosters. A variant of the basic FVF cell is used in this structure. In Fig. 8(a), the valid range of V_N is very small, in order to keep both M1 and M2 work in saturation. To enlarge the input range of the FVF cell, a source follower can be used to shift the dc level between V_x and the gate of M2. In Fig. 8(b), I_1, M3, M5, M9 and I_3 form a FVF cell with the level shifter (formed by M9 and I_3), which is the same as I_2, M4, M6, M10 and I_4. M1 and M2 are input transistors. If V_P goes higher than V_N, the gate–source voltage of M1 becomes larger. Due to the function of the FVF cell, the drain current of the M1 can increase without limit as long as the gate–source voltage is large enough, and this current is mirrored by the output stage of M6, M18 and M7, M11. If V_N goes higher than V_P, the same operation happens symmetrically. Therefore, the class-AB operation with a non-limited transient output current is realized. The static current is set by I_1 and I_2. M19 and M20 are used for common mode feedback.

Behavior simulation shows that a more than 85 dB DC gain is needed. Therefore, a cascode output stage is used with a gain-boosting technique[12]. The boosters perform another function besides boosting the dc gain. Assuming M11 (Fig. 8(b)) is forced to provide a large current, without the booster, the gate of M13 is constant resulting in a voltage increase at node V_1. This action may push M11 to the linear region and limit the transient output current. If the booster is used, the gate voltage of M13 can be adjusted by the booster and V_1 is set as a constant. As a result, the output transient current can be much larger resulting in a higher slew-rate.

The simulated DC transfer characteristics of the OTA (Fig. 9) confirm the theoretical postulations above. The solid curve is the one with the booster while the dashed curve is that without the booster. For both cases, the output current keeps
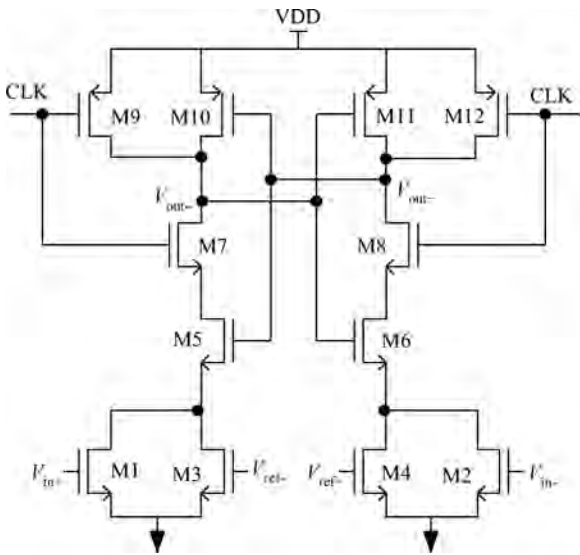
Fig. 10. Comparator schematic.

rising with the increase of input, confirming the class-AB characteristic of the OTA. At the same time, the OTA with the booster has a much larger output current when the input is big.

3.2. Comparator

A dynamic comparator, without a static current, is used in this design to reduce the power consumption. Due to the use of the RSD technique, this comparator is sufficient to meet the offset and accuracy requirements of the system. The schematic of the comparator is shown in Fig. 10. W/L of M3 and M4 is one quarter of that of M1 and M2, therefore, the threshold voltage of this comparator is $+V_{\text{ref}}/4$. By interchanging the gate voltage of M3 and M4, the threshold voltage is changed to $-V_{\text{ref}}/4$.

3.3. Simulation results

The post layout circuit simulation of the entire ADC shows that the ADC gets a 103 dB SFDR. And the power consumption of the analog parts is 70 μW while that of the digital parts is less than 5 μW. The results confirm the high linearity and low power characteristics of this ADC structure.

4. Measured results

The prototype ADC is fabricated in 0.18 μm CMOS mixed-signal technology and the chip photo is shown in Fig. 11. This chip contains 8 identical ADCs and the size of one individual ADC is only 40×950 μm^2. This layout shape is suitable for sensor array application.

The ADC works at a 1.8 V supply voltage and each ADC consumes only 77 μW at a conversion rate of 51.2 kSamples/s. When the digital output is truncated to 14-bit, the test DNL and INL are shown in Fig. 12. The DNL is 0.37/$-$0.43 LSB, and INL is 2.47/$-$1.00 LSB.

Figure 13 shows the 512000 points FFT spectrum. The input frequency is 1.1583 kHz and the conversion rate is 51.2 kS/s. The ADC achieves a 94 dB SFDR, 71.6 dB SNDR and 11.6 bit ENOB.
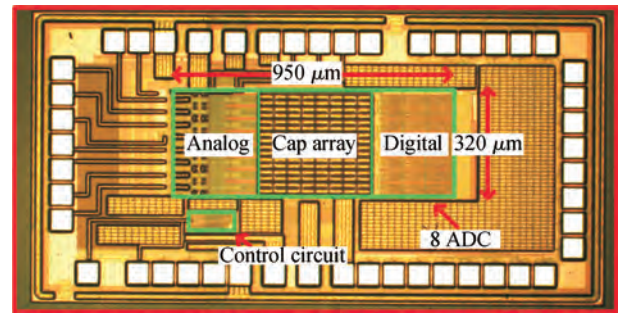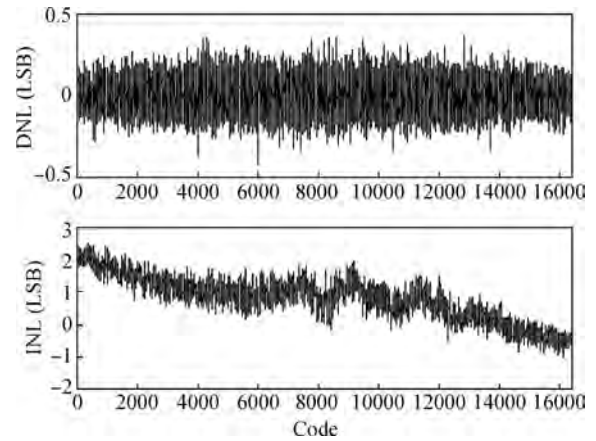

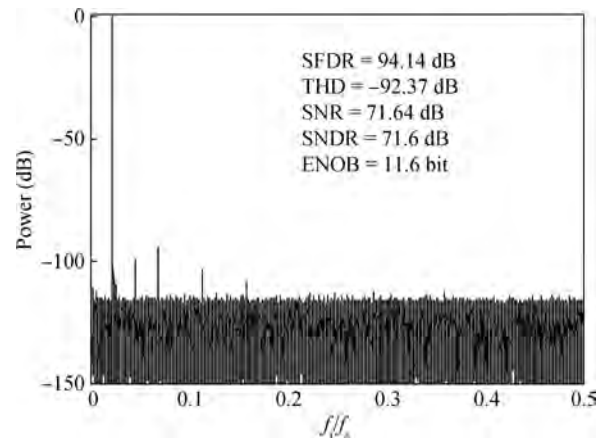Fig. 11. Chip photo.

Fig. 12. Measured DNL and INL.

Fig. 13. Measured FFT spectrum at 51.2 kS/s ($f_{\text{in}} = 1.1583$ kHz, 512000 points FFT).

Table 1 lists the performance of this design and compares it with other extended counting ADCs. In this table, FOM is calculated by the following equation

$$\text{FOM} = \frac{\text{Power}}{\text{Conversionrate} \times 2^{\text{ENOB}}}. \quad (16)$$

FOM is a good judgement of ADC power efficiency. As shown in Table 1, this work has a better FOM when compared with other designs. Therefore, the double-sampling technique and class-AB OTA do improve the power efficiency. The other advantage of this design is the small silicon area. This makes it suitable for large scale array applications.

Table 1. Performance comparison with other extended counting ADCs.

Parameter	Ref. [1]	Ref. [7]	Ref. [3]	Ref. [4]	This work
Process (μm)	0.8	0.6	0.18	0.18	0.18
Conversion rate (k Samples/s)	16	500	1000	23000	51.2
Power (mW)	0.15	48	38.1	48	0.077
Silicon area (mm^2)	1.3	0.7	3.5	0.5	0.04
SFDR (dB)	91	89	94.5	87	94
SNDR (dB)	80	81	86.3	72.2	71.6
FOM (pJ/step)	1.1	10.4	1.46	0.62	0.48

5. Conclusion

A 14 bit, 51.2 kS/s extended counting ADC is designed in this paper. A fully floating double-sampling technique and class-AB OTA structure is used to decrease the power consumption whilst not influencing accuracy and area. The ADC is fabricated in 0.18 μm CMOS technology with an area of 0.04 mm^2, and achieves a 94 dB SFDR and 11.6 bit ENOB. The power consumption is only 77 μW. This ADC is suitable for large scale sensor array applications.

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