A 7–27 GHz DSCL divide-by-2 frequency divider*

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Abstract: This paper presents the design and analysis of a high speed broadband divide-by-2 frequency divider. The proposed divider is a dynamic source-coupled logic (DSCL) structure formed with two dynamic-loading master-slave D latches, which enables high frequency operation and low power consumption. This divider exhibits a wide locking range from 7–27 GHz and the minimum power consumption is only 1.22 mW from a 1.2 V supply. The input sensitivity is as low as –25.4 dBm across the operating frequency range. This chip occupies 685 × 430 μm^2 area with two on-chip spiral inductors in 90 nm CMOS process.

Key words: broadband; frequency divider; dynamic source-coupled logic; dynamic-loading; input-sensitivity; CMOS

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1. Introduction

Frequency dividers are widely used in communication applications and they are the essential blocks of the phase-locked loops (PLLs) in conventional millimeter-wave transmitter/receivers and radio astronomy receivers/detectors. Because of the demand for low power, wide bandwidth, and high data rates in radio astronomy receiver/detectors systems, integrated circuits tend to operate at higher frequencies, lower power consumption and higher level of integration. Thanks to the continuously decreasing feature size (transistor gate length), chip area becomes smaller and smaller while the supply voltage is lowered despite of many new challenges.

There are several existing topologies for CMOS-based high-frequency FDs, such as static, dynamic and injected-locked frequency dividers (ILFDs)[1−3]. Static source-coupled logic (SCL) type FDs are considered the main vehicle in application below 10 GHz. Successful current-mode logic (CML) or dynamic SCL FDs have been normally used from 10 to 40 GHz[4−6]. From 40 to 100 GHz, an ILFD is suitable because of the limit of today's standard CMOS process[2]. On one hand, although ILFDs can achieve high operating frequency and low power consumption, they have an inherently narrow frequency locking range. On the other hand, comparing with dynamic SCL FDs, static SCL FDs consume more power in the same process. In this paper, a dynamic source-coupled logic (DSCL) structure divide-by-2 frequency divider is proposed which can work across 7–27 GHz operating frequency using IBM 90 nm CMOS technology. The presented divider achieves not only a wide input locking range but also low power dissipation at a power supply voltage of 1.2 V.

This DSCL divide-by-2 frequency divider is designed to demonstrate the function of DSCL structure latches and their capacity when operate at low input voltage amplitude and the working frequency range rather than the highest operating frequency in IBM 90 nm CMOS technology. In order to improve input sensitivity of the proposed FD, a pair of on-chip spiral inductors is used in series with the differential input signals[2, 7].

2. Divider structure

An SCL frequency divider is actually a master-slave SCL D-flip-flop that is composed of two cascaded latches. The most common published high-speed frequency dividers operating above 10 GHz are dynamic SCL frequency dividers and ILFDs. But ILFDs are not so suitable because it is difficult to achieve a wide input locking range below 40 GHz operating frequency. Therefore, dynamic SCL frequency dividers are good alternatives.

2.1. Classic dynamic SCL FD

Figure 1 shows the principle of a classic dynamic-loading SCL divide-by-2 FD proposed by Razavi[5, 8]. Each latch consists of a pair of dynamic loads (MD1, MD2) which are driven by differential clock signals, a pair of sample devices (MS1, MS2) and a pair of regenerative hold devices (MH1, MH2). Input signals IN+ and IN– are a pair of differential output signals from the voltage-controlled oscillator (VCO) circuit. When IN+ is low, MD1 and MD2 in the master (latch I) are "on" and latch I is in the sample mode, while MD1 and MD2 in the slave (latch II) are "off " and latch II is in the hold mode. When IN+ goes high, MD1 and MD2 in latch I are "off " and the master is in the regenerative hold mode. In contrast with static SCL topologies, the dynamic SCL FDs use PMOS devices as variable resistance loads instead of pure resistance loads. It is confirmed to have sped up the operating performance and avoided the trouble of choosing appropriate pure resistance loads R that used in static SCL topologies for the reason as follows. If load

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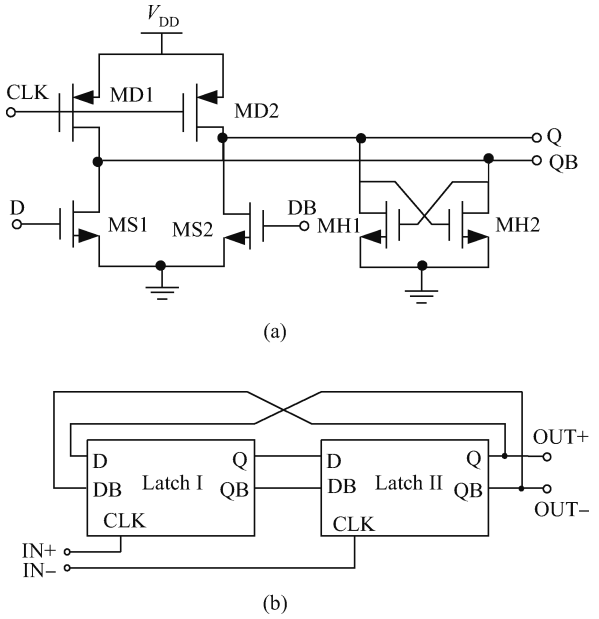


Fig. 1. Structure of Razavi's FD (a) latch (b) divide-by-2 FD with two latches.

resistance R is large, the RC time constant will increase and it will limit the top operating frequency. If R is small, the amplitude of the FD's output signals will drop and it will not be able to drive the next circuit block.

However, dynamic SCL topologies can achieve smaller resistance loads in the sample stage to ensure a small RC parasitic parameter and larger resistance loads in the hold stage to keep large output signal amplitude because of the dynamic loads' resistance varying with the voltage of clock signal (V_{CLK}) from the VCO. The dynamic loads' resistance r_{ds} of MD1 and MD2 is given by

$$r_{ds} = \frac{1}{g_{ds}} = \frac{1 + \lambda V_{DS}}{I_D \lambda} = \frac{1}{K' \dfrac{W}{2L} (|V_{GS}| - |V_T|)^2 \lambda}. \quad (1)$$

Here, λ denotes the channel-length modulation factor, K' is the process transconductance coefficient, W and L identify the length and width of MD1 and MD2. V_{GS}, V_T, I_D are the operating parameters of MD1 and MD2. In the sample mode, V_{CLK} is smaller than the DC voltage level, to wit, $|V_{GS}| = |V_{DD} - V_{CLK}|$ is larger and r_{ds} is smaller, therefore, RC parameter is smaller and the process of discharge tends to be faster. In the hold mode, V_{CLK} is larger than the DC voltage level and $|V_{GS}| = |V_{DD} - V_{CLK}|$ is smaller and r_{ds} is larger and the output amplitude will be greater. As a result, the operating frequency will go further higher.

2.2. The proposed DSCL FD

Figure 2 shows the block diagram of the proposed DSCL divide-by-2 frequency divider. The divider is formed with two feedback dynamic-loading master-slave D latches, which enables high frequency operation and low power consumption. The input clock signal is amplified by two on chip inductors to improve the input sensitivity of the FD. The pre-buffer and output buffer are used to drive 50 Ω output load.

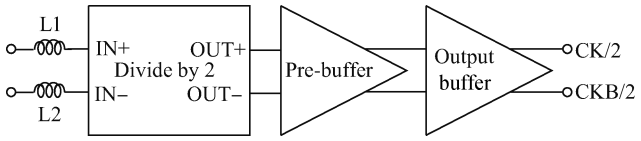


Fig. 2. Block diagram of the DSCL FD.

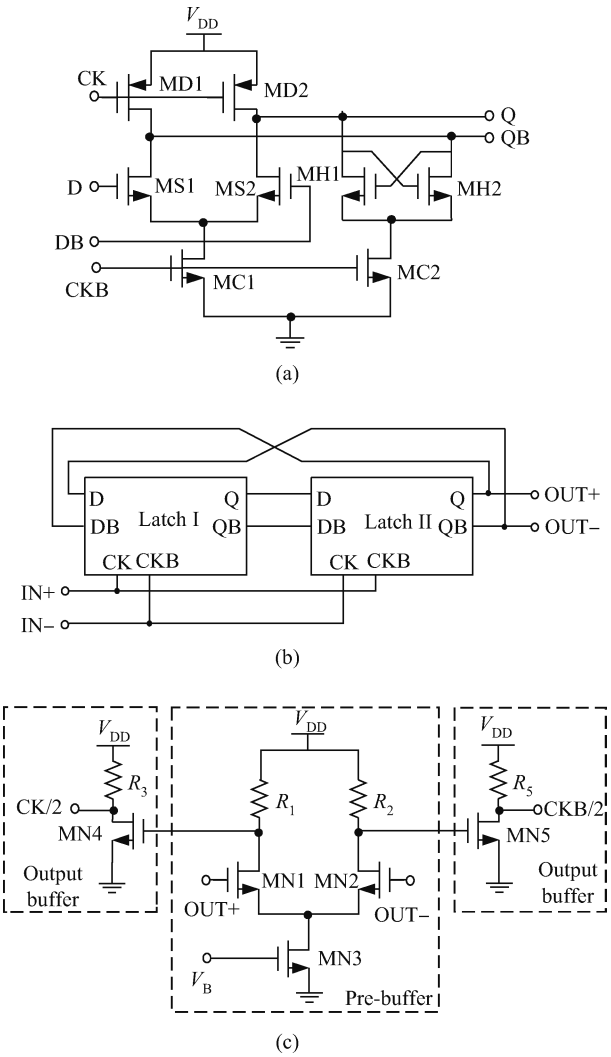


Fig. 3. Structure of the proposed FD (a) latch (b) divide-by-2 FD with two latches (c) the proposed FD's buffer.

Figure 3 shows the circuit implementation of a low power consumption dynamic SCL divide-by-2 FD. In contrast with Razavi's FD, the proposed FD consists of two identical latches and each latch has another two control transistors, MC1 and MC2. The addition of MC1 and MC2 helps switch off the latch and shut down any current path in the latch during half the clock cycles. It ensures that sample devices (MS1, MS2) and regenerative hold devices (MH1, MH2) are "off" during the hold-mode, thereby the dynamic load resistances become larger and the output impedances at Q and QB increase during the regeneration mode. This large output impedance leads to higher output swing. Furthermore, the large load resistance makes it reliable to design a lower g_m in the latch transistor pairs to drive the load and, in this case, it is possible to design

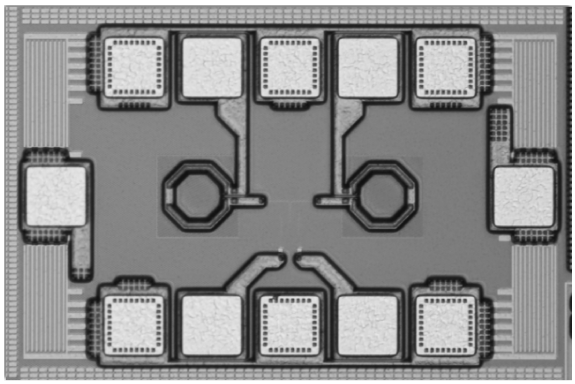
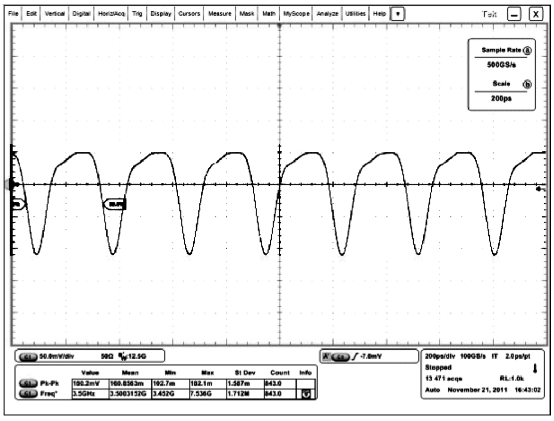
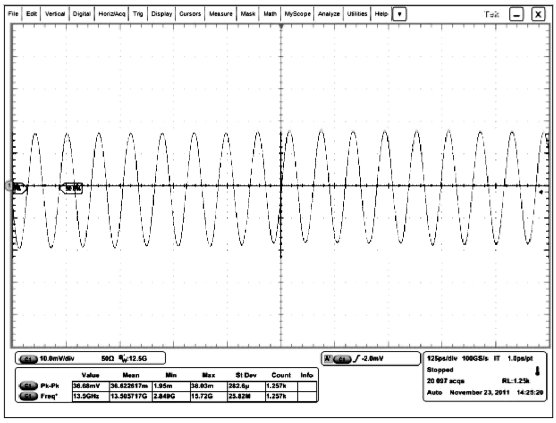


Fig. 4. Chip microphotograph of the proposed FD.



(a)



(b)

Fig. 5. The proposed FD's output waveforms. (a) 3. 5 GHz. (b) 13.5 GHz.

MH1 and MH2 smaller to decrease the parasitic capacitances during the sample-mode, which speeds up the dynamics of the latch. When input signal IN+ is low, all of the pair of dynamic loads (MD1, MD2), the pair of sample devices (MS1, MS2) and the pair of regenerative hold devices (MH1, MH2) in the master (latch I) are "on" and latch I is in the sample mode, while all of the devices in the slave (latch II) are "off" and latch II is in the hold mode. When IN+ goes high, the reverse applies.

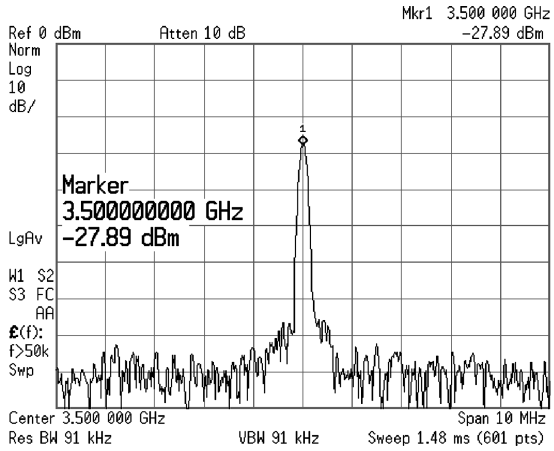
Here, some methods are considered to optimize device parameters. Firstly, find out the electron mobility of PMOS and NMOS from the PDK of IBM 90nm process and the set ratio of MD1/MD2, MS1/MS2 and MC1. Secondly, estimate the RC time constant with the target operating frequency and decide the width and length of MD1/MD2, MS1/MS2 and MC1 preliminary. Thirdly, set parameters of MH1/MH2/MC2 considering of the loop gain provided by MH1 and MH2, which increases the differential output voltage. Lastly, sweep the parameters and decide the better one by simulate the free resonating frequency. Also, a two-stage output buffer in Fig. 3(b) has been used to test the output signal connecting to 50 Ω internal impedance terminals. The first stage is a differential amplifier with low load resistance and the second stage is a source follower with a large NMOS width and current. This two-stage buffer topology yields a larger output amplitude and a lower limitation of operating frequency[6].

In order to improve the input sensitivity of the proposed FD, a pair of on-chip spiral inductors which are connected in series with the 50 Ω source has been used. They can resonate with their total input gate capacitances (C_{MD1}/C_{MD2}, C_{MC1}/C_{MD2}) and boost the effective clock signal swing Q times[7]. Here, Q is equivalent Q of the input circuit and it is not required to be very high, less than 1.5, to relax the inductor design.

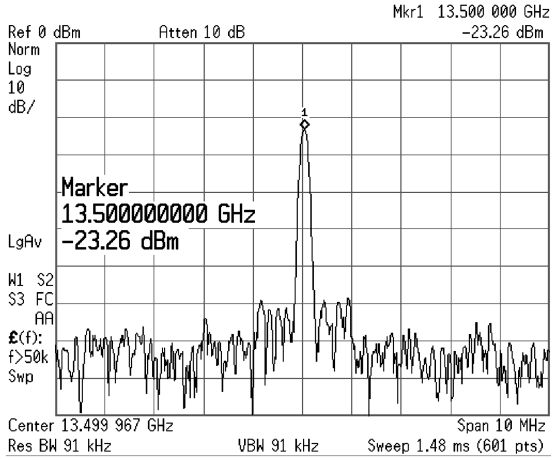
3. Measurement results

The proposed DSCL divide-by-2 frequency divider circuit has been designed in an IBM 90 nm CMOS process. Figure 4 shows the chip microphotograph of this FD. The total chip size is 685 × 430 μm^2 including the testing pads. In order to generate the differential input sinusoidal clock frequency, a 6–26.5 GHz balun was used in the input port to connect the 0.01 to 40 GHz Rohde–Schwarz SMP04 Signal Generator. A BiasT was also used to provide input bias voltage. The minimum core power consumption is 1.22 mW and the total power consumption is about 6.1 mW with two stage output buffer at 1.2 V supply. The chip has been tested across the working frequency range to investigate the upper and lower frequency limits while the minimum clock signal level required for right operation of divide-by-2 function has been swept in order to find the input sensitivity. It is found that the proposed DSCL FD is able to work in a broadband frequency range from 7 to 27 GHz. The output waveforms and output frequency spectrum of the divider are shown in Figs. 5 and 6, respectively, at an input frequency of 7 GHz and 27 GHz. Figure 7 gives the measured input sensitivity curve in different input bias voltage and the proposed scheme exhibits a very high sensitivity even at higher input frequencies by the use of on-chip spiral inductors. Due to the half circle working mode, the minimum power consumption is extremely low, as shown in Fig. 8.

The output waveforms and output frequency spectrum show that this DSCL divide-by-2 divider can work well with a wide frequency range, from 7 to 27 GHz, which is wide enough for some millimeter-wave PLL use. In normal bias voltage situations ($V_b = 600$ mV), the input power can be as low as –8 dBm ± 4 dBm at higher working frequencies. And when changing input bias voltage, this divider can work with an even lower input power at lower working frequencies (the lowest input power is –25.4 dBm @ 12 GHz). The power consumption of this divider shares a slight increase from 7 to 27 GHz input



(a)



(b)

Fig. 6. The proposed FD's output frequency spectrum. (a) 3.5 GHz. (b) 13.5 GHz.

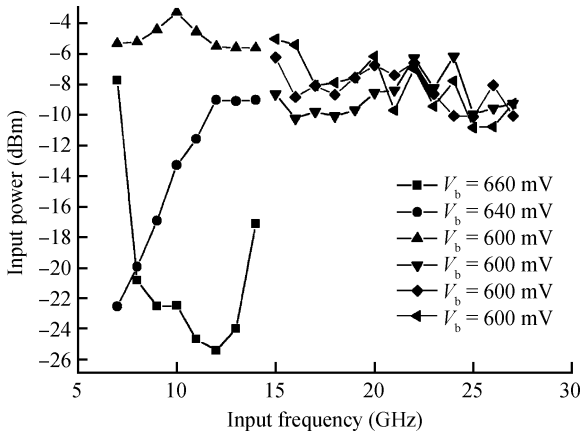


Fig. 7. Frequency divider input sensitivity versus input frequency of the proposed FD.

working frequencies, but is generally less than 4 mW.

The performance of this kind of FD is summarized in Table 1. Some previously published papers are also listed for comparison. It is superior to others in both input sensitivity and power consumption.

The proposed FD shows a wide frequency locking range,

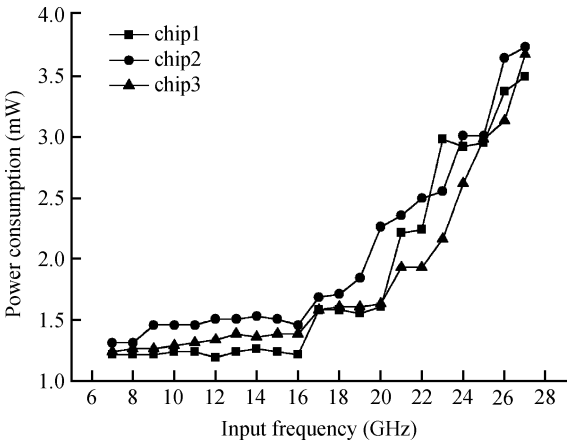


Fig. 8. The proposed FD's power consumption curve.

Table 1. Performance summary and comparison.

Parameter	CMOS-process (nm)	Freq. (GHz)	Supply (V)	PD (mW)	Core area (mm^2)
Ref. [1]	120	5–33	2.4	22.1	0.028
Ref. [8]	90	4–44	1.2	5.28	0.00076
Ref. [9]	130	20–38	1.8	12	1
This work	90	7–27	1.2	1.22	0.0048

and high input sensitivity with low power consumption. The input sensitivity versus input frequency curve shows that the input power is similar at higher input frequencies because the input amplitude after on-chip spiral inductors has increased. This is because the equivalent Q becomes higher as the operation frequency increases[7]. There are some shortcomings as well. Due to the frequency range limitation of the external input balun, to some extent, the measurement results became worse at the upper and lower frequencies. It is also obvious that when input frequency goes high, the FD dissipates more power because it needs more current to drive the divider core.

4. Conclusion

In this paper, a DSCL divide-by-2 frequency divider with a wide frequency locking range and low power consumption is proposed. Measurement results show that the locking range is 7–27 GHz. The minimum input power is 1.2 2 mW @ 7 GHz and the maximum input power is 3.48 mW @ 27 GHz. The input sensitivity is extremely high that the minimum input power is only –25.4 dBm across the operating frequency range. The measurement results also indicate that the presented DSCL FD is suitable for use in the PLL block of ALMA band-1 receivers or other ultra-wideband, low power applications.

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