Design of low power common-gate low noise amplifier for 2.4 GHz wireless sensor network applications*

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Abstract: This paper presents a differential low power low noise amplifier designed for the wireless sensor network (WSN) in a TSMC 0.18 μm RF CMOS process. A two-stage cross-coupling cascaded common-gate (CG) topology has been designed as the amplifier. The first stage is a capacitive cross-coupling topology. It can reduce the power and noise simultaneously. The second stage is a positive feedback cross-coupling topology, used to set up a negative resistance to enhance the equivalent Q factor of the inductor at the load to improve the gain of the LNA. A differential inductor has been designed as the load to achieve reasonable gain. This inductor has been simulated by the means of momentum electromagnetic simulation in ADS. A "double-π" circuit model has been built as the inductor model by iteration in ADS. The inductor has been fabricated separately to verify the model. The LNA has been fabricated and measured. The LNA works well centered at 2.44 GHz. The measured gain S_{21} is variable with high gain at 16.8 dB and low gain at 1 dB. The NF (noise figure) at high gain mode is 3.6 dB, the input referenced 1 dB compression point (IP1dB) is about –8 dBm and the IIP3 is 2 dBm at low gain mode. The LNA consumes about 1.2 mA current from 1.8 V power supply.

Key words: low noise amplifier; wireless sensor network; low power; inductor modeling; cross-coupling; positive feedback

DOI: 10.1088/1674-4926/33/10/105005 **EEACC:** 2570

1. Introduction

Recently, wireless sensor network (WSN) research has become popular. A WSM node is typically battery powered. To achieve long battery life, the power consumption of the WSN receiver must be reduced and maintain an appropriate receiver sensitivity[1−3]. The low noise amplifier (LNA) plays an important role as the first module of the receiver. The focus of this paper is on the design of a low power LNA.

Usually inductively degenerated common-source (CS) LNA topology is used at narrowband applications. This topology can provide higher gain and a lower noise figure (NF) than common-gate (CG) topology under 10 GHz[4]. But comparing with the CG LNA, it is hard to do the impedance matching at the inputs due to the interference of the ESD circuit parasitic capacitance, bonding wire parasitic inductance, the on-chip inductor modeling deviation, and so on[5]. The gain of the CG LNA is mostly not enough for the requirement of the system; the NF of CG LNA has a much higher direct impact on the sensitivity of the receivers.

In WSN applications, the nodes are positioned not very far away, so the receivers do not have to achieve very high sensitivity. The robustness of the circuit, the chip area, and the power consumption are key factors. In this paper a CG stage solution has been chosen. The consideration about the topology design is given. The schematic of the LNA circuit design and the relevant inductor modeling of the LNA are described.

2. Topology design consideration

In order to acquire 2 kV HBM ESD protection, the value of the ESD parasitic capacitance is about 200 fF[6]. The value of the bonding wire parasitic inductor is about 3 nH. They may lead to a large deviation into the input impedance of the amplifier. As stated in the introduction, it is easier for the CG stage to do impedance matching without the influence of parasitic reactance. The input impedance of the CG stage can be given by[7]

$$Z_{\text{in}} \approx \frac{R_{\text{D}}}{(g_{\text{m}} + g_{\text{mb}})\, r_{\text{O}}} + \frac{1}{g_{\text{m}} + g_{\text{mb}}}, \tag{1}$$

where g_{m} is the transconductance of the CG stage transistors, and R_{D} is the equivalent load connected to the drain of the transistor. The antenna impedance is 50 Ω. By adjusting the g_{m} and the R_{D}, it can obtain fully or partially resistive impedance that is less affected by parasitic reactance. However, it is easy to learn that the input impedance of the CG stage is relatively low only if the load impedance connected to the drain is small[7], so the R_{D} should not be too large. On the other hand, the voltage gain of the CG stage can be simplified as[7]

$$A_{\text{v}} = (1 + \eta)\, g_{\text{m}} R_{\text{D}}. \tag{2}$$

So the R_{D} impacts the voltage gain of the CG stage directly. To acquire higher gain, the R_{D} should be as large as possible. It is a contradiction on the requirements of input

* Project supported by the National High Technology Research and Development Program of China (No. 2007AA01Z2A7) and the Special Fund of Jiangsu Province for the Transformation of Scientific and Technological Achievements (No. BA2010073).

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Received 8 March 2012, revised manuscript received 20 April 2012

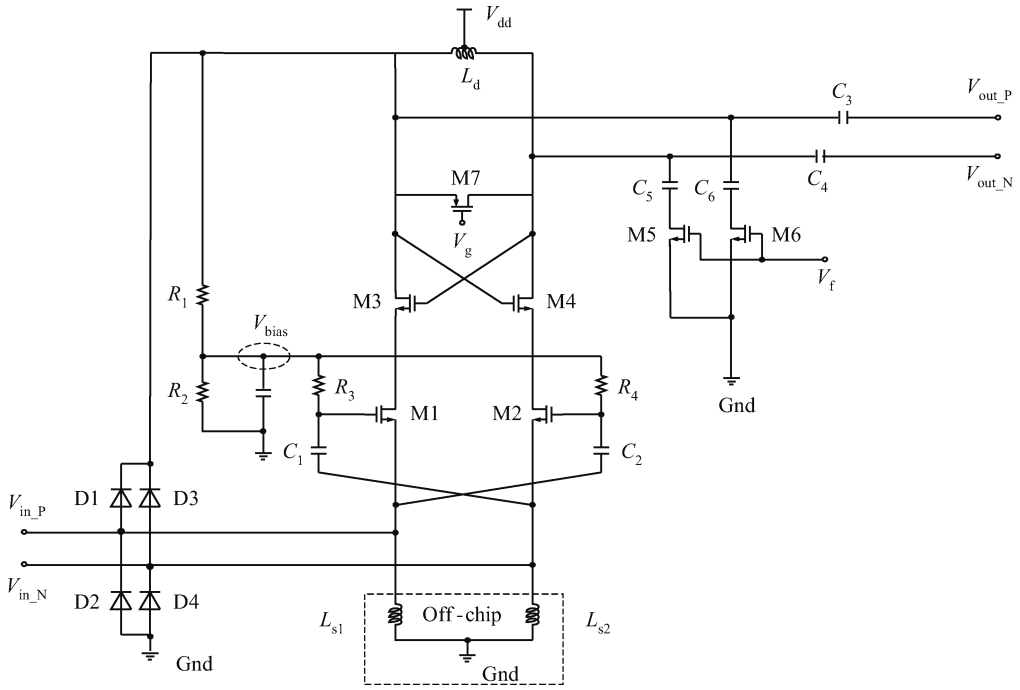


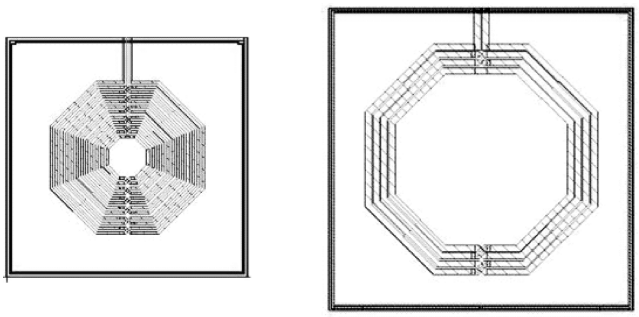
Fig. 1. Schematic of the LNA.

impedance matching. Hence the cascade CG stage topology has been chosen. The load of the circuit can be a large value connected to the drain of the second stage to improve the voltage gain. The load of the first stage is the input impedance of the second stage. It is lower than R_D itself. So it is easier to match the antenna impedance. The second stage can also isolate the signal from outputs to inputs.

In this paper a two-stage cascade CG stage solution has been chosen. Furthermore the cross-coupling technology has been used for g_m-boosting on the first stages of the LNA to obtain better matching with lower power, to reduce the noise and to enhance the gain. On the second stage, a positive feedback cross-coupling topology has been used to increase the equivalent Q factor of the inductor to enhance the voltage gain and to improve the band selection. For the purpose of providing sufficient voltage gain and occupying less chip area, an on-chip differential inductor has been designed and modeled as the load of the LNA. Considering that the distances of the nodes are variable, the LNA must be able to change the gain to avoid the saturation of the next block when the input signal is large. So, the LNA contains a PMOSFET as an active resistor as the gain control circuit at the load. Therefore, the whole LNA could achieve a good input matching, a reasonable gain, and a broad gain control range with low power consumption.

3. Circuit design

The schematic of the proposed LNA is shown in Fig. 1. Diodes D1–D4 are the input ESD protection circuit. M1 and M2 constitute the first CG stage. M3 and M4 constitute the second CG stage. R_1 and R_2 are large resistors to divider the V_{dd} to bias voltage V_{bias}. The V_{bias} is provided to M1 and M2 by R_3 and R_4 with bypass capacitance. Capacitor C_1 and C_2 constitute the first stage capacitance cross-coupling circuit. The L_{s1} and L_{s2} are external inductor choke coils providing DC path and blocking signal from grounds. L_d is a differential inductor as the load of the LNA. C_5, C_6 and M5, M6 are the frequency control circuit. C_3 and C_4 are on-chip DC-blocks. M5 constitute the gain control circuit. The source follower as the output buffer for measurement is not shown. In the receiver system, the LNA outputs are directly connected to the input of mixer as gates of the transistor. The impedance is higher than the output of LNA, so the buffer does not have to put into the system.



(a) (b)

Fig. 2. (a) The inductor new designed compares with (b) the TSMC 0.18 μm RF CMOS process provided largest inductor.

3.1. The modeling of the inductor

The value of the inductor L_d should be much larger than that of the TSMC provided inductors to achieve the gain requirement by simulation. On the other hand, on-chip inductors are bulky and area-consuming, they can occupy the majority of the available chip area. So a new designed inductor is drawn and simulated in ADS. Figure 2(a) shows the inductor. Its area is much smaller than the TSMC 0.18 μm RF CMOS process

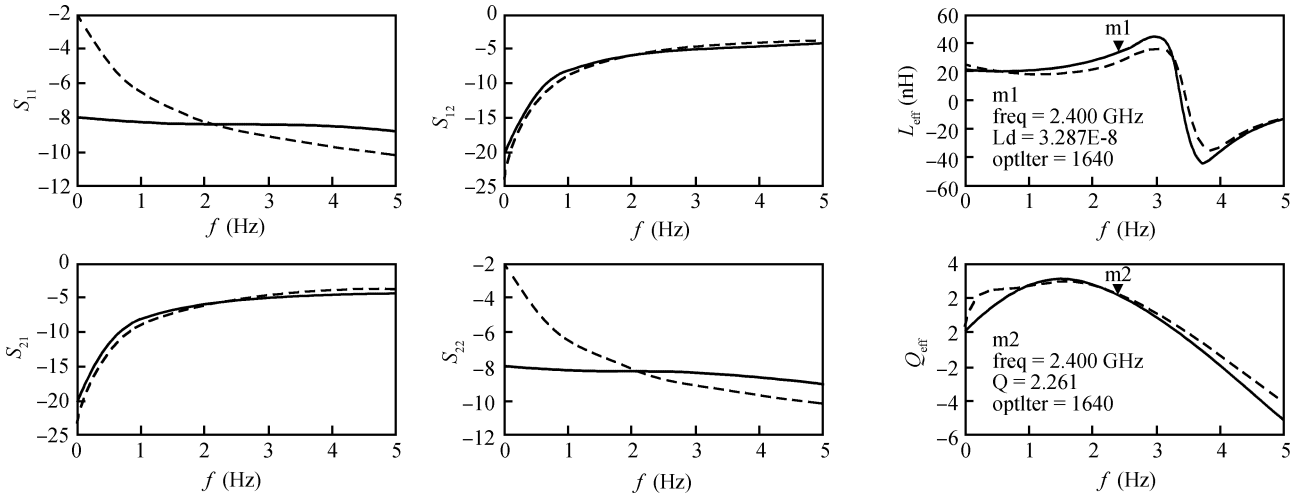


Fig. 3. S-parameters, $L_{\rm eff}$ and $Q_{\rm eff}$ simulation curve and iteration curve of the inductor model.

provided largest inductor in Fig. 2(b). Whereas the inductor TSMC can provide largest inductance at about 15 nH, the new designed inductor has a differential inductance of 32 nH.

The inductor is drawn by the top metal on the same metal layer. The inner radius of the inductor is 30 μm. The width of the metal is 3.5 μm. For 2 mA per 1 μm width of the top metal, the inductor can accept 7 mA current. It is much higher than the LNA working current. The spacing between each coil is 3.5 μm. The inductor is produced in a light N^+ region to compensate for the P^- substrate enhancing the insulation quality in order to avoid electromagnetic dissipation. There is a deep N-well guard ring surrounding the inductor to reduce the negative influence of the other circuits which are near the inductor. The area of the inductor is 350×350 μm^2.

During the simulation, the equivalent dielectric constant for two dielectric layers is given as[8]

$$\varepsilon_{\rm eq} = \frac{d_1 + d_2}{\dfrac{d_1}{\varepsilon_{\rm r1}} + \dfrac{d_2}{\varepsilon_{\rm r2}}}, \tag{3}$$

where $\varepsilon_{\rm r1}$ and $\varepsilon_{\rm r2}$ are the relative dielectric constant of the two layers, d_1 and d_2 are the distance between the boundaries in a conformably mapped plane. The data are all in the technology manual. By using the formula to compute the equivalent dielectric constant for each layer, we can get a new dielectric list of the technology for the model.

The S-parameter, Y-parameter, and Z-parameter of the inductor can be simulated by means of a momentum electromagnetic simulation in ADS. The simulation frequency is from DC to 5 GHz. And the equivalent value of the inductance $L_{\rm eff}$ and the quality factor $Q_{\rm eff}$ can be calculated as[9]

$$\begin{cases} Z_{\rm d} = Z_{11} + Z_{22} - Z_{21} - Z_{12}, \\ L_{\rm eff} = \dfrac{{\rm Im}\,(Z_{\rm d})}{\omega}, \\ Q_{\rm eff} = \dfrac{{\rm Im}\,(Z_{\rm d})}{{\rm Re}\,(Z_{\rm d})}. \end{cases} \tag{4}$$

The simulated S-parameters, $L_{\rm eff}$ and $Q_{\rm eff}$ are shown in Fig. 3 by a solid line. The self-resonant frequency of the inductor is 3.3 GHz. It attains 32 nH inductance at 2.4 GHz and

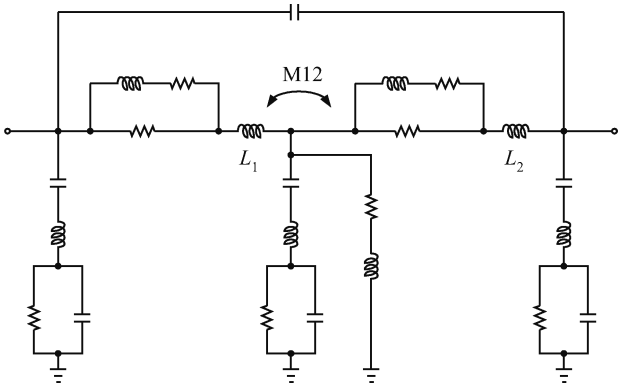


Fig. 4. The "double-π" circuit model for inductor $L_{\rm d}$.

reaches the highest value at 3.0 GHz. The $Q_{\rm eff}$ at 2.4 GHz is about 2.2. Figure 4 shows the "double-π" circuit model to build the inductor model in the LNA circuit[9]. By iteration of the value of the components on the model by using ADS iteration tools, the curve of the S-parameters, $L_{\rm eff}$ and $Q_{\rm eff}$ is shown in Fig. 3 by a short dashed line. In the vicinity of 2.44 GHz, the iteration curve and the simulation curve are close. The model can reflect the situation of the inductor $L_{\rm d}$ in the LNA circuit accurately.

3.2. Analysis of cross-coupling topology

The input impedance of a CG LNA is given by Eq. (1), which can be simplified as $1/g_{\rm m}$. The noise factor is inversely proportional to $g_{\rm m}$ too[10]. In order to achieve higher gain and lower NF, $g_{\rm m}$ should be increased. From the small signal model of the CG stage amplifier, we can find that when cross-coupling exists in the first stage, the equivalent $g_{\rm m}$ is double to $2g_{\rm m}$[11]. So the current can be nearly half down to do the matching. The input impedance matching is achieved by adjusting the size and bias current of M1 and M2 to ensure $1/(2g_{\rm m1,2})$ is equal to 50 Ω.

Compared with Ref. [11], the improvement of the design is in the second stage of the LNA. The second stage is an isolation unit to isolate the inputs and the outputs. This stage does

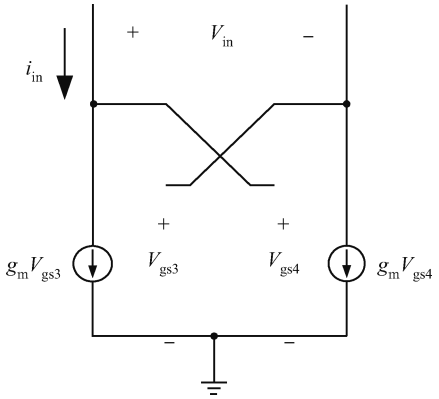


Fig. 5. Equivalent circuit of the second stage.

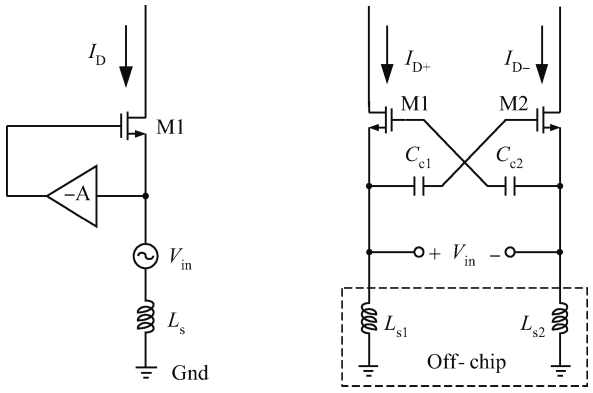


Fig. 6. G_m-boosted CG structure and capacitive cross-coupling CG LNA.

not provide current gain in Ref. [11]. But in this work, there is a cross-coupling topology on the second stage too. It is a positive feedback loop to set up a negative resistance to enhance the equivalent Q factor of the inductor at the load. Thus, the voltage gain can be enhanced indirectly without adding more power. The bias voltage of the M3 and M4 are V_{dd}, and the output DC voltage is also V_{dd}. So, we do not have to put any exceed capacitor to block the DC voltage in the cross-coupling loop.

The equivalent model of the second stage is shown in Fig. 5. The signals in M3 and M4 are a pair of differential signals, so the sources of M3 and M4 are equivalent virtual earth. The signals on the gates of M3 and M4 are equivalent to the negative V_{out} itself, respectively. The equivalent resistance from the drain of M3 and M4 can be written as

$$\begin{cases} v_{in} = v_{gs4} - v_{gs3}, \\ i_{in} = g_{m3} v_{gs3} = -g_{m4} v_{gs4}, \\ R_{in} = \frac{v_{in}}{i_{in}} = -\frac{1}{g_{m3}} - \frac{1}{g_{m4}}, \end{cases} \tag{5}$$

where g_{m3} is the transconductance of M3. g_{m4} is the transconductance of M4. As g_{m3} is equal to g_{m4}, the negative resistance is $2/g_{m3}$ paralleled into the load of the LNA, which can enhance the equivalent Q factor of the inductor at the load from 2.2 to 7.4 by simulation. This topology can improve gain from 10 to 16 dB and enhance band selection without adding more DC current. But the positive feedback loop may lead the LNA to instability. As R_p is the equivalent resistance of the LC parallel resonant network, we should keep $g_{m3} < 2/R_p$ to avoid oscillation. So during the simulation, we should monitor the stability factor k_f carefully.

3.3. Noise reduction

The noise factor of a CG stage LNA can be shown as[11]

$$F \approx 1 + \frac{\gamma}{\alpha g_m R_s}, \tag{6}$$

where γ is the channel thermal noise current coefficient, α is the short channel effect factor, and R_s is the source impedance. From Eq. (6), a direct way to reduce the NF of a CG LNA is to enlarge g_m. However, this will deteriorate the input matching performance. The g_m-boosted concept is to decouple the noise performance from the input matching. The g_m-boosted CG LNA is shown in Fig. 6, which has an effective transconductance of $(1+A)g_m$. Its noise factor is reduced to[12]:

$$F = 1 + \frac{\gamma}{\alpha(1+A)^2 g_m R_s} = 1 + \frac{\gamma}{\alpha(1+A)}\bigg|_{(1+A)g_m R_s = 1}. \tag{7}$$

The above equation suggests that noise reduction can be accomplished by increasing the values of parameters α and A or decreasing the value of parameter γ[11].

When cross-coupling, capacitors become much smaller than that of the bias resistor and the gates of the input transistors, the voltage gain of the cross-coupling network approaches 1. Therefore, the noise factor of the capacitive crossing-coupling CG stage LNA becomes

$$F \approx 1 + \frac{\gamma}{2\alpha}. \tag{8}$$

Compared with the NF of a CG stage LNA without capacitive cross-coupling, the NF is scaled down by a factor of 2. Thus, the noise factor is effectively reduced[11]. The input matching of the g_m-boosted CG LNA is implemented at a smaller bias current at the condition of $(1+A)g_m R_s = 1$. Smaller bias current also indicates less channel noise current from the input transistor.

Another way to reduce the noise in the design of the LNA can be obtained by increasing the short channel effect factor α. The factor α can be increased by augmenting the channel length of M1 and M2 in Fig. 1. A wide channel transistor can reduce the gate resistance of the MOSFETs and its associated thermal noise contribution[11]. On the other hand, the channel length determines the maximum operation frequency. After simulation, an optimized channel length of 0.3 μm is chosen for the input transistors.

3.4. Control circuit design

In order to achieve narrow-band outputs, inductor L_d and capacitances C_5 and C_6 are LC parallel resonant network as the load. M5 and M6 are the switches controlled by voltage V_f. Considering the modeling deviation of the inductor, the switches can adjust the capacitance paralleled in the LC network to change the output resonant frequency close to 2.44 GHz.

Table 1. Values of the component parameters of the LNA.

Parameter	Value	Parameter	Value
M1, M2	40 μm/300 nm	R_1, R_2	17.6 kΩ , 9.6 kΩ
M3, M4	20 μm/300 nm	R_3, R_4	10 kΩ
M5, M6	10 μm/80 nm	C_1, C_2	4 pF
M7	5 μm/250 nm	C_3, C_4	350 fF
D1, D2, D3, D4	10 μm × 10 μm	C_5, C_6	90 fF

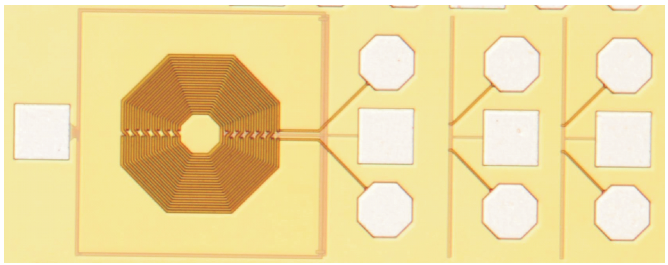


Fig. 7. Micro photo of the inductor for measurement.

Table 2. Measurement performance of the LNA.

Parameter	Value
Supply voltage	1.8 V
DC current	1.2 mA
Power consumption	2.16 mW
S_{11}	< –10 dB
S_{21} at 2.44 GHz	1–16.8 dB
S_{12}	< –50 dB
NF at high gain mode	3.6 dB
P_{1dB} at low gain mode	–8 dBm
IIP3 at low gain mode	2 dBm

By adding an active resistor on the output, the gain control of LNA can be realized. Equation (2) shows that the voltage gain of the CG stage is proportional to the load. So if the equivalent load of the LNA is reduced, the voltage gain can be lower. M7 is the active resistor. It is a PMOS transistor controlled by voltage V_g. It has a high value of R_{off} when V_g is 1.8 V. The R_{on} is about 600 Ω to parallel the equivalent load of the LNA when V_g is 0 V. It can reduce the gain of the amplifier and enhance the linearity simultaneously. After simulation and adjustment, these active resistances can adjust the gain of the LNA to the low gain mode as 0 dB in simulation.

The values of the component parameters of the LNA are shown in Table 1.

4. Measurement results

The new inductor has been fabricated separately in order to verify the model. The micro photo of the inductor is shown in Fig. 7. Measuring the S-parameter is complicated due to the deembedding. Before measuring the S-parameter, the network analyzer is calibrated to deembed any loss from the cables and the probe to the wafer connection. Furthermore, there is one open SGS pad and one short SGS pad on the right of the inductor to deembed the loss on the pad accurately. The DC pad on the left of the inductor supplies an N-well voltage for the inductor. Since the losses are all deembedded, the tested S-parameters, L_{eff}, and Q_{eff} are shown in Fig. 8. The self-resonant frequency of the inductor is 3.3 GHz. It attains 36 nH inductance at 2.4 GHz and reaches the highest value at 3.1 GHz. The Q_{eff} at 2.4 GHz is about 4.0. On the whole, the test results are close to the simulated value.

The LNA shown in Fig. 1 was fabricated in TSMC 0.18 μm RF CMOS process. The microphotograph of the LNA chip is shown in Fig. 9. The chip area is 620 × 800 μm^2 including all bonding pads and bypass capacitors. In order to minimize the contribution of the substrate resistance on the input noise, M1–M4 were divided into two parts, each part surrounded by substrate contacts[13]. In addition, each MOSFET was surrounded by a guard ring to reduce noise. Large on-chip capacitors between Vdd and ground were used for bypassing AC signals. The Vdd of the LNA and the buffer were isolated for testing power. There were some DC pads set to change the switch voltage and to detect the DC working point. The whole chip was surrounded by a seal-ring to protect the chip against potential cutting and bonding damage.

The LNA works at a 1.8 V DC power supply. It consumes about 1.2 mA current. Figure 10 shows the measured S-parameter results of the LNA working at the high gain mode in the range of 2–3 GHz. The measured S_{11} is about –13 dB at 2.44 GHz. We do not have to do any excess impedance matching on the inputs. The measured gain S_{21} of the LNA is 16.8 dB at 2.44 GHz, which reaches its highest, 18.8 dB, at 2.5 GHz due to the deviation of the inductor modeling. The S_{12} is below –50 dB what demonstrates that the isolation performance from input and output is good. We should not pay attention to the S_{22} due to the buffer. Figure 11 shows the measured S-parameter results of the LNA working at low gain mode. The S_{21} can be reduced to 1 dB at 2.44 GHz. The input matching and isolation performance are both good. The gain control circuit works well for the application.

The NF of the LNA is shown in Fig. 12, which indicates that the NF is about 3.6 dB at 2.44 GHz at high gain mode.

We pay more attention to the linearity performance at the low gain mode due to the large signal block effect. Figure 13 shows that the input-referenced 1 dB compression point is about –8 dBm and the IIP3 is 2 dBm at low gain mode. At high gain mode, the graph is not shown in this paper. The measured input referenced 1 dB compression point is about –20 dBm and the IIP3 is –10 dBm. Table 2 gives a summary of the measured results.

To evaluate the performance of the LNA, different figures of merits (FOMs) are commonly used in the literature. One FOM of the LNA (FOM_1) is the ratio of the gain in dB to the DC power consumption in mW. Furthermore, it can be extended to include the NF as follows[14]:

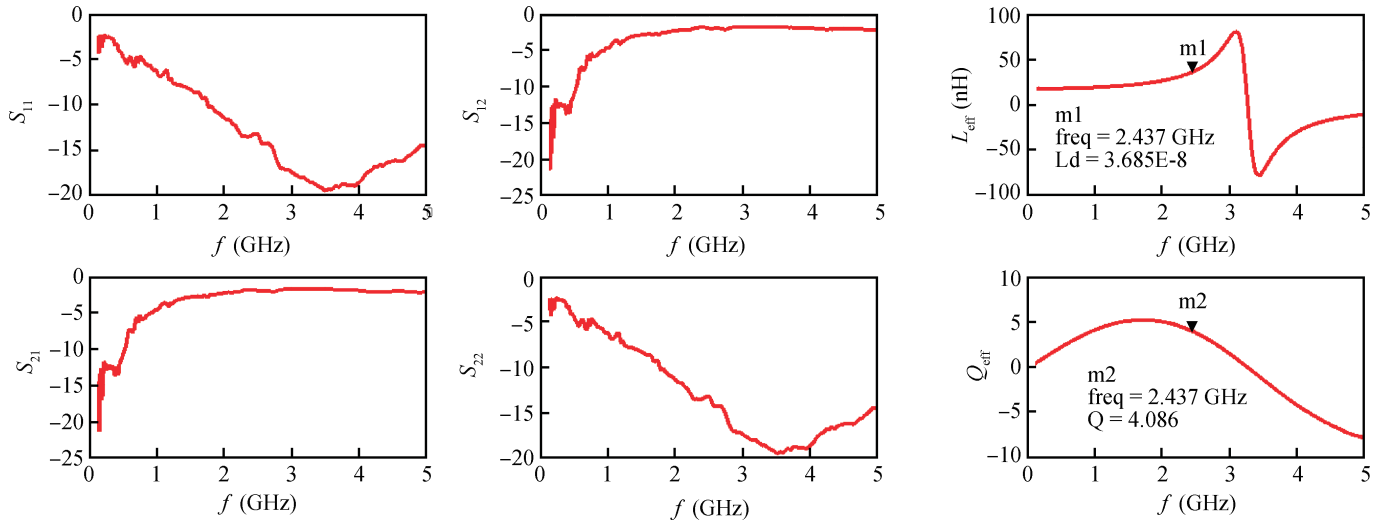


Fig. 8. S-parameters, L_{eff} and Q_{eff} test curve of the inductor.

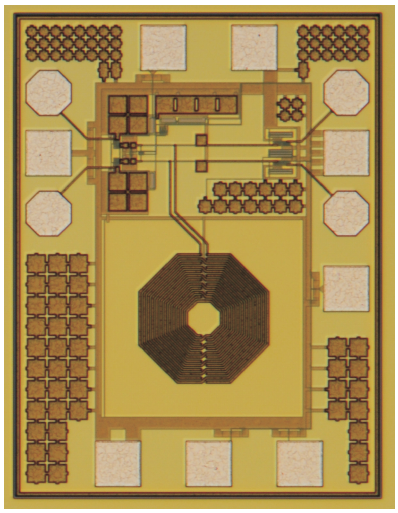


Fig. 9. Chip micro photo of the LNA.

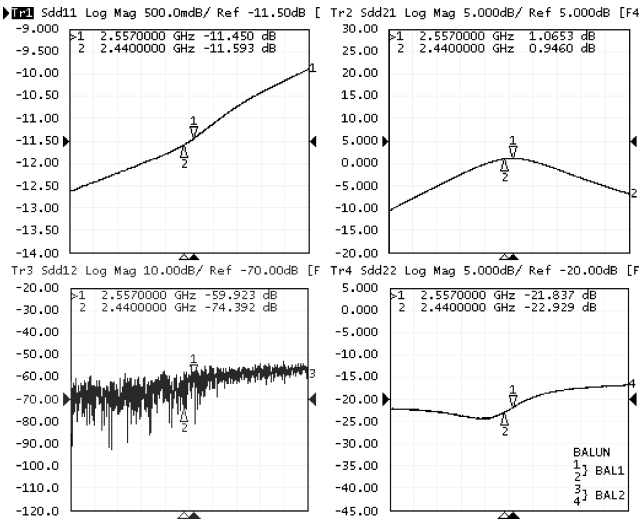


Fig. 11. S-parameter of the LNA at the low gain mode.

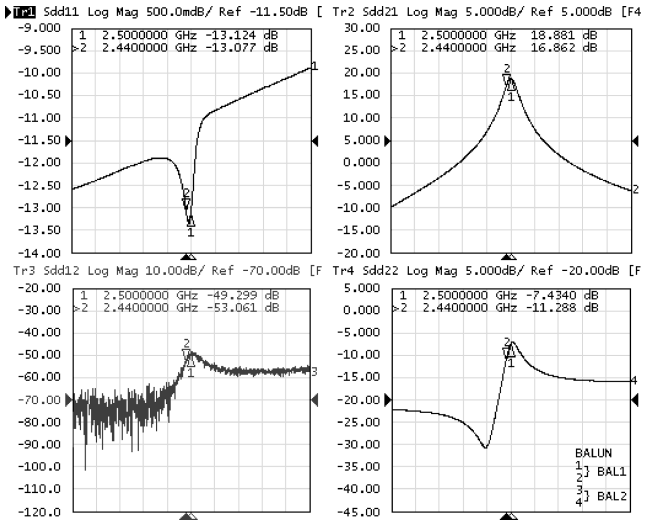


Fig. 10. S-parameter of the LNA at the high gain mode.

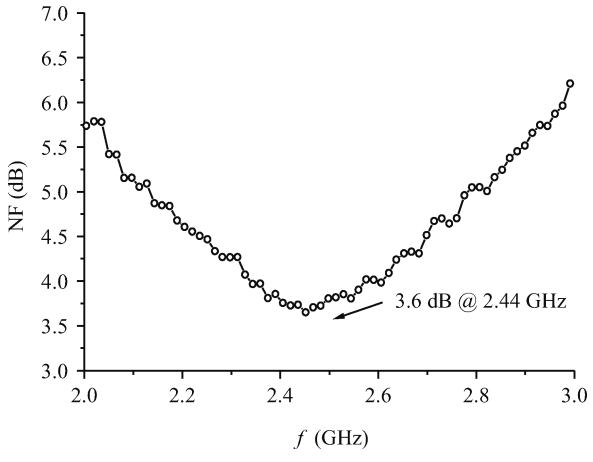


Fig. 12. Noise figure at high gain mode.

Table 3. Performance comparisons between recently published LNAs.

Parameter	Gain (dB)	NF (dB)	P_{dc} (mW)	P_{1dB} (dBm)	IIP3 (dBm)	Process (nm)	ESD	FOM_1 (dB/mW)	FOM_2 (mW^{-1})
Ref. [11]	12.9	3.9	14.4	Na	Na	180	no	0.89	0.21
Ref. [12]	9.4	2.5	3.42	Na	–7.6	180	no	2.75	1.11
Ref. [15]	14.1	1.6	7.2	Na	1.0	180	yes	1.96	1.57
Ref. [16]	20.0	3.9	22.6	Na	–11	130	no	0.88	0.30
Ref. [17]	15.2	1.7	5.6	Na	–10	180	yes	2.71	2.14
This work	16.8	3.6	2.16	–20	–10	180	yes	7.78	2.47

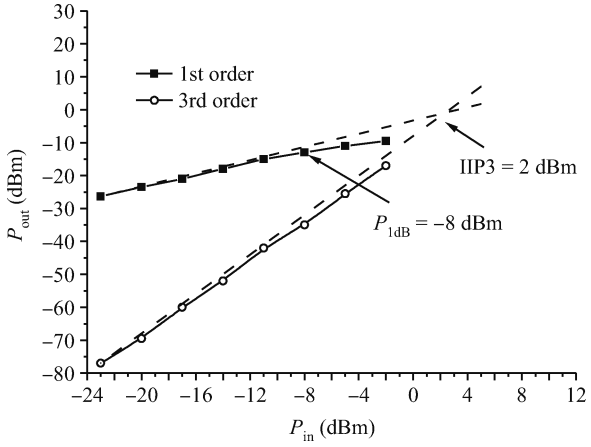


Fig. 8. IIP3 and P_{1dB} at low gain mode.

$$\mathrm{FOM_2[mW^{-1}]} = \frac{\mathrm{Gain[abs]}}{(\mathrm{NF}-1)[\mathrm{abs}]\cdot P_{\mathrm{dc}}[\mathrm{mW}]}. \qquad (9)$$

Table 3 gives the comparison results of the LNA and other designs. From Table 3 we can find that the FOM_1 and FOM_2 of the LNA are the best.

5. Conclusion

In this paper, a low power low noise amplifier for wireless sensor networks applications was presented. To reduce the LNA's power consumption and chip area, a two-stage cascaded cross-coupling common-gate topology and an internal new designed inductor were used to achieve the input and output matching. The LNA contained a gain control circuit and a frequency control circuit to adapt the deviations of process and the environments. The LNA shows 16.8 dB gain at high gain mode and 1 dB gain at low gain mode, respectively. It shows a 3.6 dB noise figure at high gain mode and −8 dBm input 1 dB compression point and 2 dBm IIP3 at low gain mode. It consumes 1.2 mA current from a 1.8 V DC supply. The power consumption of the LNA is very low and the performance of the LNA can be fully adapted to WSN system applications.

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