Design and optimization of a 0.5 V CMOS LNA for 2.4-GHz WSN application*

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Abstract: This paper presents a low noise amplifier (LNA), which could work at an ultra-low voltage of 0.5 V and was optimized for WSN application using 0.13 μm RF-CMOS technology. The circuit was analyzed and a new optimization method for a folded cascode LNA was introduced. Measured results of the proposed circuit demonstrated a power gain of 14.13 dB, consuming 3 mW DC power, showing 1.96 dB NF and an input 1-dB compression point of –19.9 dBm. Both input power matching (S_{11}) and output power matching (S_{22}) were below –10 dB. The results indicate that this LNA is fully applicable to low voltage and low power applications.

Key words: LNA; WSN; CMOS
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1. Introduction

One of the basic requirements is the receiver circuits' low voltage and low power application, because of the constraints of the Wireless Mobile Terminal's size, weight and cost, especially in wireless sensor network (WSN) application. The LNA is one of the most important and essential blocks in RF receivers[1]. Its performances under ultra-low voltage, such as noise figure and power gain, play a critical role[2].

This paper aims to reduce the LNA working voltage and power consumption while keeping its good performance. Based on this principle, a differential inductance degenerated folded cascode structure is adopted and analyzed in detail, including its input power matching condition, input noise matching condition, and the effect of the parasitic resistance of L_1, which resonates at the operating frequency with the parasitic capacitance of node A, as shown in Fig. 1, especially the voltage gain. There are several optimization methods used for conventional cascode LNAs, such as the PCSNIM proposed in Ref. [3], but they are not suitable for folded cascode LNAs. A folded cascode LNA should be optimized as two separate LNAs, and during the design of a folded cascode LNA, more factors need to be considered than during the design of a conventional one, such as the distribution of the current among M1 and M2, decreasing the losing factor η, and the bias voltage of M2. A new optimization method for a folded cascode structure is introduced in this paper.

The measured results of the chosen circuit demonstrated a power gain of 14.13 dB, consuming DC power of 3 mW at 0.5 V supply voltage, showing an NF of 1.96 dB and an input 1-dB compression point of –19.9 dBm. Both input matching (S_{11}) and output matching (S_{22}) are below –10 dB.

2. Analysis of the LNA circuit

The complete schematic of the proposed LNA is shown in Fig. 1. Due to the circuit's complete symmetry, only half of the circuit is taken for analysis. The half circuit and its small signal equivalent circuit are shown in Fig. 2. C_r is the parasitic capacitance from the drain terminal of M1 to the ground. C_t, L_{1eq} and R_{1eq} will be explained in the following.

2.1. Input power matching

The input impedance Z_{in1} is (neglect r_{DS1})

$$Z_{in1} = \frac{g_{m1}}{C_t} L_s + j\omega(L_s + L_g) + \frac{1}{j\omega C_t}, \tag{1}$$

where $C_t = C_{gs} + C_{ex}$. L_s generates the real part of Z_{in1}, while introducing little noise.

The input power matching conditions are as follows:

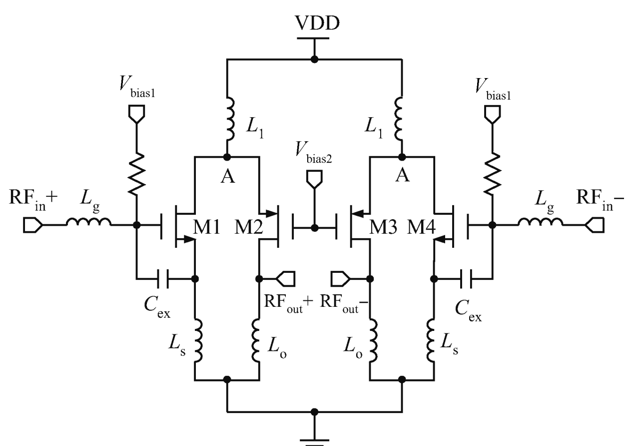

Fig. 1. Schematic of the proposed LNA circuit.

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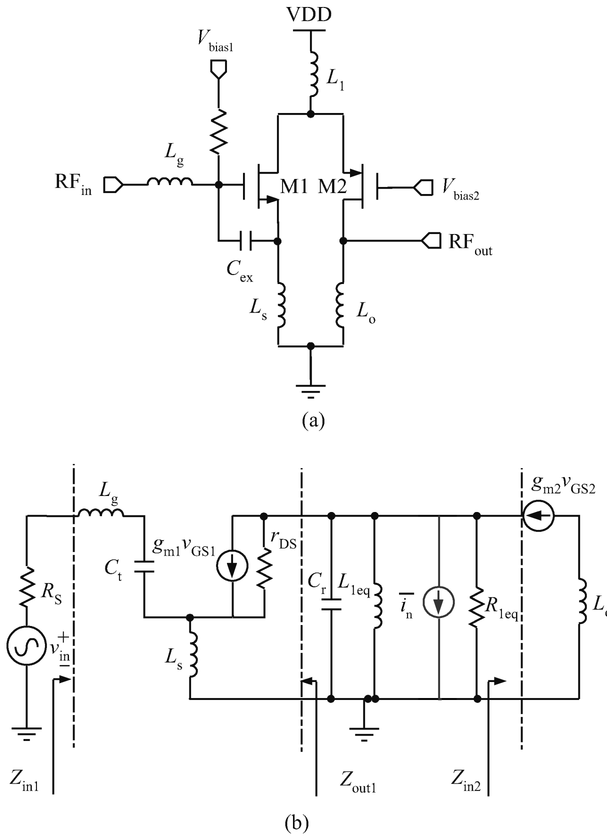

Fig. 2. (a) Half part circuit of the proposed LNA. (b) Its small signal equivalent circuit.

$$\begin{cases}\mathrm{Re}[Z_{\mathrm{in1}}] = \mathrm{Re}[Z_{\mathrm{s}}], \\ \mathrm{Im}[Z_{\mathrm{in1}}] = -\mathrm{Im}[Z_{\mathrm{s}}].\end{cases} \tag{2}$$

Typically, R_{s} is 50 Ω. Thus, the input power matching condition becomes:

$$\begin{cases}\mathrm{Re}[Z_{\mathrm{in1}}] = \mathrm{Re}[Z_{\mathrm{s}}] = 50\,\Omega, \\ \mathrm{Im}[Z_{\mathrm{in1}}] = -\mathrm{Im}[Z_{\mathrm{s}}] = 0\,\Omega.\end{cases} \tag{3}$$

Assign proper values to V_{gs}, L_{g}, L_{s}, and C_{ex} and C_{gs} (W) to make $L_{\mathrm{s}} + L_{\mathrm{g}}$ resonate with C_{t} at the operation frequency, and let

$$\frac{g_{\mathrm{m1}}}{C_{\mathrm{t}}} L_{\mathrm{s}} = R_{\mathrm{s}} = 50. \tag{4}$$

The input power matching will be achieved.

2.2. Effect of the parasitic resister of L_1

R_1 is the parasitic series resister of L_1. Through a series-parallel conversion shown in Fig. 3, the $L_{1\mathrm{eq}}$ and $R_{1\mathrm{eq}}$ is:

$$L_{1\mathrm{eq}} \approx L_1, \quad R_{1\mathrm{eq}} \approx R_1 Q^2 = R_1 \left(\frac{\omega L_1}{R_1}\right)^2 = \omega L_1 Q. \tag{5}$$

Q is the quality factor of L_1. In Eq. (5), the $R_{1\mathrm{eq}}$ varies proportionally to Q and L_1.

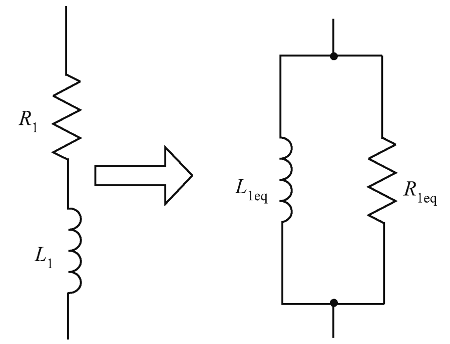

Fig. 3. Series-parallel conversion of L_1 and its parasitic resistance.

2.2.1. The current losing factor η

At the operation frequency, $L_{1\mathrm{eq}}$ and C_{r} achieve parallel resonance, and some current will be lost through the resister $R_{1\mathrm{eq}}$. The losing factor is defined as[3]:

$$\eta = \frac{Z_{\mathrm{in2}}}{Z_{\mathrm{in2}} + R_{1\mathrm{eq}}} = \frac{1/g_{\mathrm{m2}}}{1/g_{\mathrm{m2}} + R_{1\mathrm{eq}}} = \frac{1}{1 + \omega L_1 Q g_{\mathrm{m2}}}, \tag{6}$$

where $Z_{\mathrm{in2}} = \frac{1}{g_{\mathrm{m2}}}$.

Equation (6) reveals that large g_{m2} and Q can be chosen to minimize the lossy current.

2.2.2. Output noise current spectral density generated by $R_{1\mathrm{eq}}$

The noise current spectral density of $R_{1\mathrm{eq}}$ is

$$\overline{i_{\mathrm{n}}^2} = \frac{4kTB}{R_{1\mathrm{eq}}}. \tag{7}$$

Add this current source to the small signal equivalent circuit in Fig. 2(b), the output noise current spectral density $(\overline{i_{\mathrm{no}}^2})$ generated by $R_{1\mathrm{eq}}$ can be obtained:

$$\begin{aligned}\overline{i_{\mathrm{no}}^2} &= \overline{i_{\mathrm{n}}^2}\left(\frac{R_{1\mathrm{eq}} \| Z_{\mathrm{out1}}}{R_{1\mathrm{eq}} \| Z_{\mathrm{out1}} + Z_{\mathrm{in2}}}\right)^2 \\ &= \frac{4kTB}{R_{1\mathrm{eq}}}\left(\frac{1}{1 + Z_{\mathrm{in2}} Z_{\mathrm{out1}}^{-1} + Z_{\mathrm{in2}} R_{1\mathrm{eq}}^{-1}}\right)^2 \\ &= 4kTB \times \\ &\frac{1}{R_{1\mathrm{eq}}(1 + Z_{\mathrm{in2}} Z_{\mathrm{out1}}^{-1})^2 + Z_{\mathrm{in2}}^2 R_{1\mathrm{eq}}^{-1} + 2(Z_{\mathrm{in2}} + Z_{\mathrm{in2}}^2 Z_{\mathrm{out1}}^{-1})},\end{aligned} \tag{8}$$

where $Z_{\mathrm{out1}} \approx \frac{r_{\mathrm{DS}} R_{\mathrm{s}} + r_{\mathrm{DS}} L_{\mathrm{s}} g_{\mathrm{m1}}/C_{\mathrm{t}} + \omega^2 L_{\mathrm{s}}^2 + \mathrm{j}\omega L_{\mathrm{s}} R_{\mathrm{s}}}{R_{\mathrm{s}}}$.

As seen in Eq. (8), the output noise current density increases with $R_{1\mathrm{eq}}$ increasing at first, when

$$R_{1\mathrm{eq}} = \frac{Z_{\mathrm{in2}}}{1 + Z_{\mathrm{in2}} Z_{\mathrm{out1}}^{-1}} = Z_{\mathrm{in2}} \| Z_{\mathrm{out1}} ,$$

it gets the maximum value, and then, decreases with $R_{1\mathrm{eq}}$' increasing. Usually, $R_{1\mathrm{eq}}$ is larger than $Z_{\mathrm{in2}} /\!/ Z_{\mathrm{out1}}$, and in order to maximize $R_{1\mathrm{eq}}$, L_1's Q factor must be as large as possible.

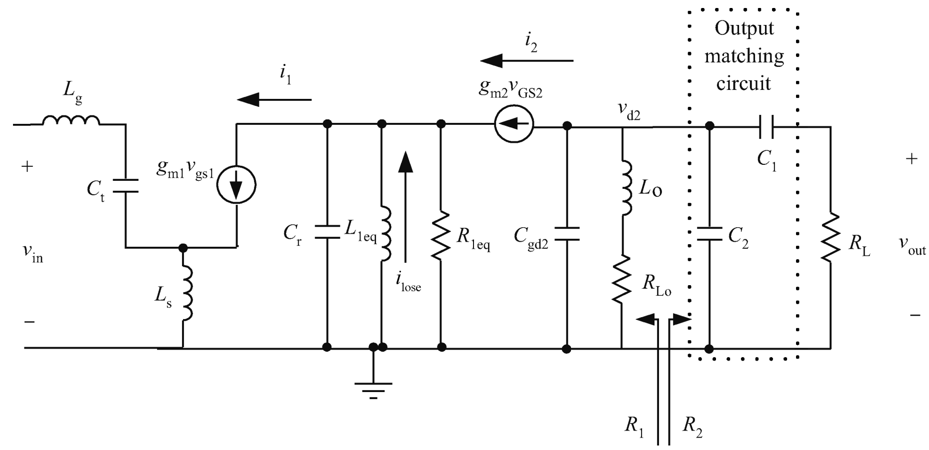

Fig. 4. Small signal equivalent circuit for voltage gain calculation.

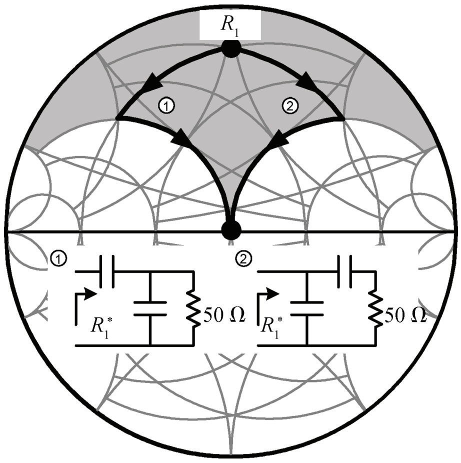

Fig. 5. Output power matching networks.

The output noise current density is inversely proportional to Z_{in2}, so a small g_{m2} is needed. This conclusion is contrary to the previous finding in the analysis of current losing factor η. As a result, the value of g_{m2} must be determined with a trade-off.

2.3. Voltage gain

The input resistance and load resistance have the same value, so the power gain is equal to the voltage gain, and then the voltage gain will be analyzed.

The small signal equivalent circuit for voltage gain calculation is shown in Fig. 4, C_{gd2} is the parasitic capacitance between the drain and gate of M2, R_{Lo} is the parasitic series resister of L_o. C_1 and C_2 form the output matching network, which is one of the two methods shown in Fig. 5, and R_L is the load resistor (usually it is 50 Ω).

In Fig. 4, it has been shown that

$$v_{out} = v_{d2}\frac{R_L}{R_L + 1/(SC_1)}, \tag{9}$$

and

$$v_{d2} = i_2(R_1 \| R_2) = i_1(1-\eta)(R_1 \| R_2). \tag{10}$$

Firstly, let i_1 be analyzed.

$$\begin{aligned} i_1 &= g_{m1}v_{gs1} = g_{m1}\frac{v_{in}}{R_{in}}\frac{1}{sC_t} \\ &= g_{m1}\frac{v_{in}}{\frac{g_{m1}}{C_t}L_s + s(L_s + L_g) + \frac{1}{sC_t}}\frac{1}{sC_t}, \end{aligned}$$

when the input power matching is achieved, $s(L_s + L_g) + 1/(sC_t) = 0$. Then

$$i_1 = g_{m1}\frac{v_{in}}{\frac{g_{m1}}{C_t}L_s}\frac{1}{sC_t} = \frac{v_{in}}{sL_s}. \tag{11}$$

It can be seen that i_1 is inversely proportional to the value of L_s, when the input power matching is achieved.

η has been discussed before, so $R_1 // R_2$ will be analyzed secondly. Given the output power matching requirement, R_1 and R_2 should satisfy the following relation:

$$R_1 = \overline{R_2}.$$

Assume that the output resistance of M2 is large enough so that it can be ignored. Through a series to parallel conversion, the equivalent circuit of $R_1 // R_2$ is shown in Fig. 6. C_{gd2}, C_2, C_1 and L_o resonate at the operating frequency to achieve the output power matching, besides,

$$\begin{aligned} &R_{Loeq} = R_{Leq}, \\ &R_{Leq} = R_L Q_L^2 = R_L\left[1 + \left(\frac{1}{\omega C_1 R_L}\right)^2\right]. \end{aligned} \tag{12}$$

Usually, it meets the requirements of industrial production standards that $S_{22} < -10$ dB.

$$S_{22} < -10\,\text{dB} \Rightarrow \left|\frac{R_{Loeq} - R_{Leq}}{R_{Loeq} + R_{Leq}}\right| < 0.316.$$

According to Eq. (12), a value range of C_1 can be obtained:

$$\begin{aligned} &\frac{1}{\sqrt{1.92(R_{Loeq} - R_L)R_L\omega^2}} < C_1 \\ &\qquad < \frac{1}{\sqrt{0.52(R_{Loeq} - R_L)R_L\omega^2}}. \end{aligned} \tag{13}$$

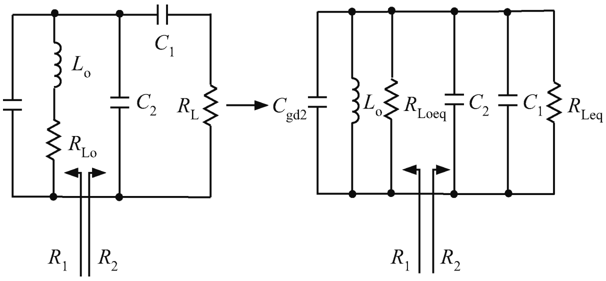

Fig. 6. Series to parallel conversion of R_1 and R_2.

Let C_1 be analyzed.

According to Eqs. (9) and (10),

$$\begin{aligned} v_{d2} &= i_2(R_1 \| R_2) = i_2(R_{Loeq} \| R_{Leq}) \\ &= i_2 \frac{R_{Loeq}R_{Leq}}{R_{Loeq}+R_{Leq}} \\ &= i_2 \frac{R_{Loeq}R_L + R_{Loeq}R_L\left(\dfrac{1}{\omega C_1 R_L}\right)^2}{R_{Loeq}+R_L+R_L\left(\dfrac{1}{\omega C_1 R_L}\right)^2} \\ &= i_2 \frac{R_{Loeq}R_L + R_{Loeq}\dfrac{1}{\omega^2 C_1^2 R_L}}{R_{Loeq}+R_L+\dfrac{1}{\omega^2 C_1^2 R_L}} \\ &= i_2 \frac{R_{Loeq}R_L^2\omega^2C_1^2 + R_{Loeq}}{(R_{Loeq}+R_L)\omega^2C_1^2R_L+1}, \end{aligned} \tag{14}$$

$$\begin{aligned} |v_{out}| &= \left| v_{d2}\frac{R_L}{R_L + 1/(SC_1)} \right| \\ &= |v_{d2}| \frac{R_L \omega C_1}{\sqrt{1+(R_L\omega C_1)^2}} \\ &= i_2 \frac{R_{Loeq}R_L^2\omega^2C_1^2 + R_{Loeq}}{(R_{Loeq}+R_L)\omega^2C_1^2R_L+1}\frac{R_L \omega C_1}{\sqrt{1+(R_L\omega C_1)^2}}. \end{aligned} \tag{15}$$

The derivative of v_{out} with respect to R_{Loeq} is

$$\begin{aligned} \frac{\partial |v_{out}|}{\partial R_{Loeq}} &= i_2 \frac{R_L\omega C_1}{\sqrt{1+(R_L\omega C_1)^2}} \frac{1}{R_{Loeq}\omega^2C_1^2R_L+1} \\ &\quad \times \left(1 - \frac{R_{Loeq}\omega^2C_1^2R_L}{R_{Loeq}\omega^2C_1^2R_L+1}\right) > 0. \end{aligned}$$

So, v_{out} varies proportionally to R_{Loeq}. A large R_{Loeq} requires a large L_o and a large Q factor.

Let

$$\frac{\partial |v_{out}|}{\partial C_1} = 0,$$

it can be obtained that

$$C_1 = \frac{1}{\sqrt{(R_{Loeq}-R_L)R_L\omega^2}} \quad \text{or } C_1 = +\infty.$$

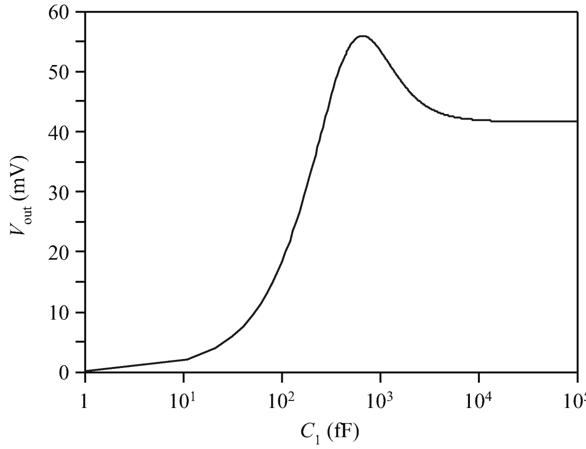

Fig. 7. v_{out} versus R_{Loeq} ($R_{Loeq} = 250\ \Omega$, $R_L = 50\ \Omega$, Freq = 2.4 GHz, $i_2 = 1$ mA).

V_{out} get its maximum value when

$$C_1 = \frac{1}{\sqrt{(R_{Loeq}-R_L)R_L\omega^2}}. \tag{16}$$

And this value is in the range of Eq. (13). A curve of v_{out} versus C_1 is shown in Fig. 7, and $R_{Loeq} = 250\ \Omega$, $R_L = 50\ \Omega$, Freq = 2.4 GHz.

According to the analysis above, there are four methods used to increase the voltage gain. The first one is decreasing the value of L_s. The second one is decreasing η. The third one is increasing R_{Loeq}, and the last one is assigning C_1's value according to Eq. (16).

2.4. Noise matching

In order to achieve noise matching, the following equation must be satisfied.

$$\begin{cases} \mathrm{Re}[Z_{opt}] = \mathrm{Re}[Z_s], \\ \mathrm{Im}[Z_{opt}] = \mathrm{Im}[Z_s]. \end{cases} \tag{17}$$

Usually large C_{gs} is needed to satisfy Eq. (17), and this leads to a large gate width and high power consumption. In order to solve this problem, C_{ex} is added. According to the noise analysis in Ref. [4], Z_{opt} can be obtained:

$$Z_{opt} = \frac{\alpha\sqrt{\dfrac{\delta}{5\gamma(1-|c|^2)}} + j(\dfrac{C_t}{C_{gs}} + \alpha|c|\sqrt{\dfrac{\delta}{5\gamma}})}{\omega C_{gs}\left\{\dfrac{\alpha^2\delta}{5\gamma(1-|c|^2)} + (\dfrac{C_t}{C_{gs}} + \alpha|c|\sqrt{\dfrac{\delta}{5\gamma}})^2\right\}} - sL_s. \tag{18}$$

Proper values of V_{gs}, L_g, L_s, C_{ex} and C_{gs} (W) can be assigned to achieve noise matching and input power matching simultaneously, because there are four equations in Eq. (2) and Eq. (17) with five unknowns.

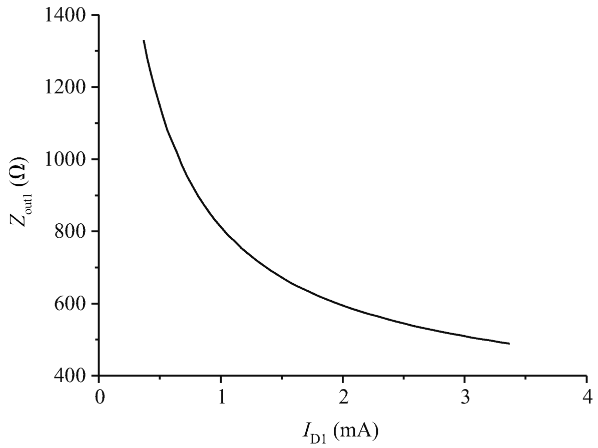

Fig. 8. The curve of Z_{out1} versus I_{D1}.

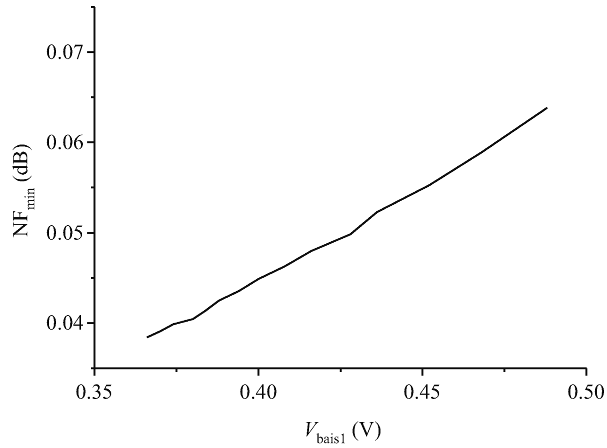

Fig. 9. Determine V_{bias} and W of M1.

3. New optimization method and measured results

There are several optimization methods used for conversional cascode LNAs, but they are not suitable for the folded cascode LNA. This is because during the design of a folded cascode LNA, more factors need to be considered than during the design of a conversional one, such as the distribution of the current among M1 and M2, decreasing the losing factor η, the bias voltage of M2, and so on. Therefore, a new optimization method a for folded cascode LNA is proposed in this paper.

3.1. Circuit optimization method

The proposed LNA was designed with 0.13 μm RF CMOS technology, and L_{s} and L_{o} are on-chip spiral inductors. L_1 consists of the bonding wire inductor connecting the chip pad and the PCB and the SMT inductor on the PCB, because of their high Q factor can reduce the noise figure and current losing factor η according to Eq. (6) and Eq. (8). L_{g} is also an off-chip inductor. The circuit is optimized to achieve power-constrained simultaneous noise and input matching, and the steps are as follows:

Step 1: Determine the distribution of the current among M1 and M2. In this design, the DC current of the single-ended LNA is 3 mA. The distribution is determined by the principle of reducing η. Two factors need to be considered. One is the parasitic resister of L_1, and the other is the output resister of M1, Z_{out1}. Z_{out1} was ignored before in order to simplify the analysis, but in practice, this factor cannot be ignored. To guarantee most of the current flows into M2, it is required that

$$Z_{\text{in2}} = \frac{1}{g_{\text{m2}}} = \frac{|V_{\text{GSM2}} - V_{\text{thM2}}|}{2I_{\text{D2}}} < 0.1\left(R_{\text{1eq}} \parallel Z_{\text{out1}}\right). \quad (19)$$

Off-chip L_1 is chosen to maximize R_{1eq}, which can achieve several kilo ohms R_{1eq} easily. If a fully integrated LNA is designed, an on-chip inductor will be adopted. As a result of the poor Q factor of the on-chip inductor, it will be difficult to realize an R_{1eq} more than 500 Ω. The curve of Z_{out1} versus I_{D1} is shown in Fig. 8. Because M1 is the major stage of an LNA, more current is assigned to M1 than to M2. For instance, I_{D1} is 2 mA, and I_{D2} is 1 mA. In addition, the distribution should meet Eq. (19). According to Fig. 8, the output resister is about 580 Ω when I_{D1} is 2 mA. With an off-chip inductor, R_{1eq} is about several kΩ, so R_{1eq} // Z_{out1} is about 580 Ω. According to Eq. (19), it can be obtained that

$$I_{\text{D2}} > \frac{|V_{\text{GSM2}} - V_{\text{thM2}}|}{2 \times 58} = 0.86 \text{ mA},$$

with $|V_{\text{GSM2}} - V_{\text{thM2}}| = 100$ mV.

Thus, it is a proper choice that $I_{\text{D1}} = 2$ mA, $I_{\text{D2}} = 1$ mA.

Step 2: Determine the DC-bias V_{bias1} and the width W of M1 to provide the minimum NFmin. With constant I_{D1}, if V_{bias1} is determined, W is also determined. According to the method proposed in Ref. [5], a curve of NFmin versus V_{bias1} with constant I_{D1} consumption can be obtained, and it is shown in Fig. 9. In this figure, it can be seen that NFmin changes inversely with V_{bias1}'s change. But the threshold voltage V_{th} is larger than 300 mV, if $V_{\text{bias1}} < 400$ mV, the overdrive voltage of M1 will be smaller than 100 mV, the process variation will affect the circuit performance greatly. So, it is suitable to make the overdrive voltage slightly larger than 100 mV, and in this design, $V_{\text{bias1}} = 420$ mV and $W = 40$ μm is chosen.

Step 3: Set L_{g}'s parasitic resistance (R_{Lg}) and L_{s}. Im[Z_{opt}] of the circuit can be seen as an approximate value of L_{g}. According to bond inductor's quality factor (about 50 at 2.4 GHz), a rough value of R_{Lg} can be obtained, and it will be adjusted in Step 6. Set the initial value of L_{s} to a value that is not too large, for example 1 nH, and it will be tuned in Step 4. A large L_{s} will reduce the power gain and worsen the noise performance.

Step 4: Set the value of L_{g} to 0. Tune C_{ex} and L_{s} to satisfy the equation: Re[Z_{opt}] = Re[Z_{in}] = 50 Ω. This is a process of trial and error.

Step 5: Calculate the value of L_{g} according to simulated Im[Z_{opt}]. After setting L_{g} to that value, Im[Z_{opt}] will change downward along the 50 Ω circle, while Im[Z_{in}] will change in the opposite direction. They will meet at the origin, because the imaginary parts of Z_{opt} and Z_{in} are almost equal.

Step 6: Calculate L_{g}'s parasitic resistance according to its quality factor, and set it to that value.

Step 7: Go back to Step 4, until the input power matching and noise matching can be achieved simultaneously through fine tuning of L_{g}.

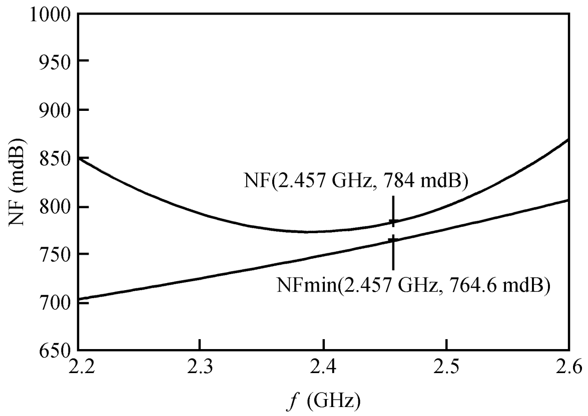

Fig. 10. The NF and NFmin of designed LNA.

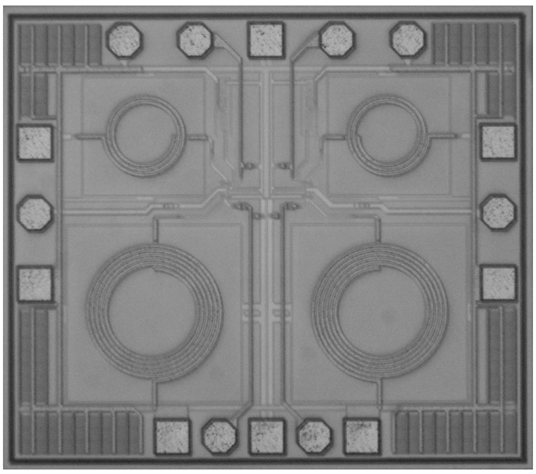

Fig. 11. Microphotograph of the proposed LNA.

Step 8: If Step 7 cannot be achieved, make a small tuning of $V_{\rm bias}$ and W, and then redo Steps 4 to 7.

Step 9: Choose the DC-bias voltage $V_{\rm bias2}$ and width W_2 of M2. Usually $V_{\rm bias2}$ is chosen to be 0 V. At constant current $I_{\rm D2}$, a large overdrive voltage leads to a small $g_{\rm m2}$ (Eq. (19)), which helps to decrease the output noise current density generated by L_1's parasitic resister according to Eq. (8). If the LNA is designed for large gain, $V_{\rm bias2}$ can be increased to get a large $g_{\rm m2}$, and thereby obtain a large gain. In this design, the LNA is designed for a low noise figure, so $V_{\rm bias2} = 0$ V is chosen. According to 1 mA $I_{\rm D2}$, W_2 can be obtained.

Step 10: Tune the value of L_1 to get the maximum gain.

Step 11: Choose proper output power matching network according to R_1.

Figure 10 shows the noise figure, NF, and the minimum noise figure, NFmin. NF is only 18 mdB larger than NFmin. Noise matching is achieved. Figure 11 shows a microphotograph of the LNA. The circuit with pads occupies an area of $915 \times 1054\ \mu{\rm m}^2$.

3.2. Measured results

In Fig. 12, it can be obtained that the input matching S_{11} is below –10 dB from 2.4 to 2.4835 GHz. It also can be seen that the output matching S_{22} is below –10 dB. Output matching is also achieved.

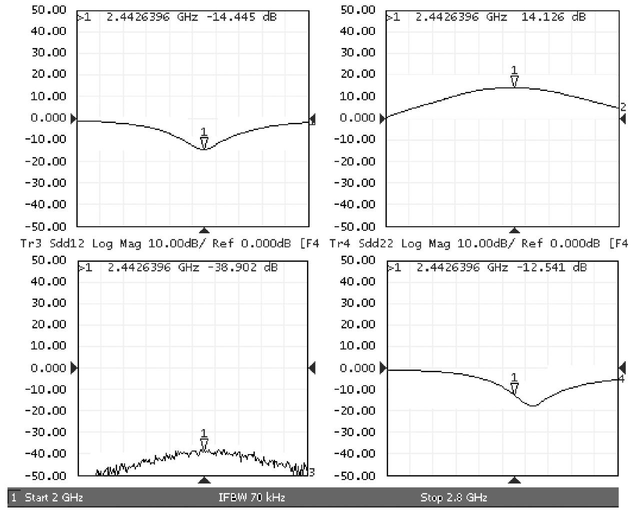

Fig. 12. Measured S-parameter.

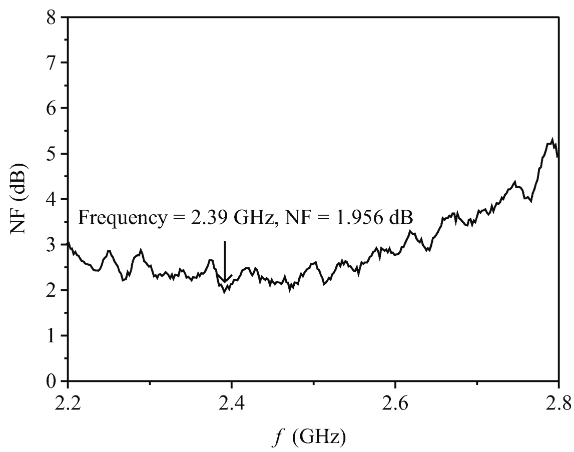

Fig. 13. Measured noise figure.

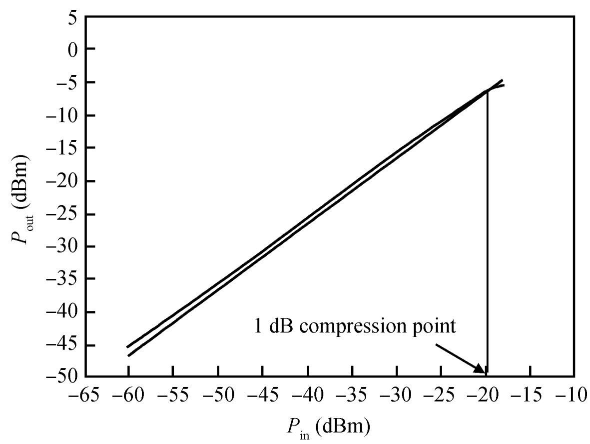

Fig. 14. Input 1-dB compression point of the LNA.

The power gain and the reverse isolation are shown in Fig. 12. The maximum power gain is 14.12 dB @ 2.442 GHz, and the reverse isolation is below –38.9 dB.

Figure 13 shows the noise figure of the proposed LNA. It can be seen that the minimum value is 1.96 dB and the maximum one is 2.53 dB, NF in most of frequency range is below

Table 1. Performances comparison of low voltage and low power.

Parameter	Gain (dB)	NF (dB)	P_{1dB} (dBm)	Freq (GHz)	P_{DC}* (mW)	V_{DD} (V)	FOM
Ref. [6]	15	2	–14	2.4	12	1	0.43
Ref. [7]	9.2	4.5	–27	5	0.9	0.6	0.05
Ref. [8]	10.3	5.3	–22	5.1	1.03	0.4	0.14
Ref. [9]	10	3.37	–18	5.2	1.08	0.6	0.57
This work	14.13	2	–19.9	2.4	1.5	0.5	0.72

* P_{DC} of single-ended topology.

2.3 dB.

Figure 14 shows the input 1-dB compression point, which is –19.9 dBm.

To compare the overall performances of the proposed LNA with the previous published very low voltage LNA shown in Table 1, we have used the figure of merit (FOM) given in Eq. (11), which includes the effect of amplifier gain, noise figure, linearity (P_{1dB}), operation frequency, and DC power consumption (PDC). This LNA has the best overall figure of merit (FOM) among recently published low power CMOS LNAs.

$$\text{FOM[GHz]} = \frac{\text{GAIN(abs)}\, P_{1dB}(\text{mW})\text{Freq(GHz)}}{(\text{NF}-1)(\text{abs})\, P_{DC}(\text{mW})}. \quad (20)$$

4. Conclusion

The half part of the proposed LNA structure is analyzed in this paper, including input power matching, the effect of L_1's parasitic resistance and noise matching. In addition, a new optimization technology for the folded cascode LNA is also given. The LNA achieves good performance at an ultra-low voltage of 0.5 V, consuming a DC power of 3 mW, showing a power gain of 14.13 dB and 1.96 dB NF. The performances of the proposed LNA are suitable for WSN applications.

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