A novel low ripple charge pump with a 2X/1.5X booster for PCM*

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Abstract: A low ripple switched capacitor charge pump applicable to phase change memory (PCM) is presented. For high power efficiency, the selected charge pump topology can automatically change the power conversion ratio between 2X/1.5X modes with the input voltage. For a low output ripple, a novel operation mode is used. Compared with the conventional switched capacitor charge pump, the flying capacitor of the proposed charge pump is charged to $V_o - V_{in}$ during the charge phase (V_o is the prospective output voltage). In the discharge phase, the flying capacitor is placed in series with the V_{in} to transfer energy to the output, so the output voltage is regulated at V_o. A simulation was implemented for a DC input range of 1.6–2.1 V in on SMIC standard 40 nm CMOS process, the result shows that the new operation mode could regulate the output of about 2.5 V with a load condition from 0 to 10 mA, and the ripple voltage is lower than 4 mV. The maximum power efficiency reaches 91%.

Key words: charge pump; DC to DC converter; PCM drivers; low ripple; power efficiency
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1. Introduction

The operation of phase change memory (PCM) requires a write voltage up to 2–3 V at 0.2–2 mA to reset the PCM cell, the charge pump appears as a very important block of PCM with a low input voltage[1]. The conventional switched capacitor regulated charge pump with pulse skipping modulation is hard to realize a low ripple output, due to the charge redistribution when the flying capacitor is connected to the output capacitor, which could influence the stability of the PCM programming and reduce the power efficiency of the charge pump[2].

Current consumption of the PCM with an 8-bit-parallelism scheme can vary from 0 to 10 mA in 1 μs when programming. Although the regulated charge pump with pulse width modulation has a low output ripple, the slow transient response is not suitable for PCM programming[3, 4].

An SC voltage doubler with pseudo-continuous output regulation using a three-stage switchable Opamp has been proposed for a fast transient response and a low ripple, but a complex pole-zero compensation circuit is needed to make it stable in different load conditions[5].

In this paper, the proposed charge pump uses a novel method to regulate the output voltage for a low output ripple, high power efficiency and fast transient response. It provides a maximum 10 mA load current and 2.5 V output with an input voltage range of 1.6–2.1 V as the power supply of the PCM programming driver. The new charge pump also can be used to overdrive the gate voltage of the NMOS selector in the PCM array up to 2.5 V for a higher saturation current, resulting in a lower memory array area cost.

1.1. Major factors for the output ripple

The typical switched capacitor charge pump is shown in Fig. 1. It has two steps in a complete operating cycle. In the charge phase, C_f is charged to V_{in}. In the discharge phase, the flying capacitor is placed in series with V_{in} to transfer energy to the output. The large output ripple caused by charge redistribution is hard to eliminate, which can be calculated as:

$$V_{ripple\_p} \cong \frac{(2V_{in} - V_{out})C_f}{C_{out} + C_f}. \quad (1)$$

The output ripple caused by load current can be written as:

$$V_{ripple\_n} \cong \frac{I_{load}T}{C_{out}}, \quad (2)$$

where I_{load} is the output current, and T is the operation period of the charge pump. For $I_{load} = 10$ mA, $T = 1$ μs, $C_f = 0.3$ μF, $C_{out} = 3$ μF, $V_{in} = 1.6$ V and $V_{out} = 2.5$ V, V_{ripple_p} is about

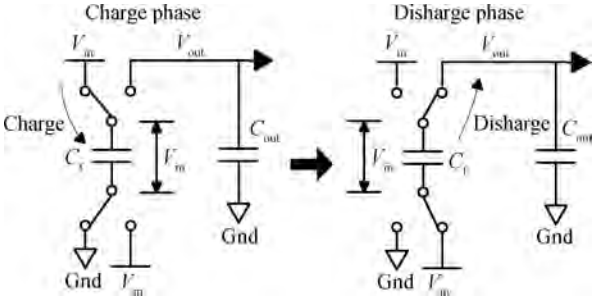

Fig. 1. The two operation steps of typical charge pump.

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Table 1. Operation timing of the booster.

Mode	Switched on phase of the MOSFETs and TG							
	M1	M2	M3	M4	M5	M6	M7	TG
2X	off	off	off	clk2	clk1	clk2	vc7 = 0	off
1.5X	clk1	clk2	clk2	clk2	off	clk2	vc7 = 0	clk1

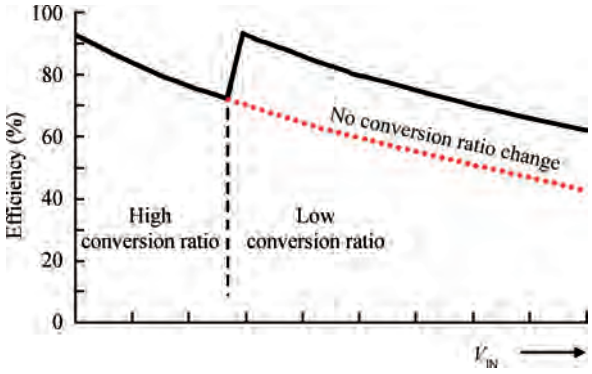

Fig. 2. Efficiency versus V_{in} for a fixed output voltage switched capacitor charge pump with different conversion rations.

60 mV, V_{ripple_n} is only 3 mV. The output ripple is dominated by the charge redistribution.

1.2. Power efficiency

The efficiency of a fixed output voltage charge pump with a conversion ratio of M can be written as:

$$\text{Efficiency} \cong \frac{V_{out}}{V_{in}M}. \tag{3}$$

Figure 2 shows the efficiency versus V_{in} for a fixed output voltage switched capacitor charge pump with different conversion ratios. With a fixed conversion ratio the efficiency will decrease like the $1/x$ function indicated with a dotted line[6, 7].

A switched capacitor charge pump topology with an automatic conversion ratio could get high power efficiency over a wide input voltage range.

2. Design of the proposed charge pump

2.1. Topology and operation mode of the booster

Figure 3 shows the booster of the proposed charge pump, which operates in a novel mode to regulate the output voltage and reduce the output ripple. M1–M7 and TG are controlled by non-overlapping clocks clk1 and clk2. In the 2X mode, V_{pump} is set to $V_o - V_{in}$. During the charge phase, clk1 = 1, clk2 = 0, M5 and M7 are both switched on, the other MOSFETs and TG are switched off, C_{f2} is charged at the beginning, if the net c2p is higher than the reference voltage V_{pump}, M7 will be switched off by the voltage comparator COMP. During the discharge phase, clk1 = 0, clk2 = 1, M4 and M6 are both switched on, the other MOSFETs and TG are switched off, the net c2n is connected to V_{in}, so the net c2p is pushed to V_o, the charge transfer from C_{f2} to C_{out}, and after several operation cycles, the output voltage is regulated at Vo. In the 1.5X mode, V_{pump} is set to $2(V_o - V_{in})$, during the charge phase, clk1 = 1, clk2 = 0, M1, M7 and TG are switched on, the other MOSFETs are switched off, C_{f1} and C_{f2} are charged at the beginning, if the net c2p is higher than the reference voltage V_{pump}, M7 will be switched off by the voltage comparator COMP, both C_{f1} and C_{f2} are charged to $V_o - V_{in}$. During the discharge phase, clk1 = 0, clk2 = 1, M2, M3, M4 and M6 are switched on, the other MOSFETs and TG are switched off, net c1n and c2n are connected to V_{in}, so net c1p and c2p are pushed to V_o, the charge transfer from C_{f1} and C_{f2} to Cout, and after several operation cycles, the output voltage is regulated at V_o. V_o is the prospective output voltage in this design which is set to 2.5 V. The booster operates according to Table 1.

Compared with the conventional switched capacitor charge pump, the flying capacitors of the proposed charge pump are only charged to $V_o - V_{in}$ during the charge phase, which could reduce the influence of the charge redistribution on the output ripple.

Level shifters convert the high voltage of signals to VH which is the higher voltage between V_{in} and V_{out}, so PMOS M3, M4, M6 and M7 could be completely switched off.

2.2. Reference voltage V_{pump}

The reference voltage V_{pump} is generated by a band-gap, several resistances and amplifiers. However, we find that V_{out} decreases as the load current increases due to the internal resistance of the charge pump. So we add a correction factor $K(V_{out} - V_o)$ to V_{pump}. As shown in Fig. 4, the resistance of the V_{pump} generator is given as:

$$\frac{V_o}{V_{bg}} = n, \tag{4}$$

$$\frac{R_1}{R_0} = K, \tag{5}$$

$$\frac{R_3}{R_0} = \frac{K}{(n-1)(K+1)}, \tag{6}$$

$$\frac{R_4 + R_5 + R_6}{R_5} = \frac{2R_1}{R_3}, \tag{7}$$

$$R_5 = R_6, \tag{8}$$

where V_{bg} is a bandgap reference voltage of about 1.25 V. In 2X mode, Mode = 1, TG_2X is switched on and TG_1.5X is switched off, $V_{pump} = V_o - V_{in} + K(V_o - V_{out})$. In 1.5X mode, Mode = 0, TG_1.5X is switched on and TG_2X is switched off, $V_{pump} = 2(V_o - V_{in}) + 2K(V_o - V_{out})$. In this design, K = 5.

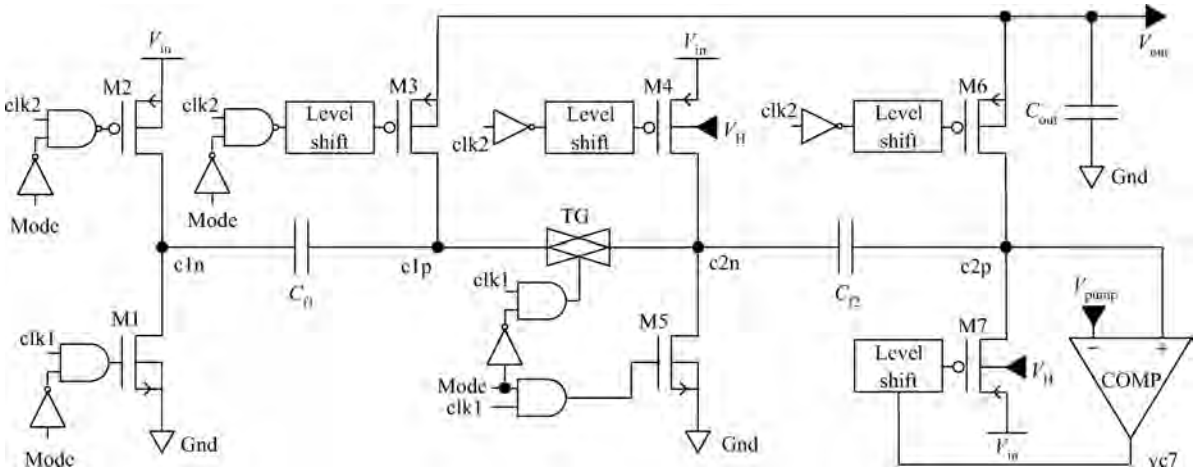

Fig. 3. The proposed charge pump is composed of $V_o - V_{DD}$ reference voltage generator, bulk bias selector, non-overlapping clock generator, hysteresis comparator and a conventional booster.

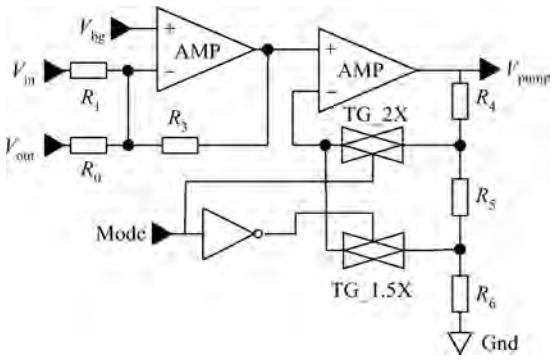

Fig. 4. Reference voltage V_{pump} generator.

2.3. Bulk bias

The input voltage ranges from 1.6 to 2.1 V, and the output voltage ranges from 0 (star up) to 2.5 V, so a bulk bias circuit is needed to prevent latch-up by tying the bulk to the highest supply, which is shown in Fig. 5. When V_{out} is higher than V_{in}, co $= 1$, V_H is connected to V_{out} by M5, otherwise V_H is connected to V_{in} by M6 ($W_2/L_2 = mW_1/L_1$, $W_4/L_4 = mW_3/L_3$). The level shifter ensures the M6 can be completely switched off to reduce the current flowing from V_{out} to V_{in}, when Vout is higher than V_{in}. The resistance in series with the bulk of M5 and M6 limits the pnp base current in the event that the bulk node is inadvertently forward biased because of the slow comparator response time in a fast event such as a short. Compared with the traditional power switch circuit, this design reduces the chip area and the power cost, because it doesn't need any amplifiers or voltage dividers[8].

2.4. Non-overlapping clock

Figure 6 shows the two phase non-overlapping clock generator, which controls M1–M7 and TG of the booster. CLK is 1 MHz clock signal. When the PCM is in the read state or stand by, EN $= 0$, net Q is connected to input D of the D flip flop by the mux, clk1 and clk2 maintain the original state, so the charge pump is hung up. When the PCM is programming, EN $= 1$, the net Q_ is connected to the input D of the D flip flop by the mux, clk1 and clk2 output the two phase non-overlapping clock, and the booster begins to work.

2.5. Voltage comparator COMP

For the stability of the booster, COMP should be a hysteresis voltage comparator to prevent M7 of the booster switching repeatedly during the charge phase. However, it is hard to accurately control the threshold voltage of a hysteresis voltage comparator.

In this design we used a rail-to-rail amplifier and a D flip-flop to ensure that M7 is switched on only once in the charge phase as shown in Fig. 7.

During the discharge phase clk1 $= 0$, so vc7 $= 1$, M7 is switched off, and Q of the D flip-flop is set at "1".

At the beginning of the charge phase, if c2p is lower than the V_{pump}, the amplifier outputs a low voltage, clk1 $= 1$, Q $= 1$, vc7 $= 0$, M7 is switched on, and there is a charge transfer from V_{in} to c2p. When c2p is higher than V_{pump}, the rising edge of the amplifier output sets at Q $= 0$, so vc7 $= 1$, M7 is switched off. During the same charge phase, if the voltage of c2p drops lower than V_{pump} due to the leak current, M7 will not be switched on again, until the next charge phase.

If c2p is higher than V_{pump} at the beginning of the charge phase, the amplifier output high voltage, vc7 $= 1$, and M7 is switched off. During the same charge phase, if the voltage drops lower than V_{pump}, M7 will be switched on until c2p is higher than V_{pump} again, but only once.

2.6. Power conversion ratio control

We set V_o at 2.5 V for PCM programming, with an input voltage range of 1.6–2.1 V, and with a 2X conversion ratio to meet the requirements. However, as the input is normally at 1.8 V, the maximum theoretical efficiency is only 69% in 2X mode, but is 92% in 1.5X mode. So the booster is designed in 2X mode with an input range from 1.6 to 1.76 V and 1.5X in mode with an input range from 1.72 to 2.1 V. Both the 1.5X and 2X modes could work in the hysteresis gap of 1.72–1.76 V, which always guarantees a stable operation.

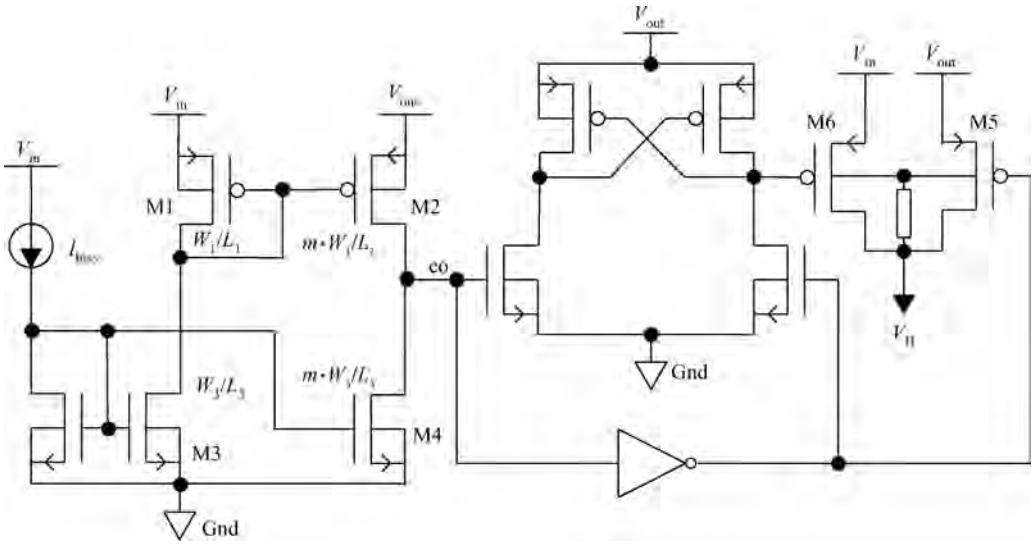

Fig. 5. Comparator circuit to bias bulk voltages at the higher of the input or output voltage.

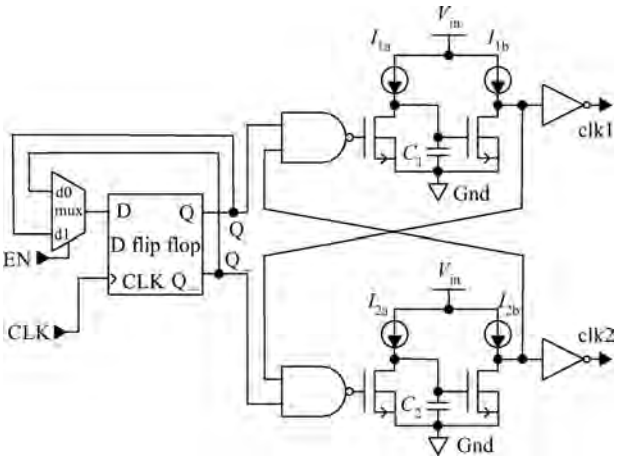

Fig. 6. Two phase non-overlapping clock generator.

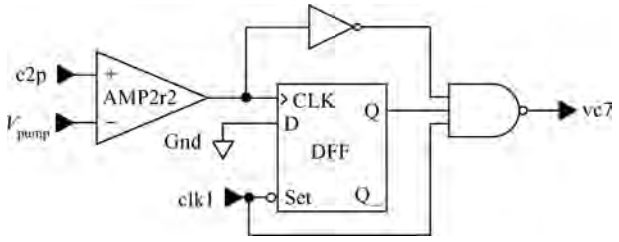

Fig. 7. Voltage comparator COMP.

This charge pump also has a 1 MHz fixed-frequency oscillator, an overheat protection circuit and a soft start circuit in it. The scheme of the charge pump is shown in Fig. 8.

2.7. Transient response

Although the PWM charge pump has a low output ripple, due to the internal oscillator, it needs a few clock cycles to stabilize it when the load current changes, that means the output voltage has a longer recovery time, especially as the load changes from empty to heavy conditions[4].

Under the light load conditions, the reference voltage V_{pump} of the proposed charge pump approximately equals $V_{in} - V_o$ in 2X mode, and $2(V_{in} - V_o)$ in 1.5X mode. Independent of the load current, in the charge phase, C_{f1} or C_{f2} is always charged to $V_{in} - V_o$, and in the discharge phase, c1p or c2p will be pushed to V_o.

Under the heavy load conditions, V_{pump} will vary with V_{out} immediately when the load current changes，and in the following charge phase C_{f1} or C_{f2} will be charged as V_{pump} adjusts, the recovery time is only one or two clock cycles.

Therefore, the new charge pump has a faster transient response with the load current changing at different load conditions.

3. Simulation results

The proposed charge pump was designed and simulated with an SMIC 40 nm CMOS process, only thick oxide 1.8 V MOSFETs were used, which could be overdriven to 2.5 V. Figure 9 shows the layout, the total area of the test chip is 900 × 900 μm^2, and the core size is only 250 × 250 μm^2.

The flying capacitors are both 0.3 μF, and the output capacitor is 3 μF, which are external capacitors for high power efficiency[9]. The charge pump can provide a 10 mA maximum load current and a 2.5 V regulated output voltage with an input voltage range of 1.6–2.1 V.

Figure 10 shows a transient response of V_{out} with different load currents at a supply voltage of 1.8 V from Spectre simulations. The mean voltage of the output decreased to 11 mV with the load current increasing from 0 to 10 mA, due to the internal resistance of the charge pump. A larger factor K could reduce the variation of V_{out}, but more chip area will be cost by the resistive divider of the reference voltage V_{pump} generator.

The output ripple and efficiencies with different load currents and supply voltages are shown in Table 2. In contrast, we removed the COMP module from the booster of Fig. 3, using pulse skipping modulation to regulate V_{out}. The simulation results with the same C_{f1}, C_{f2} and C_{out} are shown in Table 3.

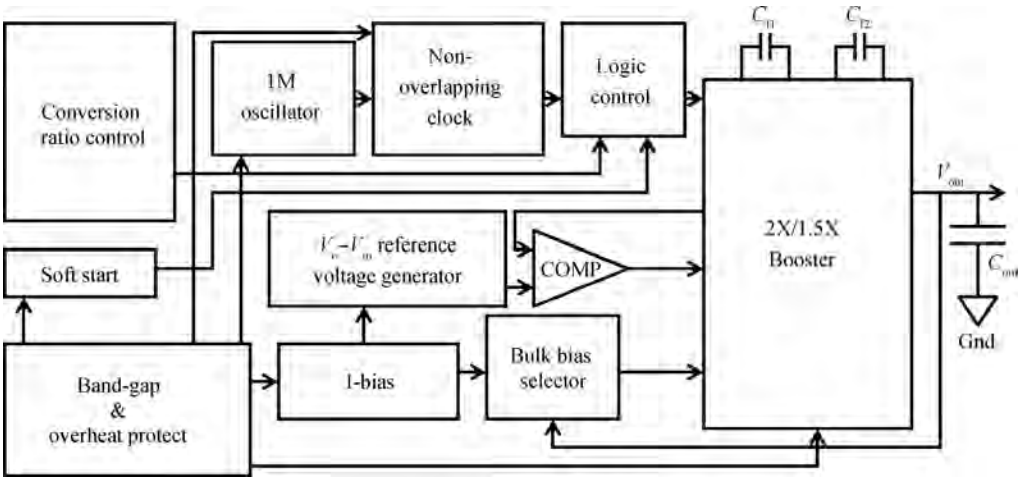

Fig. 8. The scheme of the charge pump.

Table 2. Simulation results.

Mode	Input (V)	0 mA load (V)	5 mA load			10 mA load		
			V_{out} (V)	Ripple (mV)	Eff. (%)	V_{out} (V)	Ripple (mV)	Eff. (%)
2X	1.6	2.520	2.511	1.68	77.4	2.504	3.34	77.6
	1.7	2.518	2.509	1.70	72.3	2.502	3.36	72.9
	1.8	2.516	2.507	1.69	68.7	2.500	3.35	69.2
1.5X	1.8V	2.513	2.505	1.69	90.9	2.502	3.37	91.9
	1.9	2.510	2.500	1.70	85.4	2.496	3.34	86.3
	2.0	2.510	2.494	1.68	81.1	2.491	3.33	82.0
	2.1	2.510	2.490	1.68	77.3	2.486	3.38	78.1

Table 3. Same charge pump with pulse skipping modulation.

Mode	Input (V)	0 mA load (V)	5 mA load		10 mA load	
			V_{out} (V)	Ripple (mV)	V_{out} (V)	Ripple (mV)
2X	1.6	2.509	2.509	50.79	2.506	47.68
	1.7	2.506	2.513	63.16	2.518	60.01
	1.8	2.505	2.506	47.35	2.504	48.96
1.5X	1.8	2.505	2.507	27.81	2.504	28.64
	1.9	2.510	2.509	26.16	2.506	24.32
	2.0	2.515	2.513	40.63	2.512	40.37
	2.1	2.520	2.516	56.59	2.515	51.93

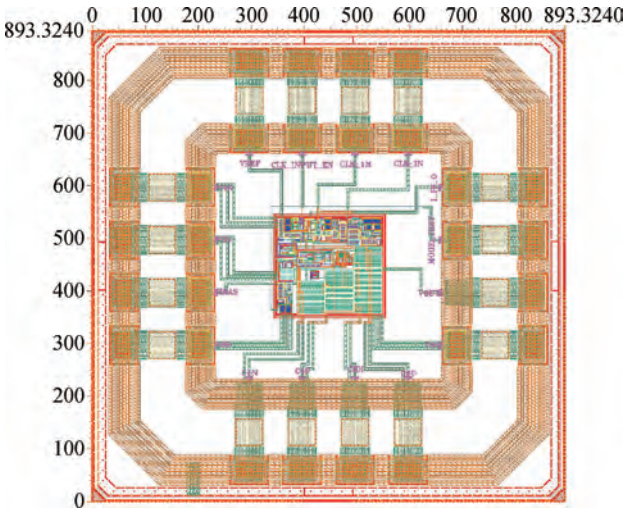

Fig. 9. Layout of the test chip in SMIC 40 nm CMOS process.

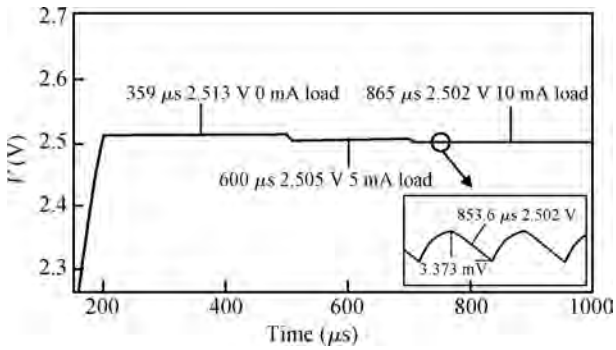

Fig. 10. Transient response of the charge pump with different load currents at a supply voltage of 1.8 V.

Power efficiency at a 10 mA load current versus V_{in} is shown in Fig. 11. The simulation results are close to the theoretical values.

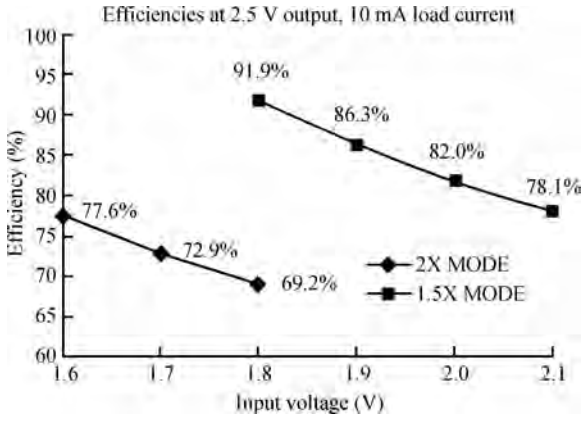

Fig. 11. Power efficiency at 10 mA load current versus V_{in}.

4. Summary

This proposed low ripple charge pump for PCM uses a novel method to regulate the output voltage for a low output ripple and fast transient response. The 2X/1.5X automatic conversion ratio booster could get a high power efficiency over a wide input voltage range. In the SMIC 40nm CMOS process, a simulation was implemented for a DC input range of 1.6–2.1 V and the DC output of 2.5 V with a maximum load condition of 10 mA. The results show the output ripple caused by charge redistribution was eliminated. The ripple voltage below 4 mV and of 250 × 250 μm^2 core size, meets the requirements of PCM programming. A maximum power efficiency 91% can be reached.

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