High voltage SOI LDMOS with a compound buried layer*

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Abstract: An SOI LDMOS with a compound buried layer (CBL) was proposed. The CBL consists of an upper buried oxide layer (UBOX) with a Si window and two oxide steps, a polysilicon layer and a lower buried oxide layer (LBOX). In the blocking state, the electric field strengths in the UBOX and LBOX are increased from 88 V/μm of the buried oxide (BOX) in a conventional SOI (C-SOI) LDMOS to 163 V/μm and 460 V/μm by the holes located on the top interfaces of the UBOX and LBOX, respectively. Compared with the C-SOI LDMOS, the CBL LDMOS increases the breakdown voltage from 477 to 847 V, and lowers the maximal temperature by 6 K.

Key words: SOI; electric field; specific on-resistance; breakdown voltage
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1. Introduction

Silicon-on-insulator (SOI) devices suffer a low breakdown voltage (BV) and self-heating effect (SHE). The BV is determined by the minimum of the lateral BV (BV_{lat}) and the vertical BV (BV_{ver}). An effective method to enhance the BV_{ver} is to increase the electric field (E-field) strength in the buried dielectric[1−5]. Junction termination and RESURF technologies can improve the BV_{lat}[6]. The Si window can improve the BV and alleviates the SHE in partial SOI devices[7−9].

A novel compound buried layer (CBL) SOI LDMOS is proposed in this paper. The compound buried layer mainly improves the BV_{ver} by collecting the charges on the interfaces; and the RESURF and the field plates enhance the BV_{lat}. Furthermore, the CBL SOI devices can reduce the SHE owing to the Si window.

2. Structure and mechanism

Figure 1 is the schematic cross section of an n-channel CBL SOI LDMOS. The compound buried layer (CBL) consists of a UBOX layer with a Si window and two oxide steps, a polysilicon layer and an LBOX layer. H, L_1 and L_2 are the height and widths of the two oxide steps, respectively. L_W is the Si window width. L_3 is the length of the oxide trench on the right UBOX. L is the length of the left UBOX. $t_{I,U}$ and $t_{I,L}$ are the thicknesses of the UBOX and LBOX, respectively. t_S is the thickness of the SOI layer. The x- and y-direction are given in Fig. 1.

In high voltage blocking state, a high positive voltage is applied to the drain while the source, gate and substrate are grounded, and the inversion-layer holes are formed on the top interfaces of the UBOX and LBOX. The oxide steps prevent partial extraction of the holes on the UBOX by the source, and the UBOX prevents from extracting holes on the LBOX. Consequently, holes are located on these interfaces as shown in Fig. 1(b), and thus, the E-field strengths in the UBOX and LBOX are enhanced. $E_{I,U}$ and $E_{I,L}$ denote the E-field strengths of the UBOX and LBOX. They are written as:

$$E_{I,U} = (E_S\varepsilon_S + qQ_{I,U})/\varepsilon_I, \tag{1}$$

$$E_{I,L} = (E_p\varepsilon_S + qQ_{I,L})/\varepsilon_I, \tag{2}$$

where E_S and E_P are the E-field strengths of the Si and polysilicon in the Si/UBOX and polysilicon/LBOX interfaces, respectively. ε_S and ε_I are the permittivities of Si and SiO_2; $Q_{I,U}$ and $Q_{I,L}$ are the hole charge densities on the top interfaces of the UBOX and LBOX. If breakdown occurs at O point, the BV is approximately expressed as:

$$BV = E_{S,C}(0.5t_S + \varepsilon_S t_{I,U}/\varepsilon_I) + (t_{I,U}qQ_{I,U} + t_{I,L}qQ_{I,L})/\varepsilon_I. \tag{3}$$

$E_{S,C}$ is the Si critic field. E_P can be ignored (as seen in Fig. 3(a)) because the high density holes ($Q_{I,L}$) on the LBOX top interface shield the polysilicon layer from the E-field.

For the C-SOI, the holes on the BOX top interface are extracted by source and holes are ignored, and the E-field strength of the BOX is $E_I = E_{S,C}\varepsilon_S/\varepsilon_I$. The BV of the C-SOI with a BOX thickness $t_I = (t_{I,U} + t_{I,L})$ is thus written as:

$$BV = E_{S,C}\left[0.5t_S + \varepsilon_S\left(t_{I,U} + t_{I,L}\right)/\varepsilon_I\right]. \tag{4}$$

3. Results and discussion

Figure 2 shows hole concentration distributions on the top interfaces of the UBOX and LBOX in the CBL SOI, and the

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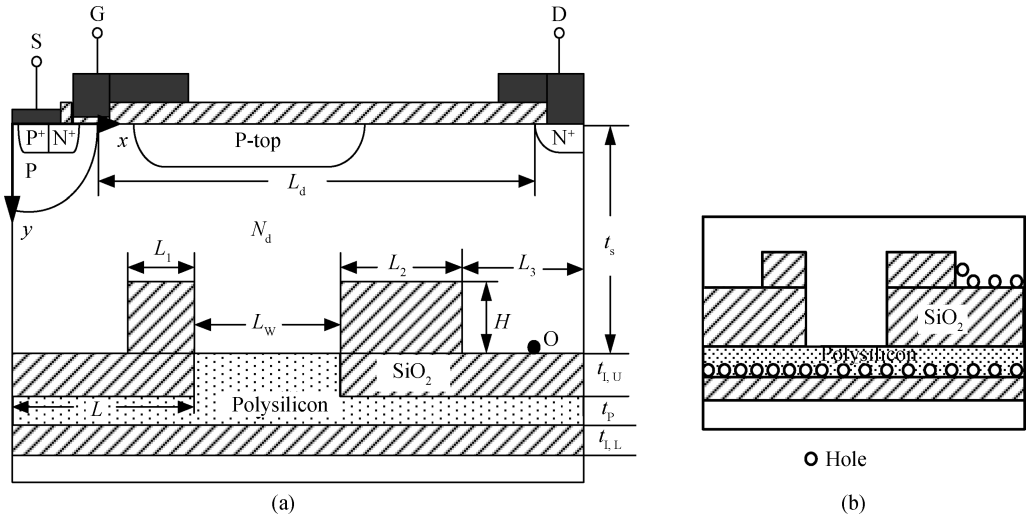

Fig. 1. Schematic cross sections of (a) CBL SOI LDMOS and (b) hole distribution in the CBL SOI LDMOS.

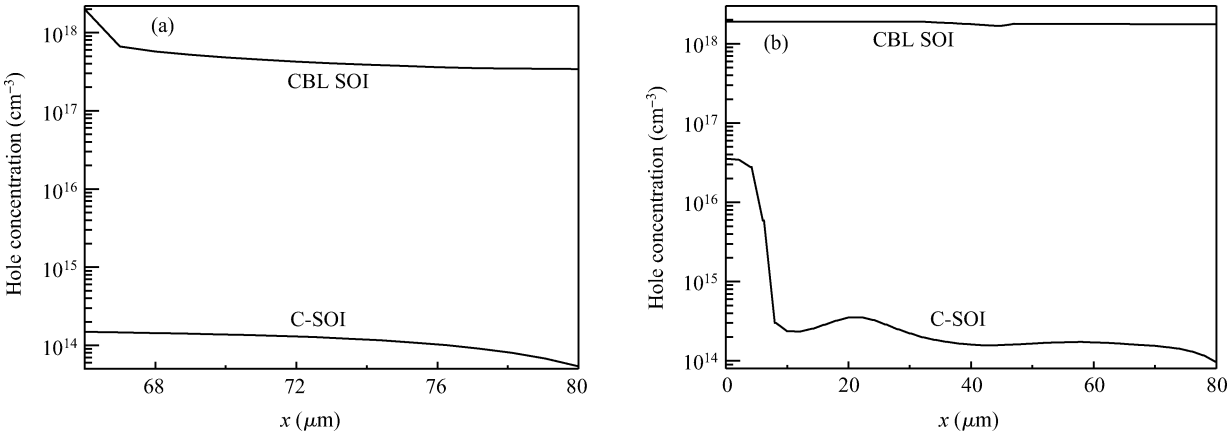

Fig. 2. Hole concentration distributions (a) on the UBOX top interface of CBL SOI and in the BOX top interface of C-SOI under the drain, and (b) on the top interfaces of the LBOX and BOX in the x-direction.

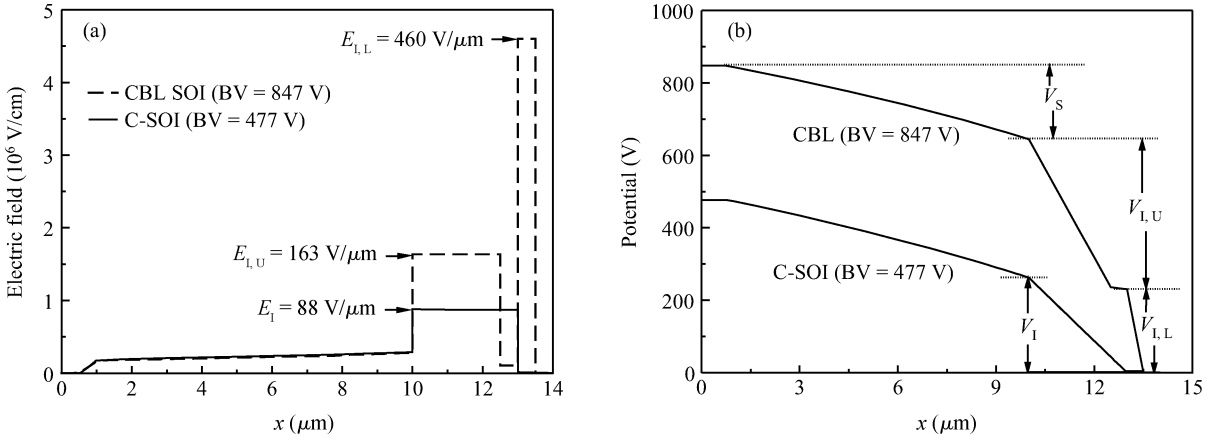

Fig. 3. (a) E-field distributions and (b) potential distributions in the y-direction under the drain end ($x = 79$ μm).

BOX top interface in the C-SOI. Under the drain, the hole concentration on the UBOX increases from below 10^{14} cm^{-3} of the C-SOI to 10^{17} cm^{-3} order of magnitude in Fig. 2(a); the hole concentration on the LBOX is 10^{18} cm^{-3} order of magnitude in Fig. 2(b). The thickness of the inversion layer is 0.1 μm and the hole concentration linearly decreases with the distance from the UBOX or LBOX in the inversion layer, and thus, the $Q_{I,U}$ and $Q_{I,L}$ are 10^{11} cm^{-2} and 10^{12} cm^{-2} order of magnitude by simulation. Figure 3 shows the E-field and potential distributions in the y-direction. $E_{I,U}$ increases to 1.63×10^6

V/cm of the CBL SOI from 8.8×10^5 V/cm of the BOX in the C-SOI; especially, $E_{\mathrm{I,L}}$ reaches 4.6×10^6 V/cm. The increases in $E_{\mathrm{I,U}}$ and $E_{\mathrm{I,L}}$ enhance the voltages sustained by the UBOX and LBOX, denoted by $V_{\mathrm{I,U}}$ ($= E_{\mathrm{I,U}} \times t_{\mathrm{I,U}}$) and $V_{\mathrm{I,L}}$ ($= E_{\mathrm{I,L}} \times t_{\mathrm{I,L}}$), as seen in Fig. 3(b). BV $= V_{\mathrm{S}} + V_{\mathrm{I,U}} + V_{\mathrm{I,L}}$ for the CBL SOI LDMOS while BV $= V_{\mathrm{I}} + V_{\mathrm{S}}$ for the C-SOI, where V_{S} and V_{I} are the voltages sustained by the SOI layer and BOX.

Figure 4 shows the eqi-potential contours. The right oxide trench on the UBOX collects holes and thus increases the E-field strength in the dot line rectangle in Fig. 4(a) in comparison with that in Fig. 4(b). Owing to lack of the UBOX and oxide steps, the potential drop in the dot line rectangle of Fig. 4(b) is much less than that of Fig. 4(a). Figure 4(c) shows the surface field distribution for CBL SOI and C-SOI. Without the UBOX and oxide steps, the lateral E-field at source side is very low. The equi-potential contours distribution and the surface electric field of the CBL SOI are more uniform than those of the conventional SOI in Figs. 3 and 4. Therefore, the average E-field strength in the lateral is enhanced and thus improves the $\mathrm{BV_{lat}}$. Figures 3 and 4 demonstrate that the CBL SOI reshapes the vertical and lateral E-field distributions and thus improves both the $\mathrm{BV_{lat}}$ and the $\mathrm{BV_{ver}}$.

Figure 5(a) shows the dependence of the BV and specific on-resistance ($R_{\mathrm{on,sp}}$) on H, L_1 and L_2 at $L_{\mathrm{W}} = 16$ μm and $L = 30$ μm, where the location and the length of the Si window are fixed while the L_1 and L_2 lengthen/shorten to the source and drain, respectively. Figure 5(b) is the E-field distribution in the y-direction. $Q_{\mathrm{I,U}}$, and thus $E_{\mathrm{I,U}}$ as well as $V_{\mathrm{I,U}}$, increase with the increases in H and L_2. However, most potential contours are located within the right oxide step and the UBOX, the voltage drops across the SOI layer (denoted by V_{S}) and the LBOX ($V_{\mathrm{I,L}}$) therefore decrease for the large L_2 and H values. So BV firstly increases and then decreases. L_1 has little influence on BV. The high H narrows the current path, leading to a high $R_{\mathrm{on,sp}}$. The optimal value of H is 2 μm taking a trade-off between BV and $R_{\mathrm{on,sp}}$ into consideration. For a large L_2 value, the space of the SOI layer is compacted and thus the optimal N_{d} increases, resulting in a decrease in the $R_{\mathrm{on,sp}}$. The L_2 of 20 μm is optimal.

Figure 6(a) shows the influences of L and L_{W} on BV, and Figure 6(b) is the E-field distributions in the y-direction, where $L_1 = 14$ μm, $L_2 = 20$ μm and $H = 2$ μm. The inset in Fig. 6(b) is the potential distribution under the source. The potentials at $\mathrm{O_1}$, $\mathrm{O_2}$ and $\mathrm{O_3}$ are the same, and the potential at $\mathrm{O_3}$ is equal to the value of the $V_{\mathrm{I,L}}$ (as seen in Fig. 4(a)), which is also shown in the inset figure. In Figs. 6(a) and 6(b), as the L increases, the potential at $\mathrm{O_1}$, and thus, $E_{\mathrm{I,L}}$ and $V_{\mathrm{I,L}}$ increase. The increase in L or L_{W} actually causes a decrease in L_3, resulting in an increase in the $Q_{\mathrm{I,U}}$, $E_{\mathrm{I,U}}$ and $V_{\mathrm{I,U}}$ hence increase; V_{S} nevertheless decreases for large L and L_{W}, owing to the reduction of space to include potential contours for the SOI layer with a decreasing L_3. Therefore, the BV firstly increases and then decreases with L and L_{W}. The optimal structure parameters are $L_{\mathrm{W}} = 16$ μm and $L = 30$ μm. It can be concluded that the location of $\mathrm{O_1}$ and the length of L_3 affect BV significantly.

Figure 7(a) shows the surface temperature profiles at $V_{\mathrm{d}} =$ 10 V or 20 V and $V_{\mathrm{g}} = 15$ V. The temperature of CBL SOI is lower than that of C-SOI, especially at the high V_{d}. The maximal temperature (T_{max}) for CBL SOI is lowered by 6 K than

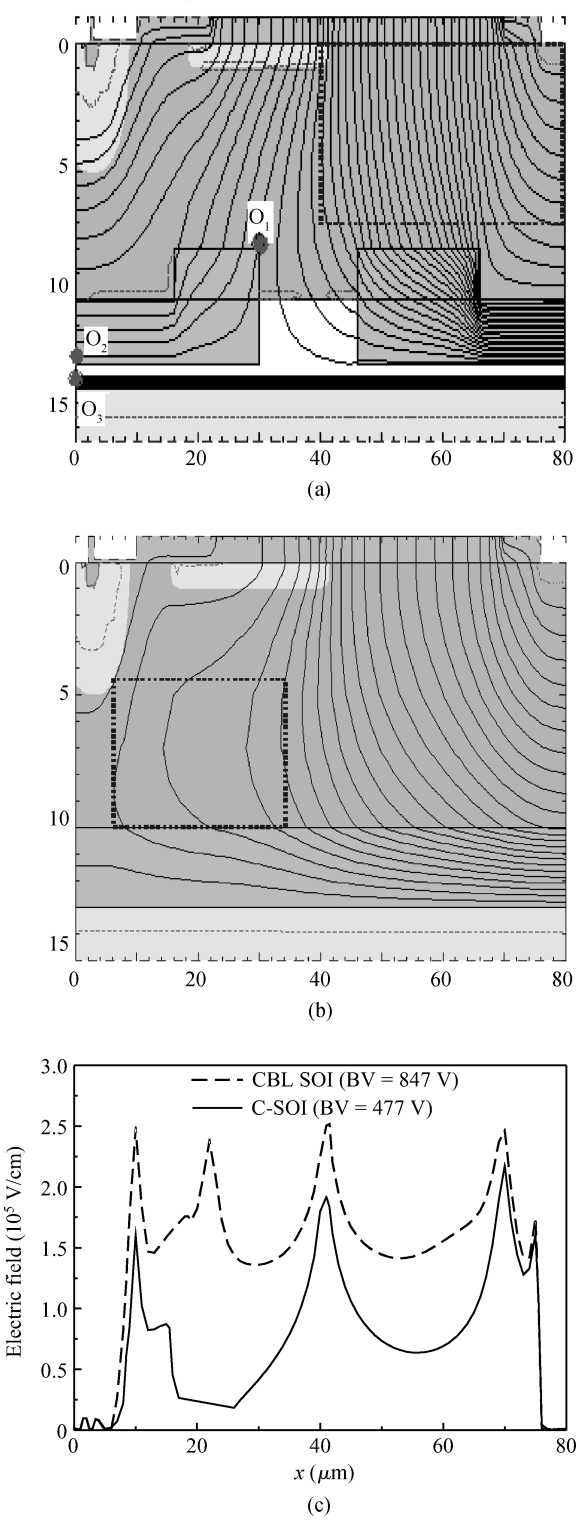

Fig. 4. Eqi-potential contours (20 V/contour) of (a) CBL SOI and (b) C-SOI LDMOSFETs. (c) Surface electric field distribution.

that of the C-SOI at $V_{\mathrm{d}} = 10$ V and $V_{\mathrm{g}} = 15$ V, owing to both the Si window on the UBOX and the thin LBOX alleviating the self-heating effect. Figure 7(b) demonstrates the BV and T_{max} as the function of t_{I1} or t_{ox} for CBL SOI and C-SOI. The BV and T_{max} increase with the increase in t_{I1} or t_{ox}, while the T_{max} increases slowly for the CBL SOI compared with that of the C-SOI. Therefore, the CBL SOI is more suitable for high

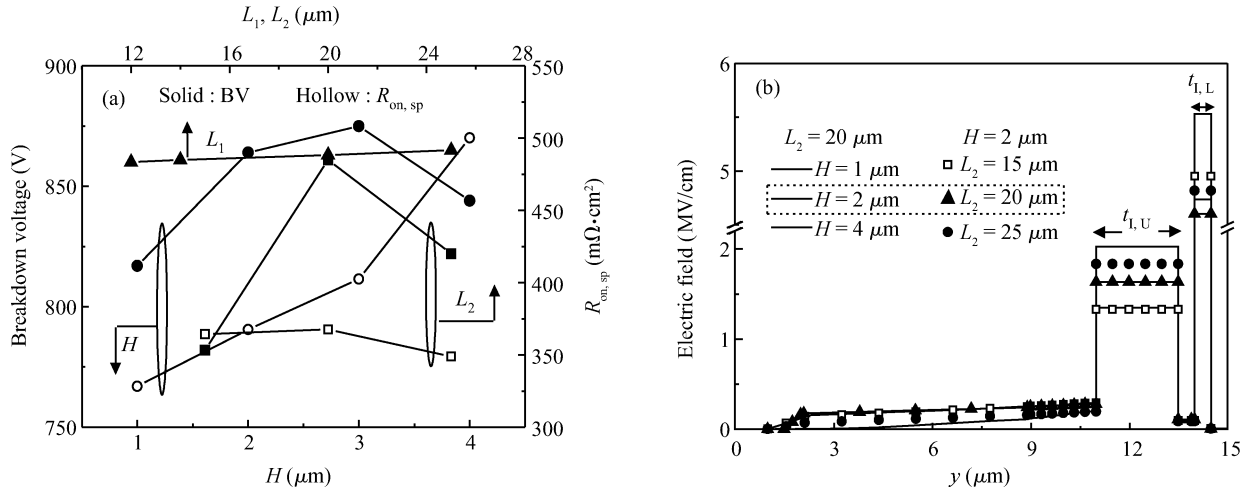

Fig. 5. (a) Dependences of BV and R_{on} on H, L_1 and L_2. (b) Influences of H and L_2 on the E-field distribution under the drain.

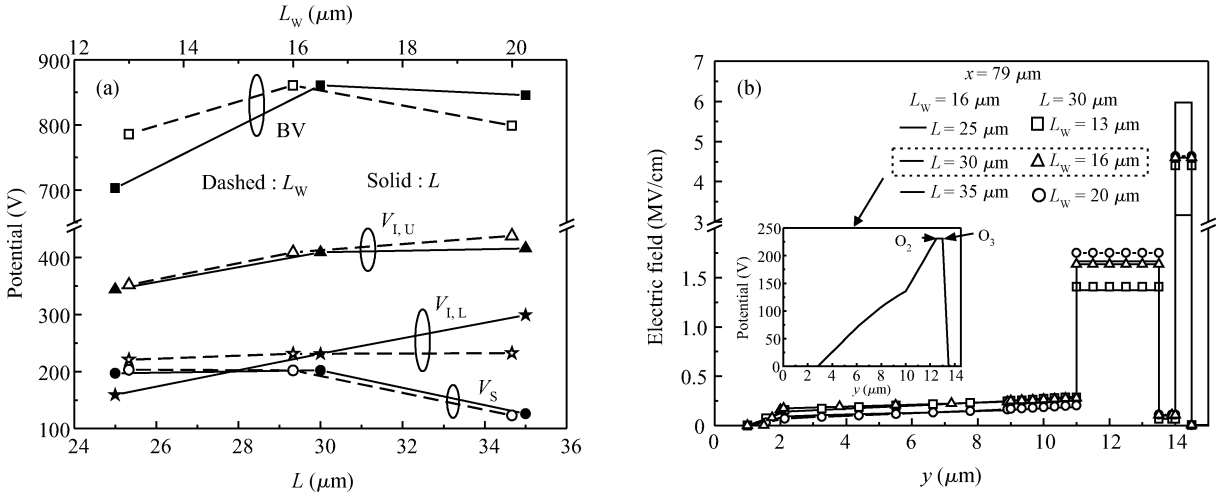

Fig. 6. (a) Influences of L and L_W on BV (BV = $V_S + V_{I, U} + V_{I, L}$). (b) Influences of L and L_W on the E-field distributions at the drain end (x = 79 μm). The inset figure is the potential distribution under the source (x = 0.1 μm).

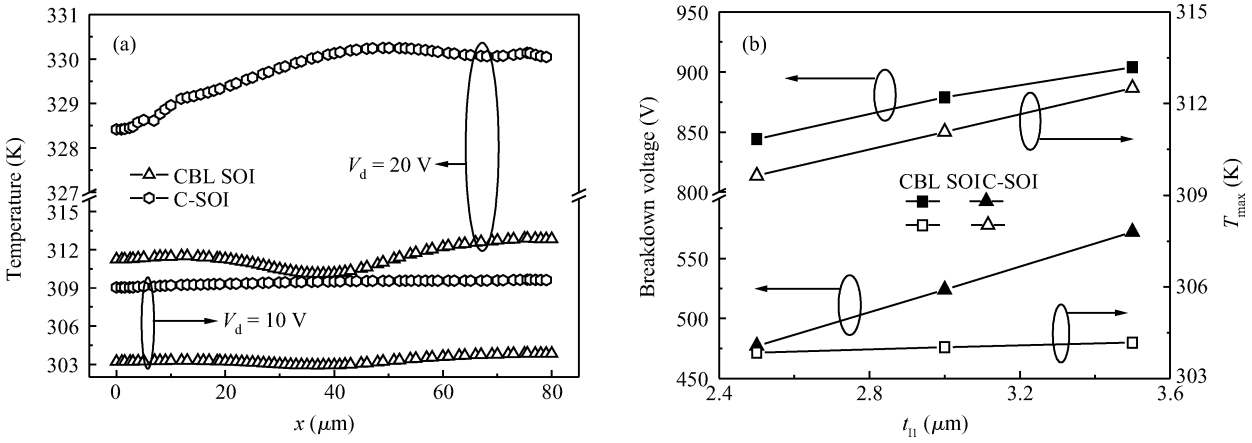

Fig. 7. (a) Surface temperature profiles at V_d = 10 V or 20 V and V_g = 15 V. (b) T_{max} as a function of t_{I1} for CBL SOI and t_{ox} for C-SOI at V_d = 10 V and V_g = 15 V (t_{I2} = 0.5 μm for CBL SOI).

temperature and high voltage applications.

The key processes of the CBL SOI wafer are given as follows: device wafer: oxidation and Si_3N_4 deposition, photolithography and etch twice to form Si trenches, followed by local thermal oxidation and the deposition of SiO_2 to form oxide steps and UBO, polysilicon deposition and planarization; handle wafer: oxidation; bonding and thinning, in which two-sided photolithography is used three times to transfer alignment marks of the buried patterns to the device wafer surface. The LDMOS on the CBL SOI wafer is fabricated by using the standard MOS process.

4. Conclusion

An SOI high-voltage LDMOS with a compound buried layer is proposed. The BV for the CBL SOI LDMOS increases from 477 V of the C-SOI to 847 V due to the holes located on the interfaces of the UBOX and LBOX. The maximal temperature for the CBL SOI is lowered by 6 K than that of the C-SOI. The CBL SOI devices proposed are suitable for high voltage or high power applications.

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