A 10-bit 50-MS/s reference-free low power SAR ADC in 0.18-μm SOI CMOS technology

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Abstract: A 10-bit 50-MS/s reference-free low power successive approximation register (SAR) analog-to-digital converter (ADC) is presented. An energy efficient switching scheme is utilized in this design to obtain low power and high frequency operation performance without an additional analog power supply or on-chip/off-chip reference. An on-chip calibration DAC (CDAC) is implemented to cancel the offset of the latch-type sense amplifier (SA) to ensure precision whilst getting rid of the dependence on the pre-amplifier, so that the power consumption can be reduced further. The design was fabricated in IBM 0.18-μm 1P4M SOI CMOS process technology. At a 1.5-V supply and 50-MS/s with 5-MHz input, the ADC achieves an SNDR of 56.76 dB and consumes 1.72 mW, resulting in a figure of merit (FOM) of 61.1 fJ/conversion-step.

Key words: successive approximation register; analog-to-digital converter; reference-free; on-chip calibration; energy efficient

DOI: 10.1088/1674-4926/33/9/095005 **EEACC:** 1265H

1. Introduction

For applications requiring medium-to-high resolution and medium-to-high speed ADCs, the pipelined architecture is considered to be the most optimal one in terms of power consumption and area[1−4]. However, recently, for tens of MS/s with 10-bit to 12-bit applications, the successive approximation register (SAR) design has re-emerged as a valuable alternative to the pipelined solution[5, 6].

In recent years, with the feature size of CMOS devices scaled down, SAR ADCs have achieved several tens of MS/s to low GS/s sampling rates with 5-bit to 10-bit resolution[7−9]. With thinner line-widths, the FOM value of a SAR ADC has been improved significantly, the state-of-the-art device is in the range of tens of fJ/conversion-step and the conversion rate can reach up to 50-MS/s. However, most of these achievements are obtained in 65 and 90 nm technologies[6−9], while the FOM value of designs fabricated in 0.18-μm is in the range of 100–200 fJ/conversion-step. It is difficult to obtain a FOM value lower than 100 fJ/conversion-step in 0.18-μm process technology[10]. Meanwhile, most of the high-resolution ADCs have a strong dependence on pure analog supply voltage and an on-chip/off-chip reference to ensure their performances, which makes the designs not suitable for embedded applications.

In SAR ADCs, the main sources of power consumption are the DAC network, comparator, voltage reference and digital control circuit. The power consumption of the comparator and DAC capacitor networks are limited by mismatch and noise. Recently, several energy efficient switching methods have been proposed to lower the switching energy of the capacitor network such as monotonic capacitor switching procedure[5] energy-saving[11], set-and-down[12], and these switching schemes all reduce the switching energy significantly. But when considering the reset energy after every conversion, the total power consumption of the DAC capacitor networks are not reduced very much. These methods all depend on high-quality voltage references to ensure the performance of the ADCs which also causes large static power consumption. Pre-amplifiers are commonly utilized to enhance the linearity of the ADCs[5, 13], which will also cause large static power consumption.

This paper presents a 10-bit 50-MS/s reference-free low power SAR ADC fabricated in 0.18-μm SOI CMOS process technology. A passive charge sharing switching scheme is utilized to reduce power consumption significantly as well as the total capacitance of the DAC capacitor network. In addition, the switching scheme removes the dependence on high-quality reference voltage which reduced the static power consumption while making the design more suitable for embedded applications. This paper also presents a no pre-amplifier comparator scheme using a latch-type sense amplifier assisted with on-chip calibration to obtain high accuracy while reducing the static power consumption. This design has a power efficiency of 61.1 fJ/conversion-step and occupies an active area of 0.255 mm^2.

2. ADC architecture

To achieve a 10-bit accuracy, a fully differential architecture is utilized to suppress the substrate and supply noise. Figure 1 shows the architecture of the proposed SAR ADC. It comprises full differential DAC capacitor networks (MDAC), a latch-type sense amplifier (SA), a resistive DAC for calibration (CDAC), a track-and-hold (T/H) circuit, sampling capacitors, calibration logic and SAR logic. The gray parts are the digital parts of the design. The separated T/H circuit and sampling ca-

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Received 19 March 2012, revised manuscript received 10 April 2012

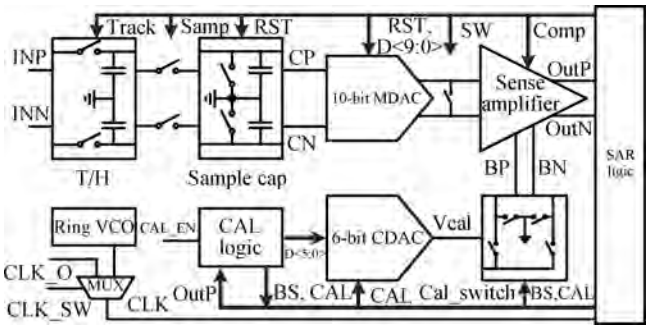

Fig. 1. The proposed SAR ADC architecture.

pacitors can significantly improve the time efficiency which allows the tracking of differential input signals while converting the present held signal[14]. The SAR logic controls the MDAC to perform the binary-scaled feedback during the conversion phase while the calibration logic controls the CDAC to perform the binary-scaled feedback and generate a proper calibration voltage for SA during the calibration phase when the calibration signal is enabled.

As mentioned in the introduction, the DAC capacitor switching scheme utilized in this design obtains great benefits. The switching scheme uses a full passive charge sharing during the conversion phase which is similar to the scheme presented in Ref. [14]. However, the scheme proposed in Ref. [14] suffered from the effects of unequal parasitic capacitances on the top and bottom plants of the capacitor array as well as the parasitic capacitances of the switches. In this design, a full differential capacitor network is implemented so that the DAC is not sensitive to the parasitic capacitance of the capacitor array and the switches. As is described in the next section, the switching scheme combined with the charge redistribution technology reduced the total capacitor further, thus reducing the power consumption. Benefiting from the switching scheme, no reference voltage different from the supply voltage is needed. So the on-chip reference voltage generator can be removed and thus reduces the power consumption further.

Pre-amplifiers are also removed to reduce the power consumption and only one latch-type SA is utilized to make a decision during the conversion phase. On-chip calibration is implemented to eliminate the offset of latch-type SA so that it can satisfy the requirements of precision and operation frequency. By tuning the body node voltages of one transistor pair of SA through the CDAC, the threshold values of this transistor pair can be adjusted, thus the offset of the latch-type SA can be eliminated to smaller than $\frac{1}{2}$LSB to ensure precision. After calibration, the SA can be operated at a frequency up to 500-MHz with low power consumption.

2.1. DAC switching scheme

In the conventional charge redistribution SAR ADC, the bottom plates of the capacitor array are connected to the analog input signal during the sampling phase and are switched to either a high reference voltage ($V_{\rm REF}$) or a low reference voltage (ground) during the conversion phase using the trial-and-error search procedure[15, 16]. The comparator makes the decision whether to switch to $V_{\rm REFH}$ or $V_{\rm REFL}$ from the most significant bit (MSB) to the least significant bit (LSB). The ADC repeats this procedure until the LSB is decided. Although the trial-and-error search procedure is simple and intuitive, it is not an energy efficient switching scheme, especially when unsuccessful trials occur. Meanwhile, during the conversion phase, the reference voltage is connected with the capacitor array and the noise and ripple of it will deteriorate the linearity of the ADC directly.

Figure 2 shows the 3-bit example of the proposed capacitor switching scheme. Passive charge sharing is utilized to perform the binary-scaled feedback instead of conventional charge redistribution during the conversion phase. During the sampling phase, input signals are sampled on $V_{\rm op}$ and $V_{\rm on}$ while the reference voltage is sampled on the top plate of the capacitor array. Then all the switches open and the reference voltage will no longer affect the capacitor array. The MSB bit-cycling is done by comparing $V_{\rm op}[1]$ and $V_{\rm on}[1]$. The value of the MSB sets the array for the second bit estimation. The SAR logic controls the two 2C capacitors to connect with $V_{\rm op}$ and $V_{\rm on}$ directly for charge addition or inversely for charge subtraction as is illustrated in Fig. 2. A relative bit estimation is implemented after this charge sharing. After all the bits have been estimated, another sampling phase follows to prepare for the next conversion. Unlike the switching scheme presented in Refs. [5, 11, 12], there is zero power consumption of switching energy from the reference voltage $V_{\rm REF}$, which is the most different from the other designs. The whole power is consumed during the sampling phase.

The input signals are fully differential with a common voltage $V_{\rm cm} = \frac{1}{2}(V_{\rm inP} + V_{\rm inN}) = \frac{1}{2}V_{\rm ref}$. In this example, only the condition $V_{\rm inP} < V_{\rm inN}$ is considered, and the DACs' output finally settles to the following values:

$$V_{\rm op}[1] = V_{\rm inP}, \tag{1}$$

$$V_{\rm on}[1] = V_{\rm inN}, \tag{2}$$

$$V_{\rm op}[2] = \frac{2}{3}\left(V_{\rm inP} + \frac{1}{2}V_{\rm ref}\right), \tag{3}$$

$$V_{\rm on}[2] = \frac{2}{3}V_{\rm inN}, \tag{4}$$

$$V_{\rm op}[3a] = \frac{4}{7}\left(V_{\rm inP} + \frac{1}{2}V_{\rm ref} + \frac{1}{4}V_{\rm ref}\right), \tag{5}$$

$$V_{\rm on}[3a] = \frac{4}{7}V_{\rm inN}, \tag{6}$$

$$V_{\rm op}[3b] = \frac{4}{7}\left(V_{\rm inP} + \frac{1}{2}V_{\rm ref}\right), \tag{7}$$

$$V_{\rm on}[3b] = \frac{4}{7}\left(V_{\rm inN} + \frac{1}{4}V_{\rm ref}\right). \tag{8}$$

It can be noticed that energy from the reference voltage $V_{\rm ref}$ is only needed when charging the capacitor array during the sampling phase. The energy needed for charging the capacitor array is:

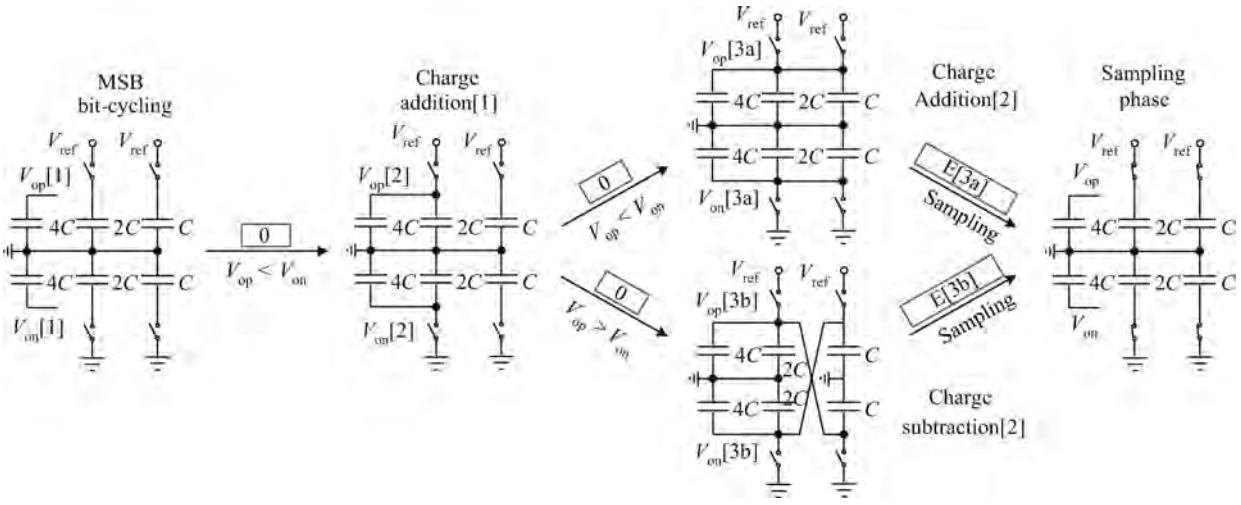

Fig. 2. A 3-bit example of presented switching schemes.

$$E[3a] = \left(V_{\text{ref}} - V_{\text{op}}[3a]\right) V_{\text{ref}} 3C = \left[V_{\text{ref}} - \frac{4}{7}\left(V_{\text{inP}} + \frac{1}{2}V_{\text{ref}}\right)\right] V_{\text{ref}} \times 3C, \tag{9}$$

$$E[3b] = \left(V_{\text{ref}} - V_{\text{op}}[3b]\right) V_{\text{ref}} 3C = \left[V_{\text{ref}} - \frac{4}{7}\left(V_{\text{inP}} + \frac{1}{4}V_{\text{ref}}\right)\right] V_{\text{ref}} \times 3C. \tag{10}$$

Since $E[3a]$ happens when $0 < V_{\text{inP}} < \frac{1}{4}V_{\text{ref}}$ and $E[3b]$ happens when $\frac{1}{4}V_{\text{ref}} < V_{\text{inP}} < \frac{1}{2}V_{\text{ref}}$. It can be deduced that

$$\frac{9}{7}C\,V_{\text{ref}}^2 < E[3a, 3b] < \frac{12}{7}C\,V_{\text{ref}}^2. \tag{11}$$

Figure 5 shows the full differential capacitor array besides the T/H circuit and sampling capacitors utilized in this design. Charge redistribution technology is utilized to obtain equal small capacitors such as $\frac{1}{2}C$, $\frac{1}{4}C$ and $\frac{1}{8}C$ for the last three bits. This method reduced the total capacitor array and thus reduced the power consumption further. So the total capacitor needed to be charged in the sampling phase is only $64C$. It can be calculated that for the 10-bit ADC, $V_{\text{op}}[10]$ and $V_{\text{on}}[10]$ will be approximately $\frac{1}{3}V_{\text{ref}}$ at the end of a successful conversion. So the reference voltage V_{ref} is only needed to charge the 64C from $\frac{1}{3}V_{\text{ref}}$ to V_{ref}, and the energy needed if

$$E[10] \approx \left(V_{\text{ref}} - \frac{1}{3}V_{\text{ref}}\right) V_{\text{ref}} \times 64C = 42.67C\,V_{\text{ref}}^2. \tag{12}$$

The power consumption is significantly reduced compared with other switching schemes. Figure 3 plots the normalized switching energy of the conventional DAC and the proposed DAC with respect to the output digital codes using the V_{cm}-based scheme, energy saving scheme and set-and-down scheme proposed in Refs. [6, 11, 12], respectively. All DAC capacitor arrays implement differential structures and have a 10-bit resolution. The average energy using these schemes is $592C\,V_{\text{ref}}^2$, $255C\,V_{\text{ref}}^2$ and $171C\,V_{\text{ref}}^2$, respectively. Unlike other

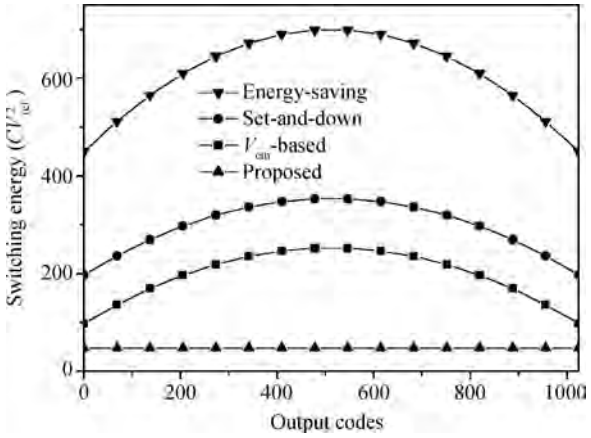

Fig. 3. Switching energy versus output code for different techniques.

switching schemes, the proposed switching scheme is independent to the output codes and has a significant improvement when compared with other schemes. It can grant an additional 75% average benefit compared with the V_{cm}-base scheme.

Other benefits can be obtained from this scheme. Since the reference voltage V_{ref} is only expected to be sampled on the capacitor array during the sampling phase and will not be connected with the capacitor array during the conversion, the supply voltage can be utilized as the reference voltage so long as the supply voltage has a low noise during the sampling phase. During the sampling phase, the digital parts of the ADC will not work until the end of the sampling phase so it is easy to get a pure voltage supply during this phase. As a reference voltage, the supply voltage will not be connected with the capacitor array during the conversion phase, and the noise of the reference voltage will not affect the linearity of the ADC, which is greatly different from the common schemes. Moreover, because there is no need of a high-quality reference voltage generator, the power consumption can be reduced significantly.

2.2. On-chip calibration for sense amplifier

For a high resolution SAR ADC, a pre-amplifier is a good choice to eliminate offset of the comparator. However, in order

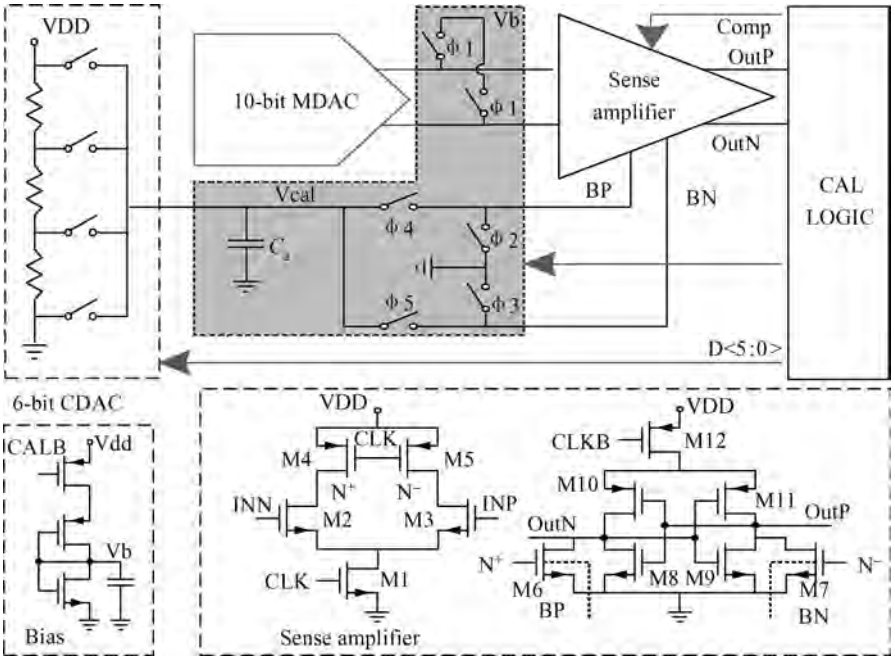

Fig. 4. Block diagram of latch-type sense amplifier with on-chip calibration.

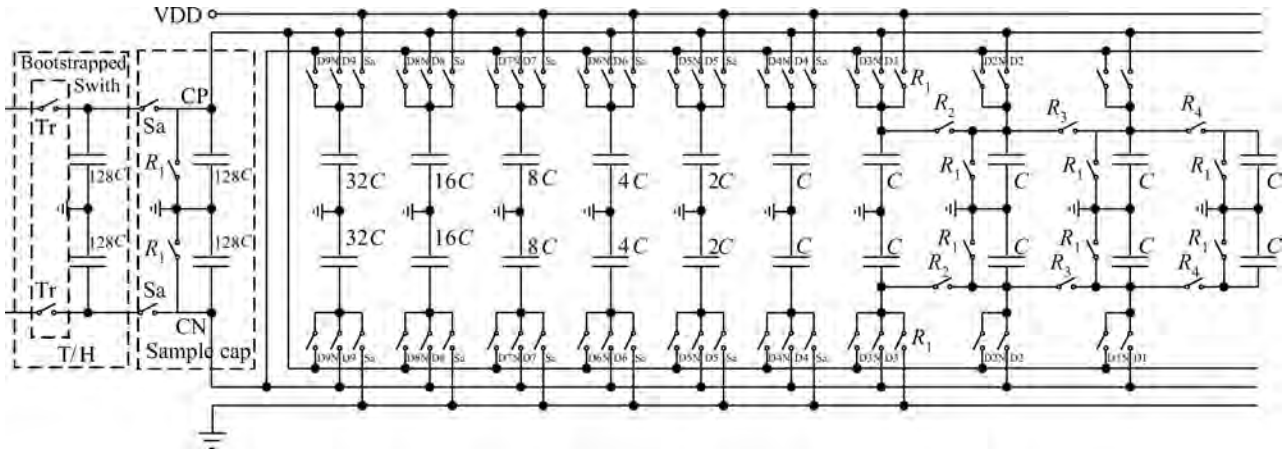

Fig. 5. The full differential capacitor array besides T/H circuit and sampling capacitors.

to ensure a high speed operation and reduce the setting time of the comparator's input signals, a large bandwidth pre-amplifier is usually utilized and this will cause a large static power consumption[13, 17].

In this design, on-chip calibration is implemented for a latch-type SA to eliminate the offset instead of the pre-amplifier. Figure 4 shows the block diagram of latch-type SA with the on-chip calibration. A 6-bit resistive CDAC is realized to provide a calibration voltage to tune the body node voltage of one transistor pair of the SA, thus eliminating the offset to an acceptable level. The detail of the calibration will be described in the next section. Since the load of the CDAC is capacitive, only a small current is needed to implement the calibration. So compared with the common structures, this scheme is more power efficient. Also, because no pre-amplifier is used before SA, there is no problem setting a time for the input signals which are suitable for the high frequency operation.

3. Circuit design

3.1. Capacitor networks

In a high resolution ADC of more than 10-bit, the unit capacitor should be sized larger to meet both the kT/C noise and matching requirements. A unit capacitance of approximately 40 fF metal-insulator-metal capacitor (MIM-cap of $4.5 \times 4.5\ \mu m^2$) is utilized in this design.

The differential capacitor networks besides the T/H circuit and sampling capacitors is shown in Fig. 5. Figure 6 shows the waveforms of the proposed SAR ADC for signal conversion. The operation of the ADC can be explained with these waveforms. Before the start of conversion, there is a reset phase. The charge on the sampling capacitor, C_S, is reset to zero by charge purging while Tr opens to stop tracking and hold the input signals on the tracking capacitor, C_T. At the same time,

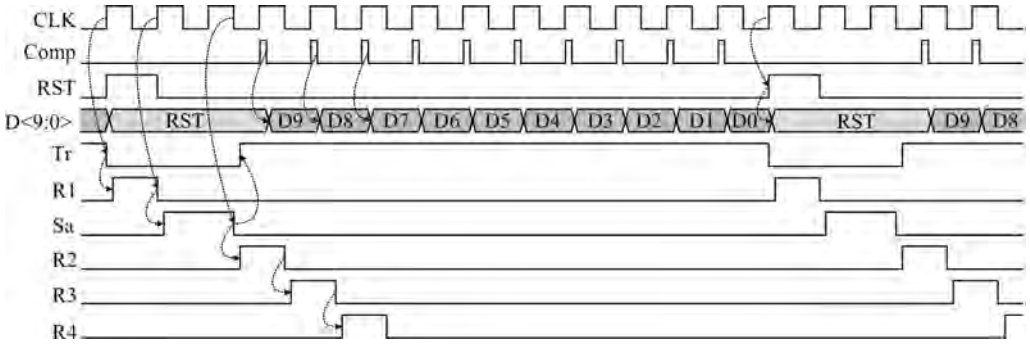

Fig. 6. The waveforms of the proposed SAR ADC for signal conversion.

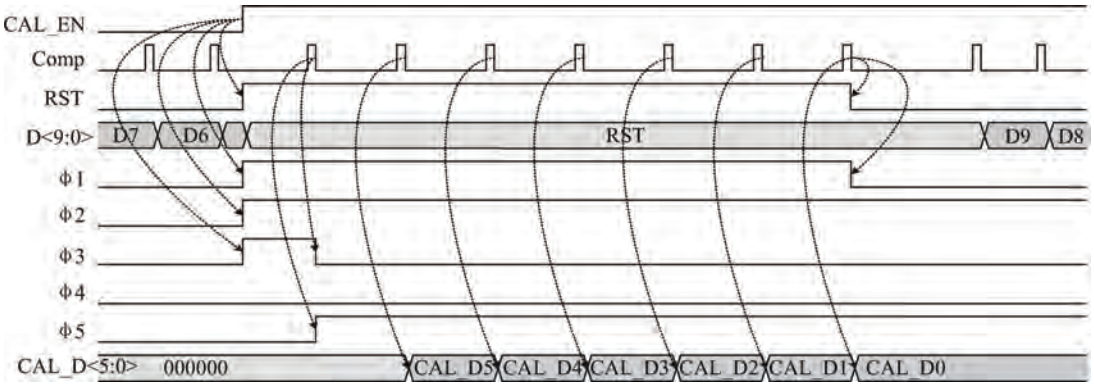

Fig. 7. The waveforms of on-chip calibration.

the binary-scaled capacitor array of unit capacitors C_u is pre-charged to the supply voltage V_{DD}. The charge on the capacitor array will be utilized to provide a feedback DAC function in the SAR ADC, and thus this function is the reference voltage in the charge redistribution SAR. Since this pre-charging happens before the actual analog to digital conversion, it does not depend on the input signal and thus no tough constraints are imposed on this reference.

Then the sampling phase, Sa closes so that half of the charge on C_t can be transferred to C_s in a simple passive charge-sharing action. After sampling, Sa opens and St closes, so the input signals can be tracked again. Since tracking the input signals can be implemented during the whole conversion phase, there is no settling problem.

It can be noticed that a small charge less than CV_{ref} such as $\frac{1}{2}CV_{ref}$, $\frac{1}{4}CV_{ref}$ and $\frac{1}{8}V_{ref}$ are obtained by charge redistribution through the operation of switches R_2, R_3 and R_4 during the first three bit-cyclings. This procedure can reduce the total capacitor of the capacitor array significantly without using the capacitor less than the unit capacitor C_u which will cause a mismatch problem. Meanwhile, since the charge redistribution is operated during the first three bit-cyclings, it will not affect the conversion process.

To determine the MSB, the SA is activated and after it has made a decision, a charge equal to half of the input range is added to or subtracted from the sampled charge by connecting the MSB charged capacitors to C_S directly or inversely. This is again a passive charge-sharing process that does not take any power and settles very fast. The following bits are determined in a similar operation.

It can be deduced that after a successful conversion, the voltage difference between CP and CN will be:

$$\begin{aligned}\Delta V &= V_{CP} - V_{CN} \\ &= \frac{32}{97}\left[(V_{inP} - V_{inN}) \pm \sum_{n=1}^{n=9}\frac{V_{DD}}{2^n}\right].\end{aligned} \tag{13}$$

As shown in Fig. 5, the adding and subtracting of the bit-weighted charge is implemented by operating the switches D9…D1 and D9N…D1N.

3.2. Comparator with on-chip calibration

Latch-type sense amplifiers are kinds of high energy effective comparators. They can achieve fast decisions due to a strong positive feedback but there are usually large offsets which will deteriorate the linearity of the ADC.

As is shown in Fig. 4, a double-tail latch-type SA proposed in Ref. [18] is utilized in this design to obtain a fast decision. In order to eliminate the offset of the SA, on-chip calibration is implemented by tuning the body nodes of the second-stage input transistors M6 and M7 (BP and BN, respectively) to adjust the threshold voltage of these two transistors. A 6-bit resistor string is utilized as CDAC to provide the calibration voltage ranging from zero to the supply voltage for calibration.

Figure 7 shows the waveform of the on-chip calibration. The on-chip calibration can be implemented at any time whenever the calibration enabled signal CAL-EN turns from low to high. When there is a positive edge of CAL_EN, the common signal conversion will be broken and the calibration will

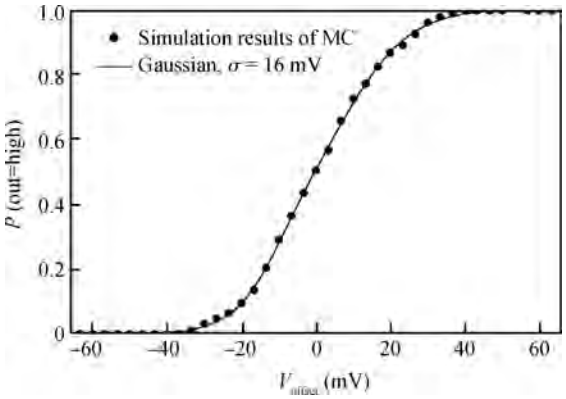

Fig. 8. The SA's equivalent input noise simulated by a Monte-Carlo-simulation.

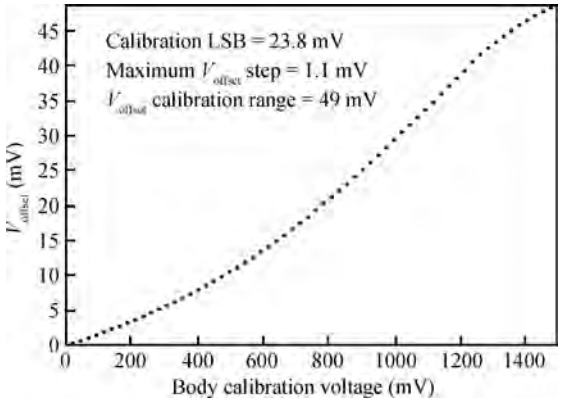

Fig. 9. The body calibration voltage versus V_{offset}.

be implemented. The input of the SA will be connected to the same bias voltage V_{b} and body nodes BN and BP will both be connected to the ground. The SA is operated with the same input to make a decision as to which side should be connected to the calibration voltage V_{cal} so that the threshold voltage of M6 or M7 can be adjusted. Figure 7 illustrates one situation, it was decided that body node BN was to be connected with V_{cal} while BP was connected to the ground. Controlled by the calibration control logic, the 6-bit CADC will prove a final calibration voltage after a SAR process. After the calibration, the final calibration voltage will be tied to the proper body node and the conversion phase will continue until the calibration enabled signal CAL-EN triggers a new calibration. A capacitor C_{a} is added to reduce the feedback noise from the input transistors through the parasitic capacitances crossing the body nodes and source nodes.

Figure 8 shows the SA's equivalent input noise simulated by a Monte-Carlo-simulation when considering both mismatch and process variation, and then fitted the simulation results to a Gaussian cumulative distribution. As is shown in Fig. 8, the simulation results give an equal input offset of $\sigma = 16$ mV.

The CDAC can provide a calibration voltage from 0 to the supply voltage (1.5-V in this design), with a LSB of 23.8 mV. The maximum offset voltage calibration range can reach up to 49 mV to cover a $\pm 3\sigma$ offset. Figure 9 shows the body calibration voltage versus the offset voltage of SA, a maximum V_{offset} step equals 1.1 mV which is less than $\frac{1}{2}$LSB that can be obtained after calibration.

3.3. Full differential T/H circuit

The performance of the T/H circuit will directly affect the performance of the ADC. Boosted-switch topology is usually used for the T/H circuit or S/H circuits to overcome the high V_{t} of the switch devices[13, 19] as well as to increase the input bandwidth and dynamic performance of the ADC.

Conventional NMOS bootstrapped switches can reduce the variation in on-resistance by keeping the overdrive voltage constant. However, some factors of the conventional NMOS bootstrapped switches will still cause errors and introduce nonlinear distortion, resulting in the drop of the circuit accuracy such as clock injection, channel charge redistribution as well as on-resistance variation because of body effect[20, 21].

In this design, a complementary bootstrapped switch including both the NMOS-type and PMOS-type bootstrapped circuits is implemented to overcome the nonlinearity caused by factors such as clock injection and channel charge redistribution. In SOI CMOS process technology, the body nodes of both NMOS and PMOS transistors are both allowed to connect with the source nodes. Utilizing the characteristics of SOI CMOS process technology, it is easy to realize such a full differential structure as is shown in Fig. 10. It consists of a clock boost circuit to provide shift-level clock signals $N = V_{\text{CLK}} + V_{\text{DD}}$ and $P = V_{\text{CLKB}} + V_{\text{DD}}$ for the bootstrapped switches. The NMOS device M14 is the NMOS-type switch with a gate voltage changing from zero to $V_{\text{in}} + V_{\text{DD}}$ during the sampling phase. Similarly, the PMOS device M15 is the P-type switch with a gate voltage changing from V_{DD} to $V_{\text{in}} - V_{\text{DD}}$ during the sampling phase. This ensures that the switches have a $|V_{\text{GS}}| = V_{\text{DD}}$ when sampling, thus reducing the on resistance.

It can be noted that the body node of the NMOS device M14 and PMOS device M15 are both connected to source nodes to eliminate the nonlinearity induced by the variation in threshold voltage caused by the body effect.

3.4. SAR logic and calibration logic

For a high-speed operation, the SAR logic must be well designed to achieve more spare time allocation for the settling of DAC. Meanwhile, in order to reduce the power consumption, the digital part should be simplified.

In order to enhance the time efficiency of the conversion, a self-timed bit-cycling scheme is utilized in this design. Figure 11 shows the full-custom SAR logic for this scheme. The SA outputs OutP and OutN are utilized to trigger the registers to generate relative switch control signals to settle the capacitor array to a new value for next bit decision. OutP and OutN also generate a done signal to reset the SA. It can be noted that there is only a small constant delay $t_{\text{delay}} = t_{\text{CLK-Q}}$ between the SA making a decision and the SAR logic part changing its switching codes for the DAC's new settling. Also, as is shown in Fig. 11, only 20 DFFs are needed to realize the 10-bit SAR operation. This is so that low power consumption of the digital part can be realized while it is still suitable for high frequency operation.

The calibration logic uses a similar structure to control the 6-bit CDAC to obtain a proper calibration voltage. During

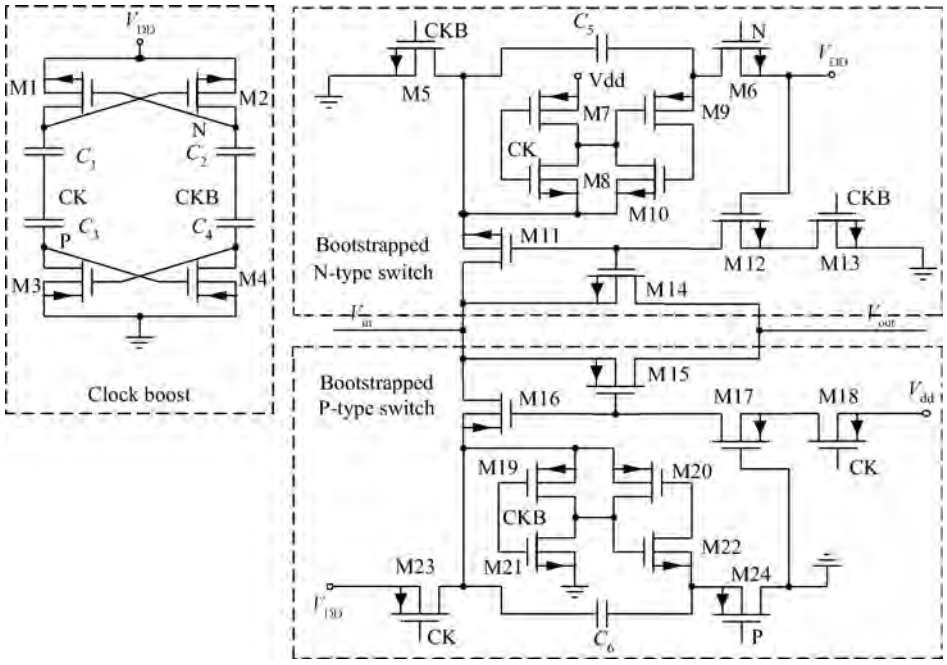

Fig. 10. The schematic of the proposed complementary bootstrapped switch.

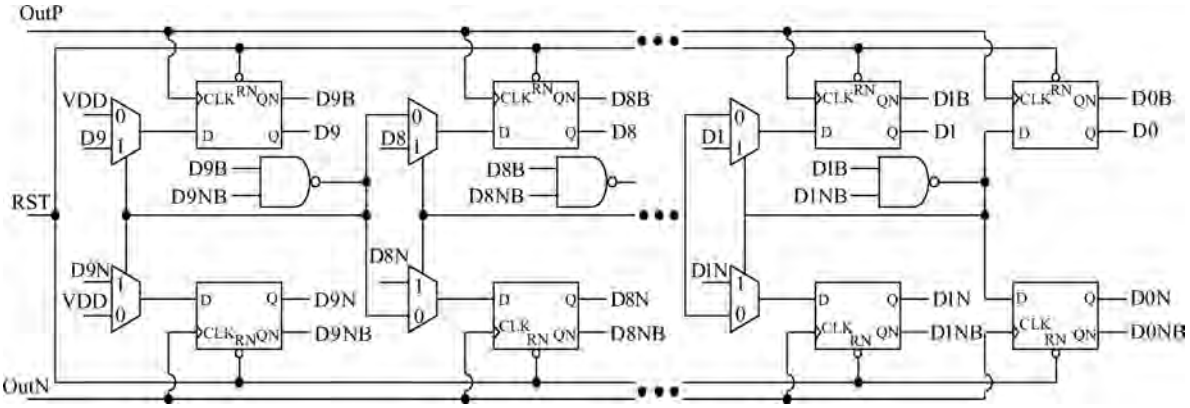

Fig. 11. The proposed SAR logic.

the calibration phase, the SA is operated at a low frequency ($\frac{1}{16} f_{\mathrm{CLK}}$) to enhance precision.

4. Experiential results

The 10-bit SAR ADC was fabricated in 0.18-μm 1P4M SOI CMOS process technology with a supply voltage of 1.5-V. This design consumes 1.72 mW at 50-MS/s. The full die micrograph and the zoomed-in view of the core are shown in Fig. 12. The total area of the chip is 1.37 × 0.45 mm^2, and the ADC core takes up 0.85 × 0.3 mm^2. The main analog parts such as the T/H circuit, capacitor array and SA are implemented symmetrically in physics in order to enhance the linearity of the whole system.

Figure 13 shows the measured FFT output spectrums when the ADC was operating at 50-MS/s with an input of 5-MHz. The measurement results indicate a signal-to-distortion-plus-noise ratio (SNDR) of 56.76 dB, and a spurious-free dynamic range (SFDR) of 64.81 dB can be achieved.

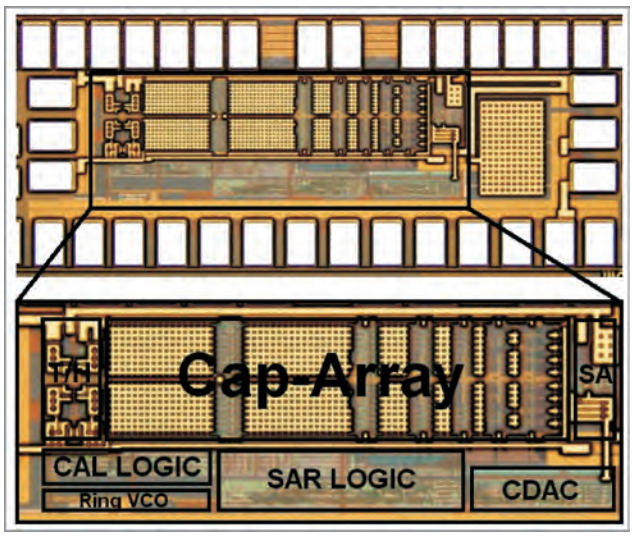

Fig. 12. Die micrograph of the proposed SAR ADC.

Table 1. Comparison with state-of-the-art works.

Parameter	ISSCC' 2009 Ref. [22]	JSSC' 2009 Ref. [23]	JSSC' 2010 Ref. [1]	JSSC' 2010 Ref. [6]	JSSC' 2010 Ref. [24]	TCAS' 2010 Ref. [25]	This work
Architecture	Pipelined	Pipelined	Pipelined	SAR	SAR	SAR	SAR
Technology (nm)	180	90	90	90	65	65	180
Resolution (bit)	10	10	10	10	10	9	10
Sampling rate (MHz)	50	50	100	100	40	50	50
Supply voltage (V)	1.8	1.2	1	1.2	1	1.2	1.5
SNDR (dB)	58.2	49.4	55	56.6	55.1	50.7	56.8
ENOB (bit)	9.4	7.9	8.8	9.1	8.9	8.08	9.1
DNL (LSB)	NA	0.38	0.81	0.79	NA	0.37	0.74
INL (LSB)	0.8	1.29	1	0.86	NA	0.4	0.95
Power (mW)	9.9	1.44	4.5	3	1.21	3	1.72
FOM (fJ/conv.-step)	298	119	98	55	65	55	61

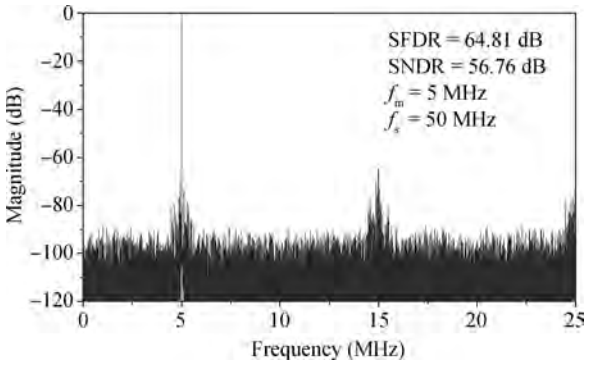

Fig. 13. Measured 64k-point FFT spectra at 50-MS/s for $f_{in} = 5$ MHz.

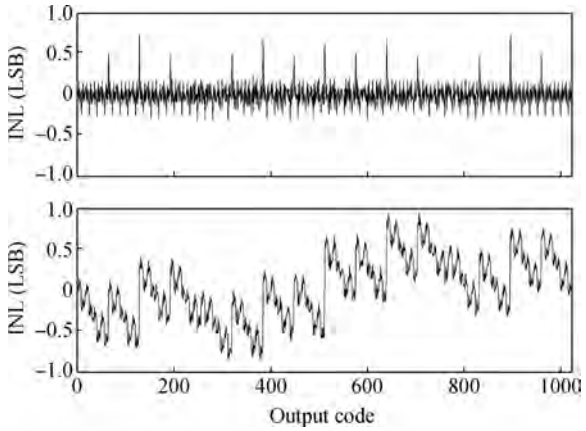

Fig. 14. Measured DNL and INL at 50-MS/s.

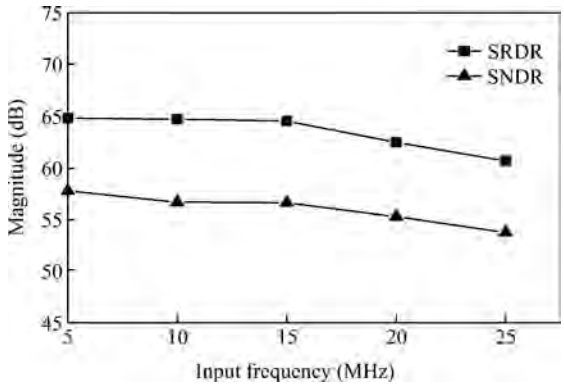

Fig. 15. Measured SFDR and SNDR versus input frequency.

Table 2. Performance summary.

Parameter	Value
Technology	0.18 μm
Resolution	10 bit
Sampling rate	50 MHz
Supply voltage	1.5 V
Full scale analog input	1.5 V_{pp} diff
SNDR	56.8 dB
SFDR	64.8 dB
ENOB	9.1 bit
FOM	61 fJ/conv.-step
DNL	+0.74/–0.33 LSB
INL	+0.95/–0.85 LSB
Power	1.72 mW
Active area	0.255 mm^2

The measured differential nonlinearity (DNL) and integral nonlinearity (INL) of the proposed ADC are shown in Fig. 14. The peak DNL and INL are $+0.74/-0.33$ and the LSB is $+0.95/-0.85$ LSB, respectively.

Figure 15 shows the dynamic performance versus the input frequency with the ADC operating at 50-MS/s. The peak SNDR/SFDR is 56.76 dB/64.81 dB with a peak ENOB of 9.1-bit and decreases to 53.75 dB/60.66 dB when the input frequency increases to the Nyquist frequency.

Table 1 shows the performance summary of this ADC. Table 2 shows the comparison of the proposed ADC with those of previous works with similar resolutions and sampling rate[1, 6, 22–25]. The proposed SAR ADC achieves an FOM of 61.1 fJ/conversion-step.

5. Conclusion

This paper presents a 10-bit 50-MS/s reference-free low power SAR ADC fabricated in 0.18-μm SOI CMOS process technology. A passive charge sharing switching scheme is utilized to reduce power consumption significantly while reducing the total capacitance of the DAC capacitor network. In addition, the switching scheme removes the dependence on a high-quality reference voltage which reduces the static power consumption while making the design more suitable for embedded applications. This paper also presents a no pre-

amplifier comparator scheme using a latch-type SA with on-chip calibration to obtain high accuracy while removing the static power consumption caused by pre-amplifiers. In order to increase the input bandwidth and dynamic performance of the ADC, a complementary bootstrapped switch including both NMOS-type and PMOS-type bootstrapped circuits is implemented. This SAR ADC occupies an active area of 0.255 mm^2. When operating at 50-MS/s with an input signal of 5-MHz, this design can obtain a power efficiency of 61.1 fJ/conversion-step.

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