A 1.8 V low-power 14-bit 20 Msps ADC with 11.2 ENOB

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Abstract: This paper describes the design of a 14-bit 20 Msps analog-to-digital converter (ADC), implemented in 0.18 μm CMOS technology, achieving 11.2 effective number of bits at Nyquist rate. An improved SHA-less structure and op-amp sharing technique is adopted to significantly reduce the power. The proposed ADC consumes only 166 mW under 1.8 V supply. A fast background calibration is utilized to ensure the overall ADC linearity.

Key words: CMOS; opamp-sharing; low-power and background calibration
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1. Introduction

High-speed high-resolution ADC is widely used in wireless communications, instrumentation, medical imaging, etc. In many of these mixed signal systems, the power specification of the ADC is becoming the most critical parameter. However it is very hard to maintain high linearity, good AC performance in terms of signal-to-noise ratio (SNR) and spurious-free dynamic range (SFDR) at high sampling rates with low power consumption. In many approaches, the most power-hungry block, the sample-and-hold amplifier (SHA) is usually removed. This can significantly reduce the power consumption and lower the noise contribution to the subsequent stages[1]. However the MDAC and sub-ADC have to deal with a dynamic input signal instead of a held one, and there is inevitably a large sampling clock skew between two paths[2], which creates a large offset of the sub-ADC. And when this offset error exceeds the redundancy of each pipeline stage, conversion failure happens. Usually the clock buffers, routing and sampling switches have to be matched very well both in design and layout[3]. But it is very difficult to ensure the required matching under process, voltage and temperature (PVT). Some work using the same sampling clock for MDAC and sub-ADC to minimize sampling skew[4], but the sharp clock pulse of sub-ADC will affect the sensitive MDAC and bring great nonlinearity. Besides, as the sizes of sampling switches are different, the large threshold voltage difference will lead to a large sampling skew. The second problem is the first MDAC kickback[1], which can easily affect input sampling network and degrades the overall linearity greatly. The third problem is the comparator offset, which can be easily minimized by using an offset-cancellation or auto-zeroing technique[5]. Finally, the linearity of a 14-bit switch-capacitor ADC is severely limited by the capacitor mismatch. Several previous works propose some improvements to get good linearity performances for high-speed 14-bit pipeline ADC, e.g. Reference [15] uses a pseudorandom dithering for capacitor calibration and Reference [17] needs an on-chip memory to store the error codes for calibration also getting the required static linearity. However, in these works, the calibration needs more than one minute to attain the convergence which is not suitable for many short-latency applications. In Ref. [16], a capacitor-averaging technique is adopted for an SHA-less ADC while consuming very little power and having high SFDR. But the SHA-less structure of Ref. [16] also depends on careful layout match and iterative post-extraction simulation to fight against the sampling skews, and the much reduced clock period for MDAC amplification, which limit the maximum sampling rate operation. In this work, an improved SHA-less front-end sampling is proposed; the input sampling and amplification phase of the sub-ADC complete in half of the sampling phase so that the MDAC amplification is very close to the conventional pipeline ADC, which means the proposed front-end sampling can sustain higher sampling operation. The op-amp is shared between adjacent stages to further reduce the total power consumption and the kickback is removed by using two-pair input. In addition, a fast background calibration is proposed which needs less than 0.5 s to converge, much faster than Refs. [11, 15, 17]. All these techniques guarantee the high performance of the proposed ADC while consuming only 166 mW power at Nyquist rate.

2. Architecture

For a high-resolution high-speed ADC design, switch-capacitor pipeline structure is widely used. The use of multi-bit (above 3.5 bit) for first stage has an optimal power and speed budget in high resolution ADC[5, 6], but for the SHA-less ADC there are a large number of comparators in the sub-ADC which will share the same sampling clock with noise sensitive MDAC, which will bring great design complexity and it is very hard to isolate the MDAC from crosstalk and noise coupling from the sub-ADC path. For design efficiency, the proposed ADC adopts six 2.5 bit stages followed by a 2 bit flash as shown in Fig. 1. Each pipeline consists of a flash ADC and a multiplying DAC (MDAC) and the op-amp of MDAC is shared between two adjacent stages. Fully differential structure is used throughout the design. A background calibration is utilized to guarantee the required overall linearity, which will be described later.

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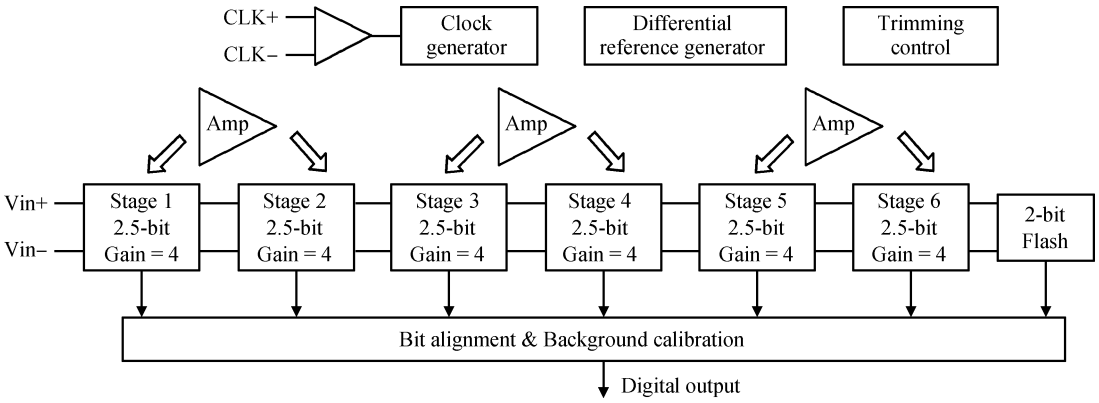

Fig. 1. ADC architecture.

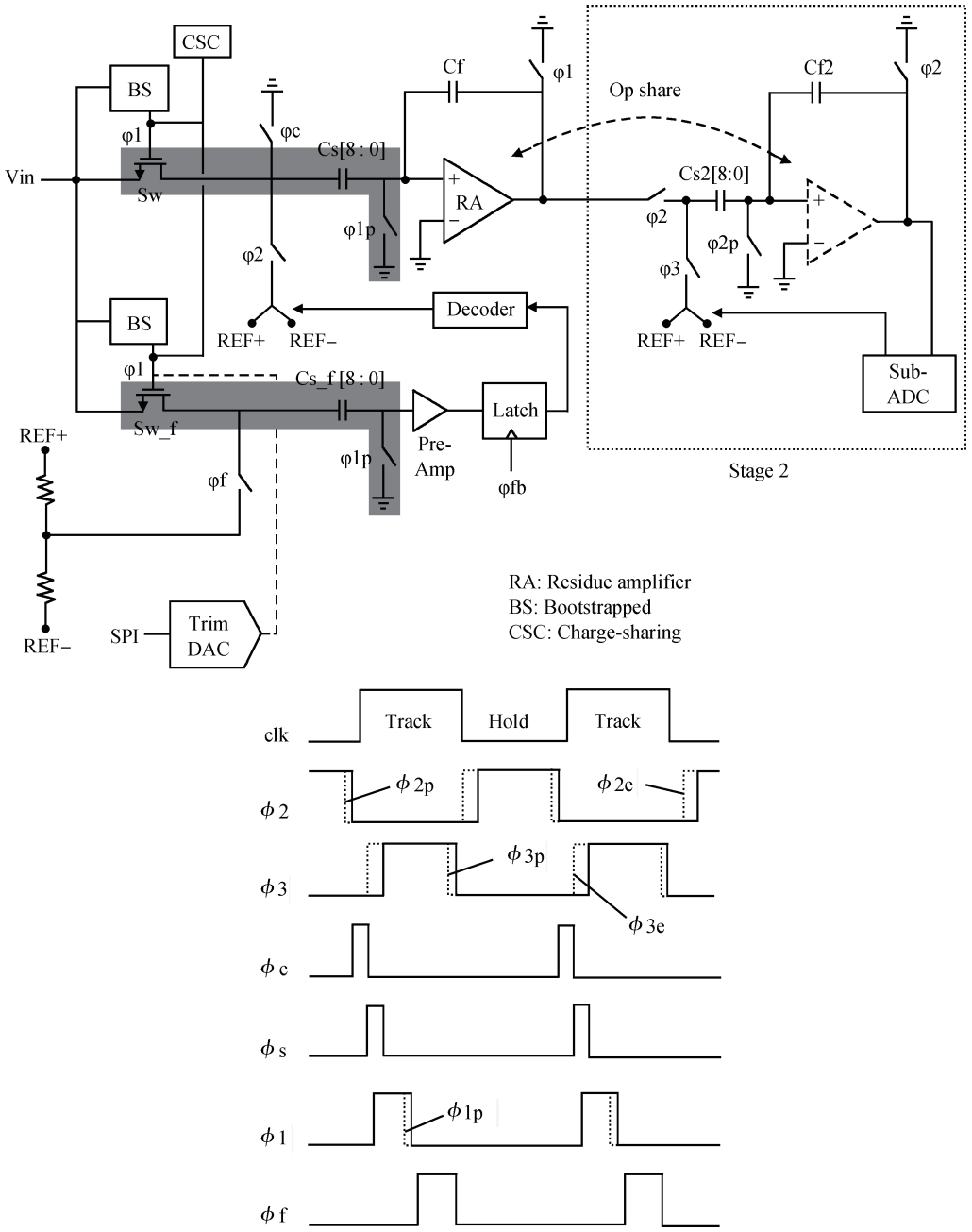

Fig. 2. Proposed op-amp sharing and SHA-less structure and timing.

3. SHA-less structure

As the dedicated SHA is removed, the first stage MDAC and sub-ADC pre-amplifier has to consume a proportion of time to sample the input, and conventionally each comparator of the sub-ADC samples the input and reference and then the pre-amplifier and latch will take a certain amount of time to make decisions, so that the amplification phase of the MDAC residue amplifier (RA) becomes short, which leads to more power consumption[1, 7]. In order to save power, the pre-amplifier is designed to sample and amplify in 1/2 clock period using a single capacitor, which reduces the sub-ADC design complexity and area compared to the conventional SHA-less front-end and the RA in the proposed timing scheme is much closer to the one with SHA as shown in Fig. 2. In this work, the maximum settling time for the RA is about 20 ns while the conventional counterpart is 23 ns. To further reduce the power consumption, the RA is shared between the first MDAC and stage 2. The first stage MDAC and sub-ADC samples the input at the same clock edge, which reduces the aperture error a lot.

One of the difficulties of using this structure is to sample at a short duration of the input and reference sampling period, $\phi 1$ and ϕf in Fig. 2. To make the sample correctly, the input switches (Sw, Sw_f in Fig. 2) have to be large enough to get the required RC constant and linearity. However, a significant charge sharing will take place between the bootstrapped capacitor and switch gate capacitance due to the increase of the switch sizes. So a charge-sharing correction (CSC)[8] is adopted to solve this problem. The input switches Sw, Sw_f, uses floating-well bulk-driven technique[5] to increase the input bandwidth to further ease the external ADC driving. The other problem is the memory effect of the MDAC sampling capacitor. The Cs samples the input at $\phi 1$ and connects to REF+ or REF- at $\phi 2$, then connects back to input to sample the next data. It is inevitable that the previous sample will affect the current sample nonlinearly. A clearing switch with a short phase ϕc is used to solve this problem[1].

The greatest challenge of this SHA-less design is the bandwidth matching of the MDAC and sub-ADC sampling path (shadow area in Fig. 2)[3]. As the sampling capacitors, the input sampling switches and the parasitics as well as the different locations of the two paths are totally different; usually the mismatch is reduced by careful layout and iterative post-layout simulation[1]. But the simulation can not guarantee the same result under different PVT conditions. So a trimming DAC is added to control the power supply of the bootstrapping circuit of sub-ADC input switches via a serial peripheral interface (SPI). With the variation of gate voltage of Sw_f, its on-resistance changes so that the bandwidth matching of the two paths can be achieved. The THD simulation of the proposed SHA-less front-end versus the traditional flip-around SHA (the SHA is designed based on the 14-bit 20 Msps requirement) is shown in Fig. 3, it can be seen that at the sampling rate of 20 Msps, the THD of the proposed SHA-less front-end maintains below –90 dB up to 10.2 MHz and very close to conventional front-end with SHA.

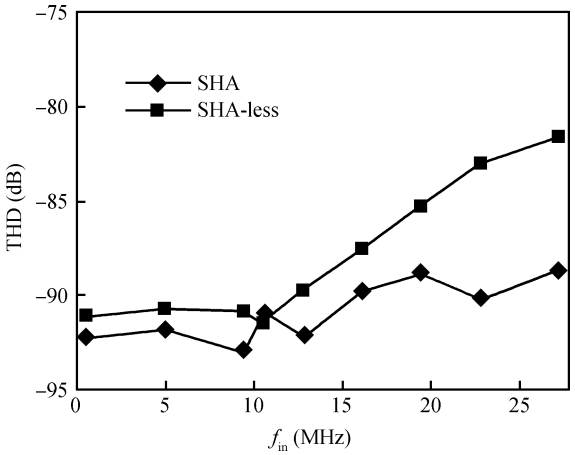

Fig. 3. THD of SHA and SHA-less structure simulated at f_s = 20 Msps.

4. Residue amplifier of MDAC

The 14-bit 20 Msps pipelined ADC requires the residue amplifier (RA) to have 100 dB DC gain and 800 MHz unity-gain bandwidth including a 20% margin. In this work a two-stage amplifier with gain-boosting is used to achieve the high gain, high bandwidth and high swing with reasonable power consumption. As shown in Fig. 4, the C_1, C_2, Amp_c of the feedback amplifier and corresponding switches consist of a common-mode feedback network (the timing shown in Fig. 2). When the RA samples the input at ϕs (timing scheme shown in Fig. 2, ϕs = "1"), the C_1 and C_2 samples the output of first and second stage common mode voltage and adjust to the correct common bias for Mn6, Mn5, and Mn9 via Amp_c. When ϕs = "0", C_1 and C_2 can hold the previous charge. Conventionally, the common-mode feedback needs two reference voltages, and in this scheme there is only one reference voltage needed, reducing the required number of switches and the clock loading. The input pair uses NMOS to save power, while introducing more $1/f$ noise than PMOS pair. But in this work, as the greatest noise contributor SHA has been removed, so the thermal noise reduces a lot which is still deigned within the total noise budget. As the RA is shared between adjacent stages, usually there will be a short phase between $\phi 2$ and $\phi 3$ to clear the interference from inputs of the first stage and the second MDAC[9]. In this work, the valid amplifying phase for the first stage MDAC is very short, so an additional pair of inputs is added to prevent the extra phase occupation. When the RA is utilized in first MDAC, at $\phi 2$e Mn1 and Mn2 will be used as input pair and at $\phi 3$e Mn3 and Mn4 instead.

The RA is miller-compensated with a positive-zero canceling resistor and the pole-splitting makes the two dominant poles move apart. As can been in Fig. 5, the first stage RA has a good phase margin of 67° and 116 dB DC gain with 930 MHz unity-bandwidth, and the settling time of the RA to attend the full swing is 18ns at the worst corner, which is sufficient for this design.

5. Voltage reference

The internal reference voltage is generated from band-gap reference and feeds into a single-to-differential amplifier to form positive and negative reference V_{reft} and V_{refb} respectively in Fig. 6. In order to provide stable and accurate reference to

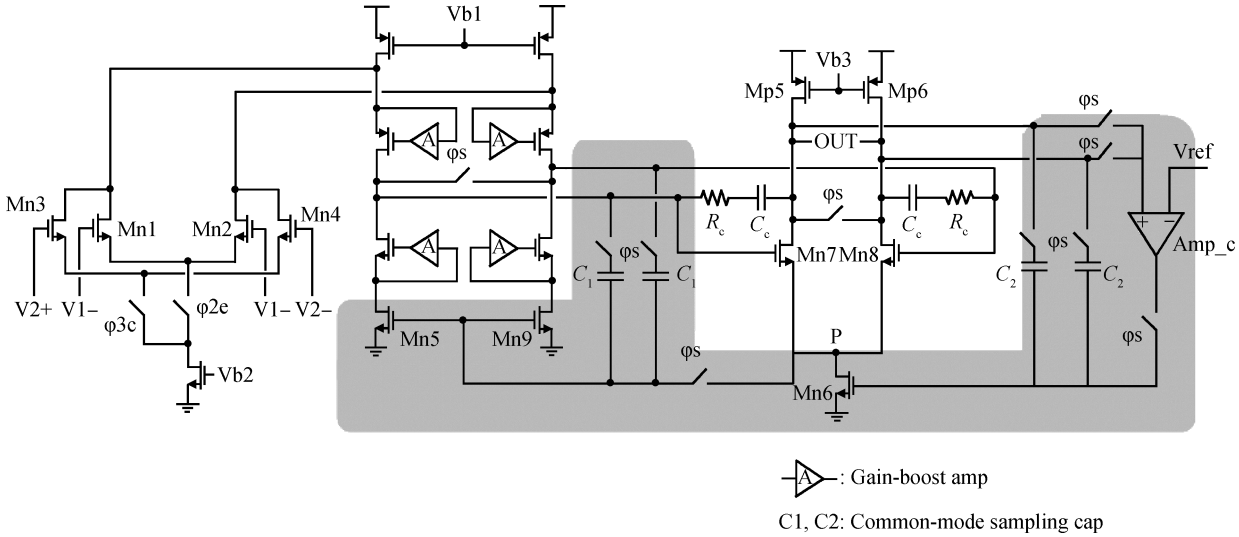

Fig. 4. Residue amplifier used in this work.

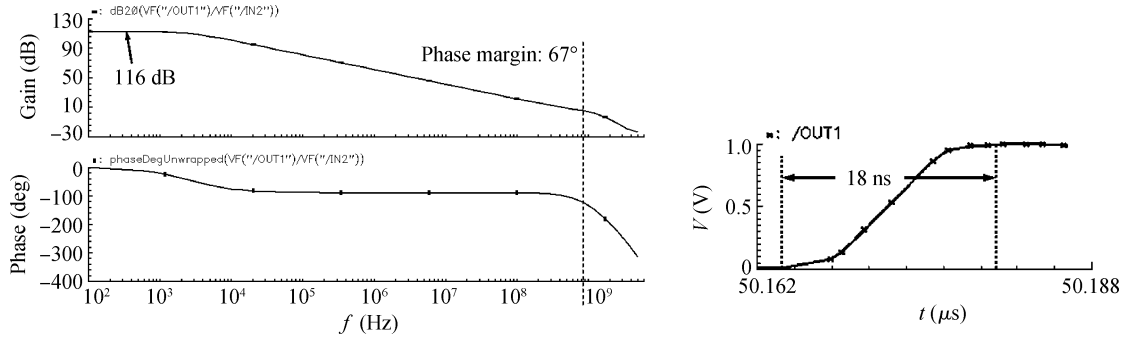

Fig. 5. Simulated DC gain, phase margin and settling time of first stage RA (at worst corner).

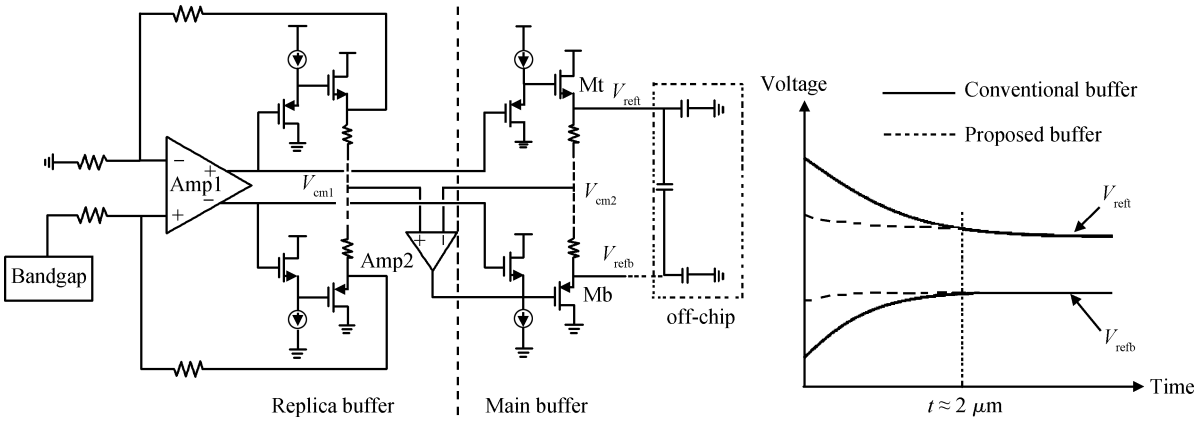

Fig. 6. Internal reference generator and settling behavior versus conventional one.

the internal blocks of pipeline ADC, the reference generator should settle very fast in less than half of the sampling period. As shown in Fig. 6, a replica push-pull buffer connected in negative feedback keeps its loop from being affected by large pipeline transient surges. As a result, even the drift of V_{reft} and V_{refb} can not change the output of the replica buffer. Because the operating point almost keeps constant, the settling behavior of the buffer amplifier is greatly improved. The main buffer, which is externally decoupled, provides very low output impedance. An additional amplifier is added to sense output common-mode voltages of the replica and the main buffer. If common-mode voltage V_{cm2} differs from V_{cm1}, the amplifier will promptly adjust V_{cm2} until it equals V_{cm1}, so that enough matching precision between both buffers can be guaranteed.

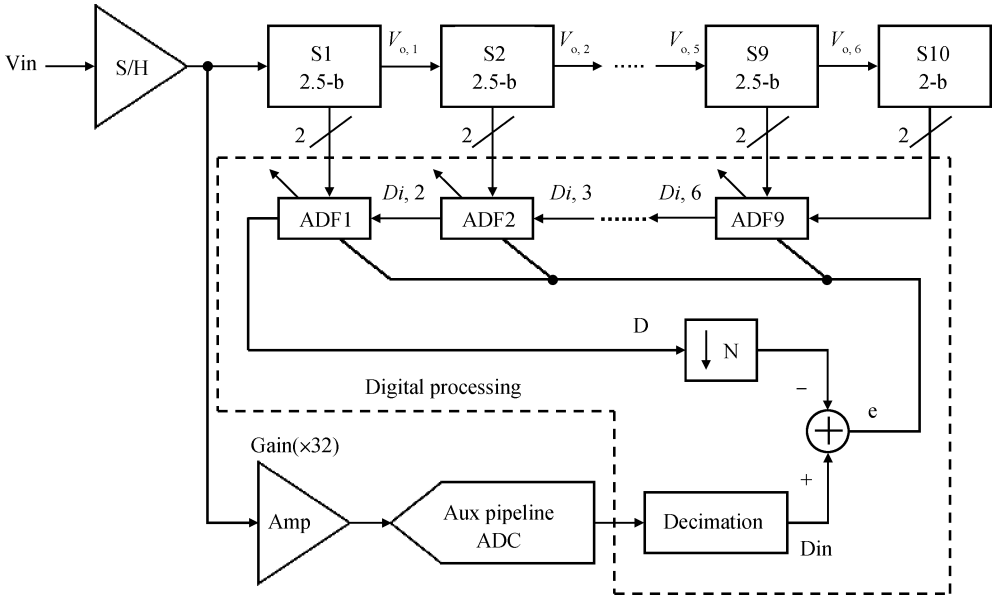

Fig. 7. Background calibration used in this work.

Simulation result shows that the proposed reference buffer can settle much faster than the conventional one (with 2 μs settling time).

6. Background calibration

The main non-linearity comes from the capacitor mismatch and op-amp non-ideality. In this work, an adaptive background calibration is carried out to reduce the non-linearity. As shown in Fig.7, the output codes from each stage of the original high-speed pipeline ADC is applied to an adaptive digital filter (ADF) using LMS (least mean square) algorithm, while the auxiliary pipeline ADC (aux ADC), slow but accurate, is utilized to quantize the S/H output as an accurate version of D_{in}. Similar to Ref. [10], the LMS engine updates the coefficients of ADF according to the difference ("e") between D_{in} and $\hat{D}_{\text{in}}$.

The sample rate and resolution of aux ADC determines the convergence time and accuracy of the calibration respectively. Usually a high-resolution, slow sampling rate sigma-delta ADC is utilized as the aux ADC. To reduce the requirement of the aux ADC, a switched-capacitor amplifier is added with sample-and-hold function to pre-amplify the output of the main S/H by the gain of 32 (2^5). As a result, an 11-bit aux ADC is accurate enough to achieve the input-referred 16-bit accuracy. The slow path, consuming only 10 mW, is designed to be 1/10th the speed of the main ADC ($f_s = 10$ Msps) and needs about 2^{22} samples which translate into less than 0.42 s convergence time. This calibration time is about 2.4 times faster than Ref. [11], and 60 times than Refs. [15, 17]. Besides, unlike correlation-based algorithms[12], this background calibration does not affect the dynamic range of MDAC.

7. Low jitter clock path

The signal-to-noise ratio (SNR) will be significantly degraded by the jitter, which mainly comes from the external clock source and the internal clock path. The clocks will add periodical and random jitter to the ADC, and usually this jitter is much larger than the signal noise. So at a given input frequency, the SNR can be defined by

$$\text{SNR} = -20\log_{10}(2\pi f_{\text{input}} t_{\text{j}}). \tag{1}$$

It is obvious that high-speed ADC is very sensitive to the quality of clock input. The low-jitter source with a proper band-pass filtering can contribute jitter of 30 fs[13]. Referring to Ref. [14], the maximum jitter of ADC is restrained by

$$t_{\text{j(ADC)}} = \sqrt{t_{\text{j}}^2 - t_{\text{j}}^2(\text{clock source})}. \tag{2}$$

Except using a clean clock source, the reasonable way to minimize jitter is to utilize layout isolation, shielding and decoupling technique. Besides, the jitter from the on-chip clock path is

$$t_{\text{j}} = \frac{V_{\text{CLK\_jitter}}}{\mathrm{d}V_{\text{CLK}}/\mathrm{d}t}. \tag{3}$$

So the clock jitter is inversely proportional to the clock signal slope and the slope can be increased by the clock buffer. And the total delay of the clock path is proportional to the clock jitter[17]. In this work, the differential clock input is used to cancel the common-mode noise and a duty cycle stabilizer with short delay controls the clock edge, which is followed by a balanced clock distribution circuit.

As shown in Fig. 8, the buffer followed by a differential-to-single ended amplifier (D-to-S) includes a PMOS input pair which can accommodate a wide input range. The NMOS cross-coupled and diode-connected pair increases the gain so as to increase the clock slope. The DCS consisting of a Schmitt trigger, a low-pass filter and flip-flops, provides the stable 50% duty cycle clock to minimize unwanted spurs and harmonics, allowing the duty cycle of the input clock to vary between 30% and 70%. Certain dummy inverters are added to the clock distribution circuit to balance the capacitance load to reduce the clock skew in each pipeline stage. The proposed clock path can minimize the clock jitter to less than 120 fs.

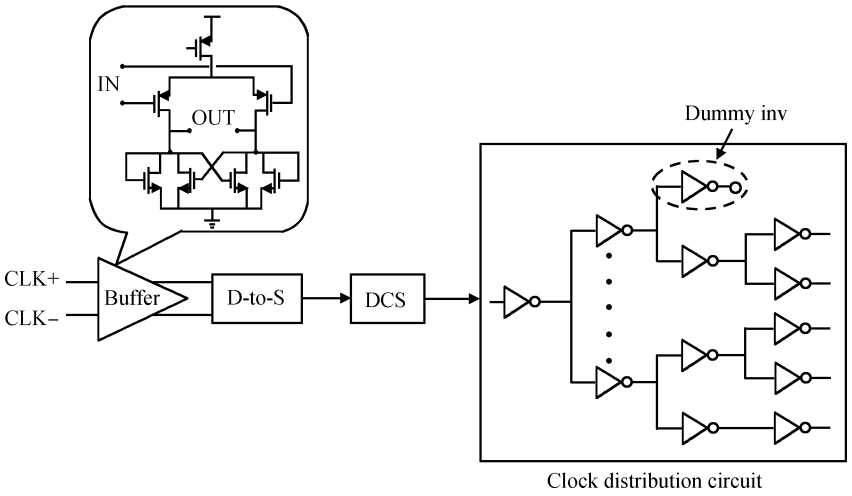

Fig. 8. Low-jitter clock path.

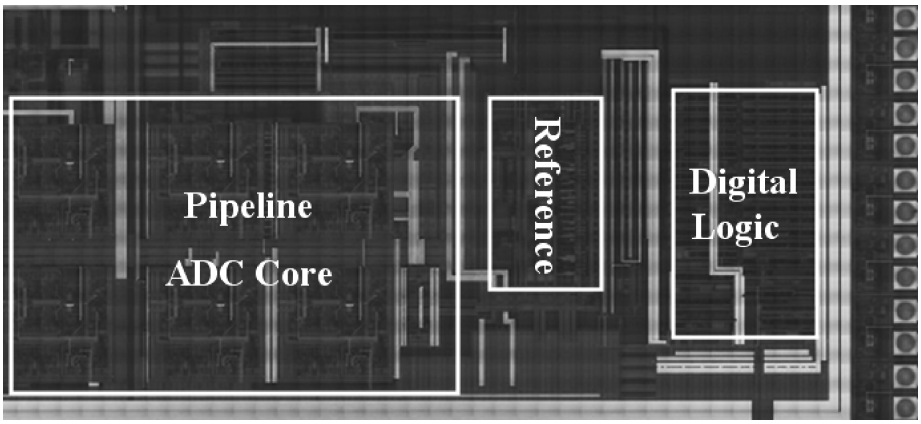

Fig. 9. Die microphotograph.

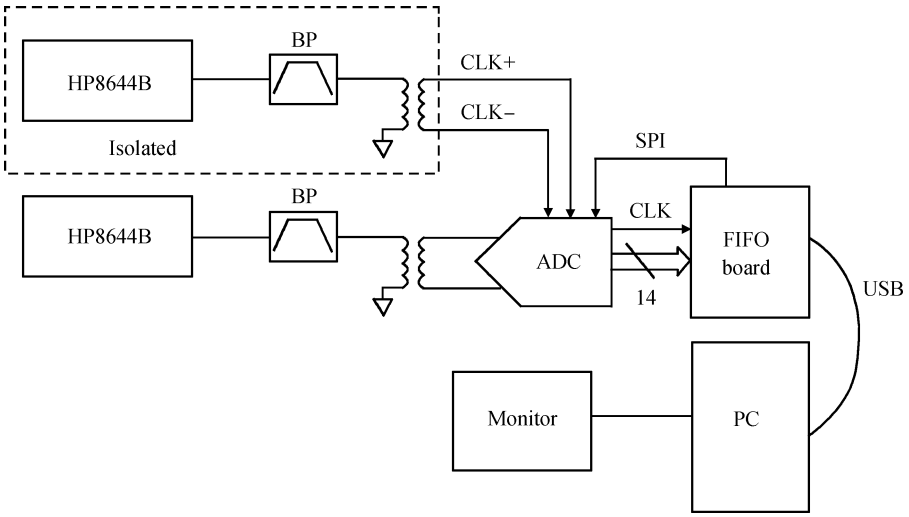

Fig. 10. ADC measurement set up.

8. Experimental results

The ADC is implemented in 1P5M 0.18 μm CMOS process with MIM capacitor, occupying 1.2 mm^2 active area. The die microphotograph is shown in Fig. 9. Necessary guard-rings are used to deal with the substrate noise from the digital circuit. The total power consumption of the ADC is 166 mW including the main pipeline, reference generator, logic circuit, clock buffer and output driver. The power is measured under supply of 1.8 V with 2 Vp-p differential input range with a 9.7 MHz (of Nyquist frequency) and 19.2 MHz frequency under 20 Msps, the corresponding total current consumption which is observed

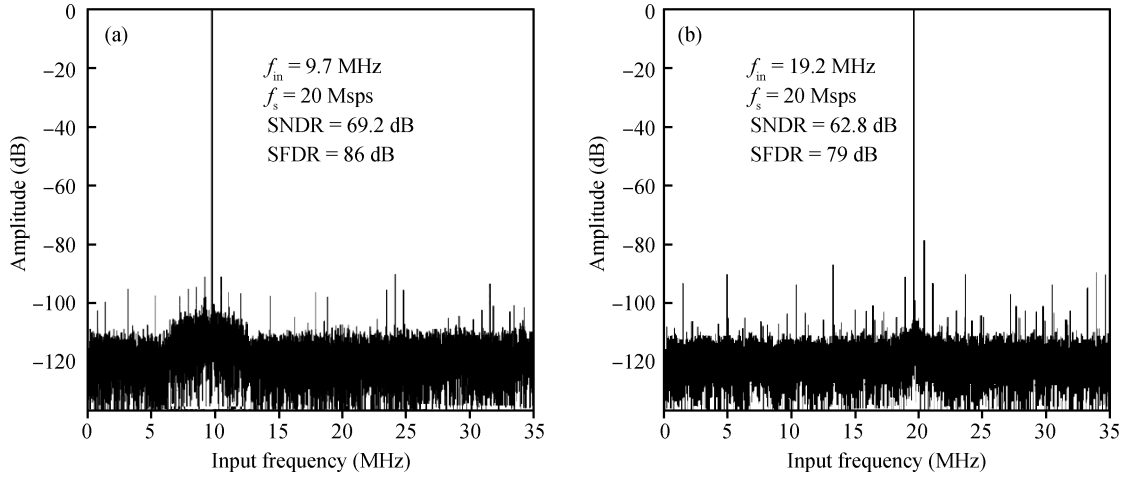

Fig. 11. Measured FFT of the ADC at $f_s = 20$ Msps and –0.5 dBFS input. (a) $f_{in} = 9.7$ MHz. (b) $f_{in} = 19.2$ MHz.

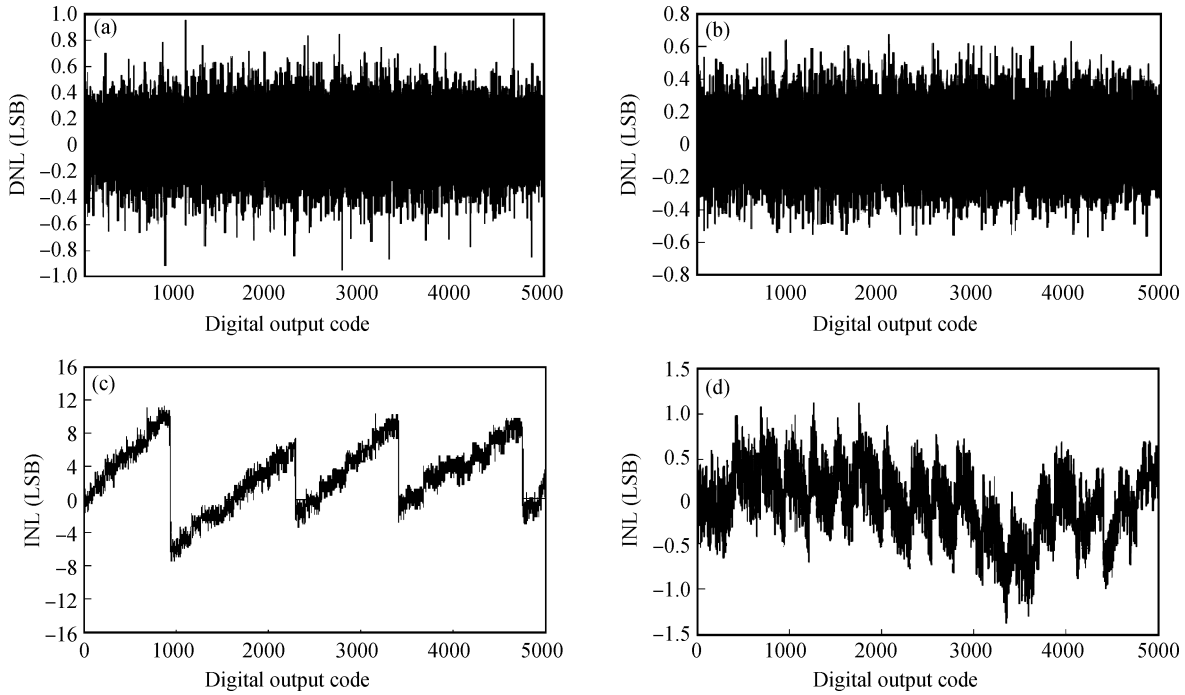

Fig. 12. DNL and INL of the ADC. (a, c) Before calibration. (b, d) After calibration.

by current/voltage meter is about 92.2 mA. As the separate power line is routed for analog and digital section, the power consumption of the analog and digital parts can be measured and the analog part consumes about 3/4 of the total power.

In the test setup (Fig. 10), the input and the clock signal are both using the low-jitter source HP8644B and are narrowly band-passed to provide an input and clock with less than 40 fs jitter. The supply of clock source is isolated from other parts on the board and all the supplies are heavily decoupled and feed to the ADC differentially. The ADC is driven differentially through a high-frequency transformer, which helps maintain the ADC performance in under-sampling case. The SPI input adjusts the internal sampling skews.

Figure 11 shows the FFT test results, where an input of –0.5 dBFS sine wave at $f_{in} = 9.7$ MHz is sampled at $f_s = 20$ MHz, achieving an SFDR of 86 dB and an SNDR of 69.2 dB, which transfers to 11.2-bit ENOB. When the input increases to 19.2 MHz, the ADC presents 79 dB SFDR and 62.8 dB SNDR due to the increase of the harmonic terms. Figure 12 indicates the static performance of the ADC in same measuring condition. When the calibration is disabled, the DNL and INL is $+0.97/-0.96$ LSB and $+11.1/-7.6$ LSB respectively and the DNL reduces to $+0.68/-0.58$ LSB and INL becomes $+1.1/-1.3$ LSB after the calibration is enabled.

To compare the proposed ADC performance with previous works, the figure-of-merit (FOM) is calculated based on the widely accepted formula, $\mathrm{FOM} = P/2^{\mathrm{ENOB}} \cdot f_s$, where P is the ADC power consumption and f_s is the sampling rate. As shown in Table 1, the proposed ADC compares with some 14-bit pipeline ADCs with sampling rate from 10 to 50 Msps. The ADC in this work exhibits high dynamic and static performance. However for design consistency consideration and

Table 1. Performance comparison.

Parameter	Ref. [15]	Ref. [16]	Ref. [17]	This work
Resolution (bit)	14	14	14	14
Sampling rate (MS/s)	30	10	50	20
DNL (LSB)	0.5	0.31	0.39	0.68
INL (LSB)	1	0.58	2.76	1.3
SFDR (dB)	84	98	80.3	86
SNDR (dB)	61	73.6	65.6	69.2
Power (mW)	350	112	142	166
FOM (pJ)	12.7	2.8	1.8	3.53

to save design time, the scaling is not applied in every pipeline stage. The first two stages are of the same size so that the shared RA always sees the same load and the following four stages are all scaled by the same coefficient. In Ref. [16], an optimized scaling technique is used to every pipeline stage. This is the main reason why the proposed ADC consumes more power than Refs. [16, 17], so as the FOM.

9. Conclusion

This paper presents the design of an SHA-less pipelined 14-bit 20 Msps ADC, fabricated in 0.18 μm 1P5M CMOS process under 1.8 V nominal supply. The measured results show that the ADC power consumption is greatly minimized due to the proposed SHA-less front-end and op-amp-sharing technique; the total power including the logic circuit, output driver and reference is only 166 mW with an FOM of 3.53 pJ at 20 Msps. A fast background calibration scheme is carried out to guarantee the ADC linearity and the measured DNL and INL is $+0.68/-0.58$ LSB and $+1.1/-1.3$ LSB respectively.

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