Design and implementation of a 3-A source and sink linear regulator for bus terminators*

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Abstract: According to the requirements of the bus terminal regulator, a linear regulator with 3-A source-sink current ability is presented. The use of the NMOS pass transistor and load current feedback technique enhances the system current ability and response speed. The method of adaptive zero compensation realizes loop stability over the whole load range for either source or sink loop. Furthermore, the transconductance matching technique reduces the shoot-through current through the output stage to less than 3 μA. The regulator has been fabricated with a 0.6-μm 30 V BCD process successfully, and the area size is about 1 mm^2. With a 20 μF output capacitor, the maximum transient output-voltage variation is within 3.5% of the output voltage with load step changes of $\pm$2 A/1 μs. At the load range of $\pm$3 A, the variation of output voltage is less than $\pm$15 mV.

Key words: bus termination regulator; linear regulator; fast response; power management IC
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1. Introduction

So far, linear regulators, especially the low dropout linear regulators (LDO) are widely used in a variety of electronic systems due to their low noise and small size. Large output current and fast transient response has fueled the growth of the linear regulator due to its many advantages[1−4]. Computer systems usually use an electronic bus to communicate signals between various computing devices such as a processor, a memory and input/output (I/O) devices, and the signals are typically driven on the bus by drivers incorporated into each of the computing devices connected thereto. There are two kinds of bus terminators: passive terminators and active terminators. Passive terminators are rarely used because of their power dissipation issue and variation of Thevenin voltage with power supply. On the contrary, due to overcoming the shortcomings of passive terminators, the active terminators have been widely used[5−7].

As active terminators can both pull and push currents, we need a voltage regulator that can source and sink current at a regulation node while providing a regulated voltage at the regulation node. A synchronous switching regulator can be used but it needs a complex circuit, thus increasing the cost, and it may also introduce additional switching noise. A linear regulator is an ideal selection for the bus terminal regulator because of its lower noise, lower cost, and faster transient response[5−11].

The output current of a bus termination regulator depends on computing device processing. Due to the rapid increase of the processing rate in digital systems, the requirement for the transient response of bus termination regulators is becoming more important. According to this bus termination regulator demand, a linear regulator with high response speed and 3A source-sink current ability is proposed in this paper.

2. System design

Figure 1 gives the system structure of the proposed bus termination linear regulator. In order to provide a normal power supply for different bus termination applications, the regulator is designed to output from 0.5 to 2.5 V. As is well known, the power loss of a linear regulator is proportional to the dropout voltage, which limits the output loading capability. In the proposed circuit, an independent power input pin VIN is introduced to reduce the drop-out voltage and guarantee the enough loading capability which can be given a lower power supply without the limitations of minimum operating voltage.

As is shown in Fig. 1, MP1, MP2 are the pass transistors of the source and sink loops, respectively. A buffered stage is applied to drive the gate of the pass transistor. Because of its lower output impedance, the buffered stage helps to eliminate the impact to loop stability caused by the parasitic pole at the gate of the pass transistor[12]. The source compensation network is composed of R_{C1}, C_{C1}, and the sink compensation network is composed of R_{C2}, C_{C2}. Because R_{C1} and R_{C2} vary with the load current, the frequency compensation networks of the sink and source loops are adaptive. This adaptive frequency compensation is very useful to eliminate the bad impact on loop stability attributed by load current variation. In addition, the source and sink loops use the same differential input pair. It not only simplifies the circuit design, but also achieves better circuit matching.

It is critically important to control the DC biased current in

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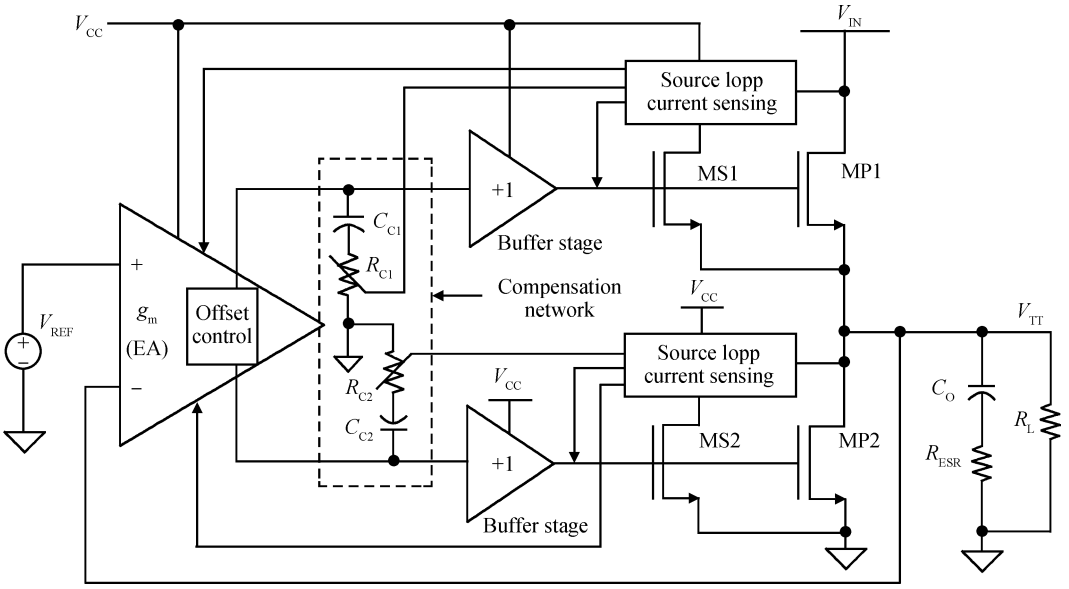

Fig. 1. System structure of the proposed source-sink regulator.

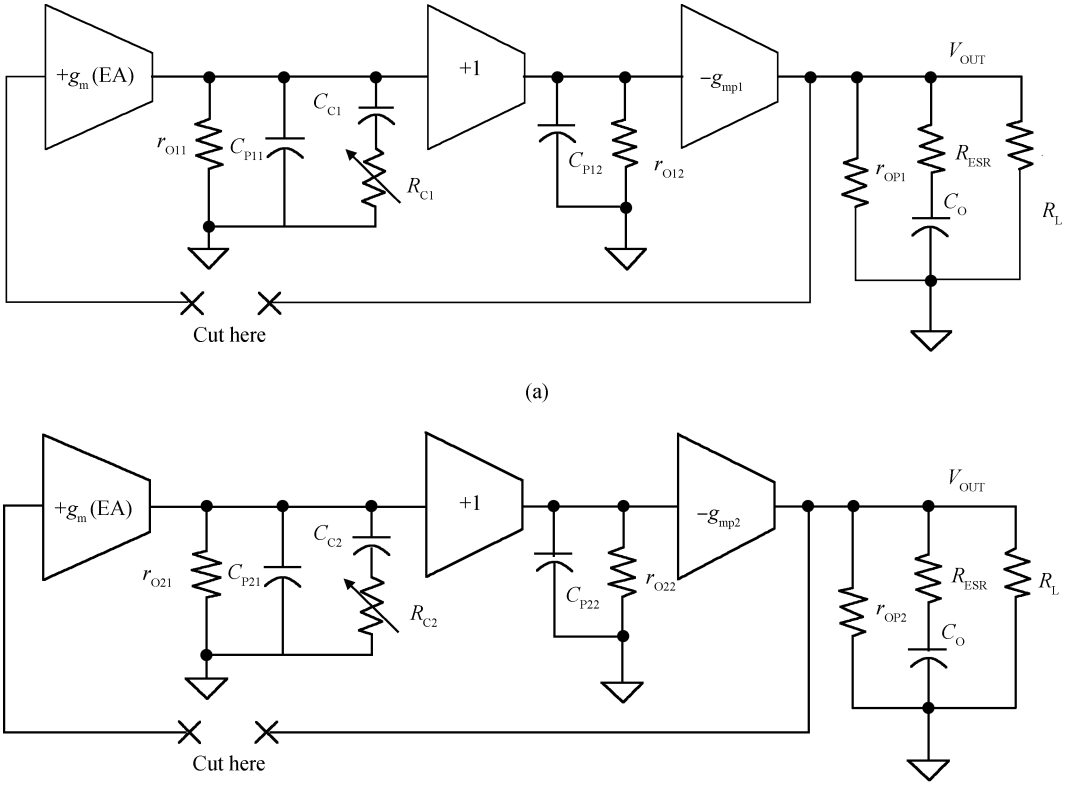

Fig. 2. Loop small-signal model. (a) Source loop. (b) Sink loop.

the output stage for the source-sink structure. In the proposed circuit, a smaller DC biased current in output stage is gained by a transconductance matching technique with a smaller input offset voltage.

3. Loop stability analysis

The small-signal equivalent-circuit model of the proposed source-sink regulator is illustrated in Fig. 2. As the source and sink loops do not work simultaneously, they will be analyzed separately. For the source loop, the dominant pole is determined by C_{C1} and the output impedance of the error amplifier stage, r_{o11}. The output capacitor C_O and the output equivalent impedance $r_{OP1} // R_L$ form the second pole. C_{C1} and R_{C1} form an adaptive zero with a load current to maintain enough phase margin. Furthermore, the output impedance of the buffer stage

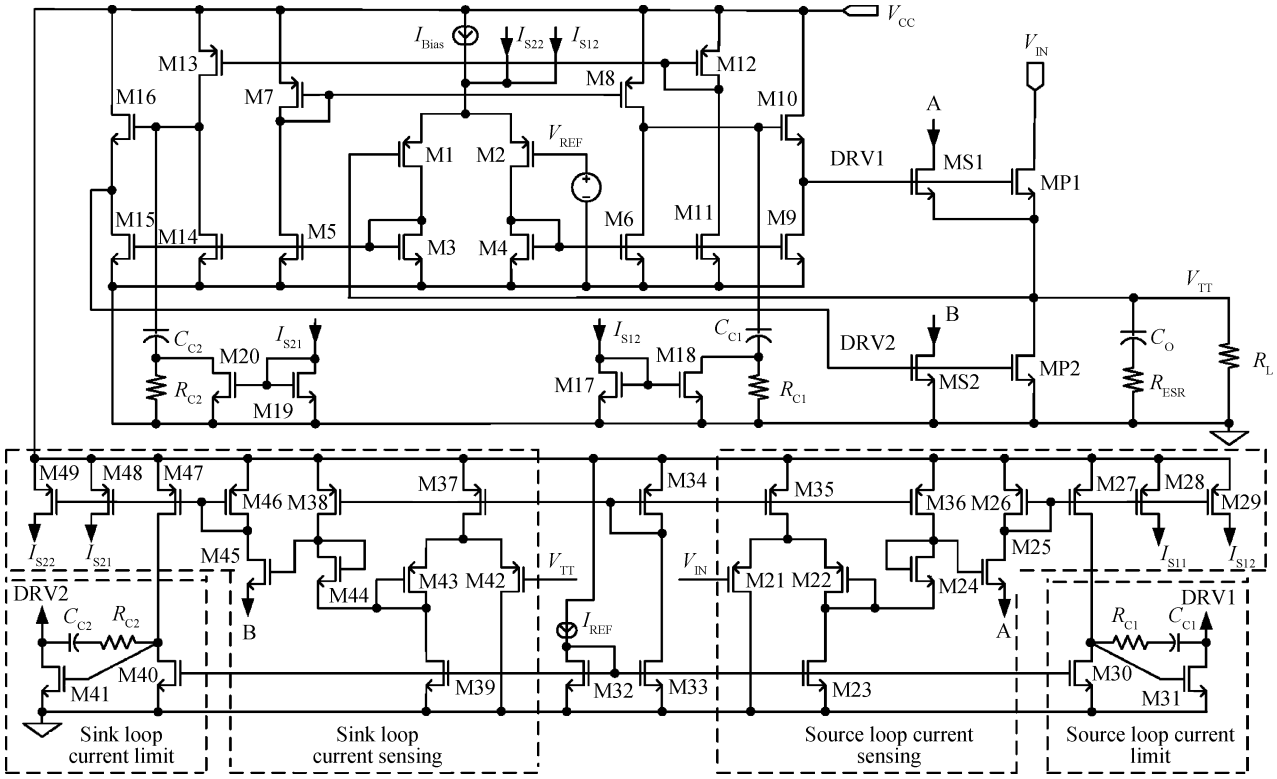

Fig. 3. Source-sink linear regulator circuit.

and capacitor C_{P12} create a pole at high frequency which is pushed outside the unity-gain frequency (UGF) by the lower output impedance. Based on the above analysis, the open-loop transfer function of the source loop can be expressed as

$$H(S) = g_{m(EA)} r_{O11} g_{mP1} r_{OP1} (1 + sR_{C1}C_{C1})(1 + sR_{ESR}C_O) \times \{(1 + sr_{O11}C_{C1})[1 + s(r_{OP1}//R_L)C_O](1 + sC_{P12}/g_{m12})\}^{-1}, \quad (1)$$

where $g_{m(EA)}$, g_{mp1} are the transconductance of the error amplifier stage and the pass transistor; r_{o11}, r_{o12}, and r_{oP1} are the output impedance of first gain stage, second gain stage, and the pass transistor, respectively; C_{C1} and C_{P12} are the node capacitors of the first stage and second stage; R_{ESR} is the equivalent series resistance (ESR) of the output capacitor and R_L is the loading resistance. From Eq. (1), the poles and zeros can be described as

$$\begin{cases} P_1 = \dfrac{1}{r_{O11}C_{C1}}, \\ P_2 = \dfrac{1}{(r_{OP1}//R_L)C_O}, \\ \quad = \left[\sqrt{2\mu_n C_{OX}\left(\dfrac{W}{L}\right)_{MP1} I_L} + \dfrac{1}{R_L}\right]/C_O, \\ P_3 = g_{m12}/C_{P12}, \\ Z_1 = 1/(r_{O11}C_{C1}), \\ Z_2 = 1/(R_{ESR}C_O), \end{cases} \quad (2)$$

where I_L represents the load current. P_2 is a pole related to the load current which is at relatively high frequency with a heavy load, while is at relatively low frequency with light load. The buffer stage is utilized to push P_2 outside UGF, thus the compensation zero produced by the output capacitor's ESR is not necessary. So the system loop only has two poles and one zero before UFG which ensures that the system loop is stable.

The sink loop is similar to the source loop, and then its open-loop transfer function can be expressed as

$$H(S) = g_{m(EA)} r_{O21} g_{mP2} r_{OP2} (1 + sR_{C2}C_{C2})(1 + sR_{ESR}C_O) \times \{(1 + sr_{O21}C_{C2})[1 + s(r_{OP2}//R_L)C_O](1 + sC_{P22}/g_{m22})\}^{-1}. \quad (3)$$

From Eq. (3), the poles and zeros can be described as

$$\begin{cases} P_1 = \dfrac{1}{r_{O21}C_{C2}}, \\ P_2 = \dfrac{1}{(r_{OP2}//R_L)C_L} = \left(\lambda I_L + \dfrac{1}{R_L}\right)/C_L, \\ P_3 = g_{m22}/C_{P22}, \\ Z_1 = 1/(r_{O21}C_{C2}), \\ Z_2 = 1/(R_{ESR}C_O). \end{cases} \quad (4)$$

4. Circuit design

Figure 3 gives the actual circuit of the proposed linear regulator. M1–M8 comprise the operational transconductance amplifier (OTA) in the source loop, and M1–M4, M11–M14 comprise the OTA in the sink loop. M9, M10, M15 and M16 form the buffered stage to drive the gate of the pass transistor in the source and sink loops. Taking into account the poor current

capacity of a PMOS transistor, especially in low supply voltage, NMOS pass transistors are selected in the source and sink loop. In the source loop, the NMOS transistor also provides a faster response speed than the PMOS due to its low output impedance.

MS1, M21–M29, M35, and M36 comprise the load current sensing circuit in the source loop. In order to weaken the impact on current sensing caused by the effect of channel length modulation, $V_{\rm TTIN}$ is transferred to the drain of the sensing transistor through two NMOS $V_{\rm GS}$ and a single stage follower formed by M21–M23. The simulation results show that VTTIN voltage can be followed to the drain of MS1 within 200 mV, whose impact on current sensing can be neglected. Similar to the source loop, MS1, M37–M39 and M42–M49 comprise the load current sensing circuit in the sink loop. Furthermore, the load current sensing circuit can still work well even at low input and output voltage.

The current sensing circuit has three functions. First, it is used to realize output current limiting. Second, it forms adaptive frequency compensation to eliminate the effect on loop stability caused by load current variation. Third, it provides a dynamic bias current corresponding to the load current to enhance the loop's response speed.

M27, M30, M31, $C_{\rm CS1}$, and $R_{\rm CS1}$ form the current limit circuit of the source loop. The load sensing current and the reference current is compared through M27 and M30, and the voltage of pass transistor's gate is regulated by M31. In case of overloading, the pass transistor will be current modulated by the current limit loop. $C_{\rm CS1}$ is a Miller compensation capacitor of the common source stage which is introduced to cancel the right half plane (RHP) zero in M31. The current limit circuit of the sink loop is similar to the source loop and is comprised by M47, M40, M41, $C_{\rm CS2}$, and $R_{\rm CS2}$.

In the regulator system, load current variation may have bad influence on the loop stability. In the proposed linear regulator, the problem has been effectively resolved by creating adaptive zero compensation varying with load current. As shown in Fig. 3, M18 and M20 operate in the deep triode region and the on-resistance of M18 is approximated to be

$$R_{\rm DS(M18)} = \frac{1}{\mu_{\rm n} C_{\rm OX}\left(\dfrac{W}{L}\right)_{\rm M18}(V_{\rm GS}-V_{\rm TH})} = \frac{1}{\sqrt{2k_1^2\mu_{\rm n}C_{\rm OX}\left(\dfrac{W}{L}\right)_{\rm M17} I_{\rm D(M17)}}}, \quad (5)$$

where $k_1 = [(\frac{W}{L})_{\rm M18}]/[(\frac{W}{L})_{\rm M17}]$. Actually, the current $I_{\rm D(M17)}$ is the sensing current, and it can be written as

$$I_{\rm D(M17)} = k_2 I_{\rm L}. \quad (6)$$

Substituting it into Eq. (5), we get the following equation

$$R_{\rm DS(M18)} = \frac{1}{\sqrt{2k_1^2\mu_{\rm n}C_{\rm OX}\left(\dfrac{W}{L}\right)_{\rm M17} I_{\rm L}}} = \frac{k}{\sqrt{I_{\rm L}}}, \quad (7)$$

where $k = \frac{1}{\sqrt{2k_1^2\mu_{\rm n}C_{\rm OX}(\frac{W}{L})_{\rm M17}}}$. Equation (7) illustrates that the on-resistance of M18 is inversely proportional to the square root of load current. Thus the adaptive zero formed by $C_{\rm C1}$ and $R_{\rm C1}$ can be described as

$$Z_1 = \frac{1}{(R_{\rm C1}//R_{\rm DS(M18)})C_{\rm C1}}. \quad (8)$$

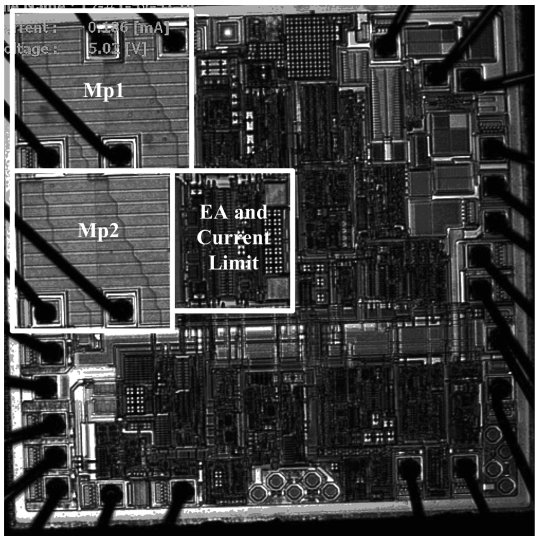

Fig. 4. Micrograph of the proposed linear regulator.

In the same way, we can obtain the adaptive compensation equations in the sink loop as follows

$$\begin{cases} R_{\rm DS(M20)} = \dfrac{k'}{\sqrt{I_{\rm L}}}, \\ Z_2 = \dfrac{1}{(R_{\rm C2}//R_{\rm DS(M20)})C_{\rm C2}}, \end{cases} \quad (9)$$

where k' can be considered as a constant which is similar to k in Eq. (7). Actually, $R_{\rm C1}$ and $R_{\rm C2}$ can be adjusted to optimize adaptive frequency compensation.

The output stage of the sink-source regulator is equivalent to class AB operational amplifier topology. So control of the output stage DC current is critically important[13, 14]. As is presented in Fig. 3, in order to ensure that MP1 and MP2 do not work simultaneously, there must be a DC bias offset voltage at the two-output stage of the OTA. The forced DC bias offset voltage must be controllable and relatively fixed. In the proposed design, the fixed offset voltage is gained by changing the proportion of the OTA's current mirrors. Depended on the matching of current mirrors, this method is relatively reliable. To achieve this, we may set the ratio of the OTA's current mirrors as below

$$\frac{\left(\dfrac{W}{L}\right)_{\rm M6}}{\left(\dfrac{W}{L}\right)_{\rm M4}} > \frac{\left(\dfrac{W}{L}\right)_{\rm M8}}{\left(\dfrac{W}{L}\right)_{\rm M7}}, \quad \frac{\left(\dfrac{W}{L}\right)_{\rm M14}}{\left(\dfrac{W}{L}\right)_{\rm M3}} > \frac{\left(\dfrac{W}{L}\right)_{\rm M13}}{\left(\dfrac{W}{L}\right)_{\rm M12}}. \quad (10)$$

The currents in M6 and M14 are bigger than that in M8 and M13. In balanced state, the mismatch in OTA's current mirrors will produce an offset voltage at differential input. Only when the input error voltage rises to a certain level, can the pass transistor be turned on. In the actual circuit, the ratio of the OTA's current mirrors is designed as

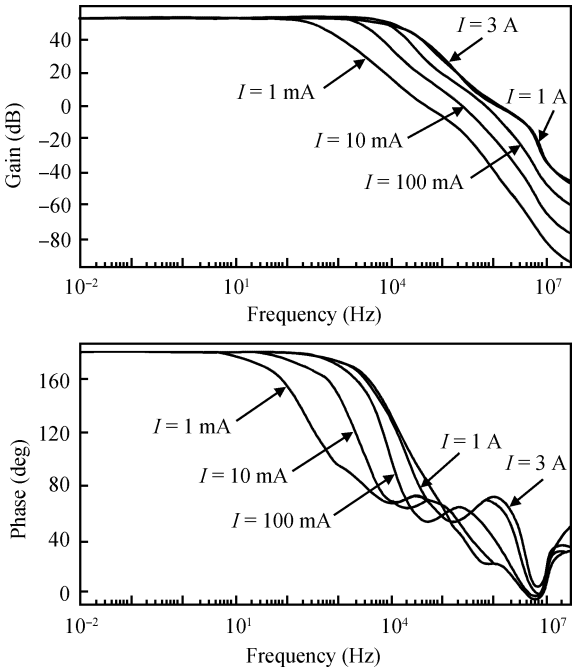

Fig. 5. Frequency response of the source loop.

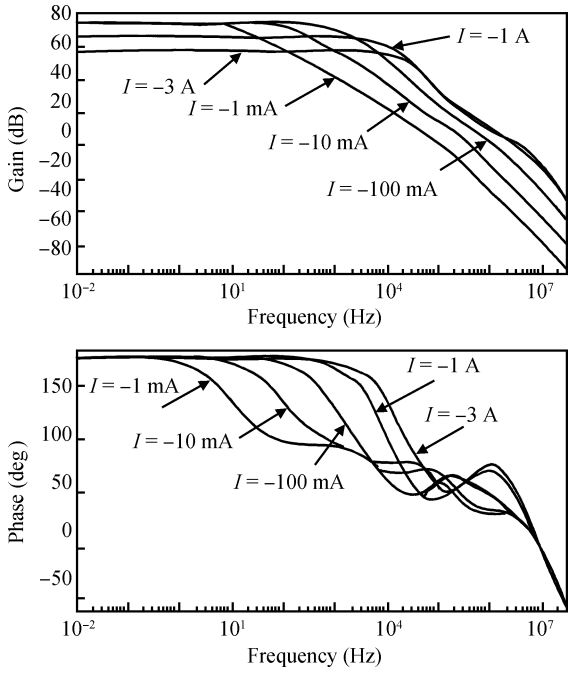

Fig. 6. Frequency response of the sink loop.

$$\frac{\left(\frac{W}{L}\right)_{M6}}{\left(\frac{W}{L}\right)_{M4}} : \frac{\left(\frac{W}{L}\right)_{M8}}{\left(\frac{W}{L}\right)_{M7}} = \frac{\left(\frac{W}{L}\right)_{M14}}{\left(\frac{W}{L}\right)_{M3}} : \frac{\left(\frac{W}{L}\right)_{M13}}{\left(\frac{W}{L}\right)_{M12}} = 40 : 38. \tag{11}$$

The offset current in OTA's current mirrors is about 2 μA, and the impedance of the output stage is nearly 500 kΩ. So the offset voltage at the output stage is approximately is 1 V. Furthermore, the OTA gain is 500, thus the equivalent input offset voltage is ±5 mV.

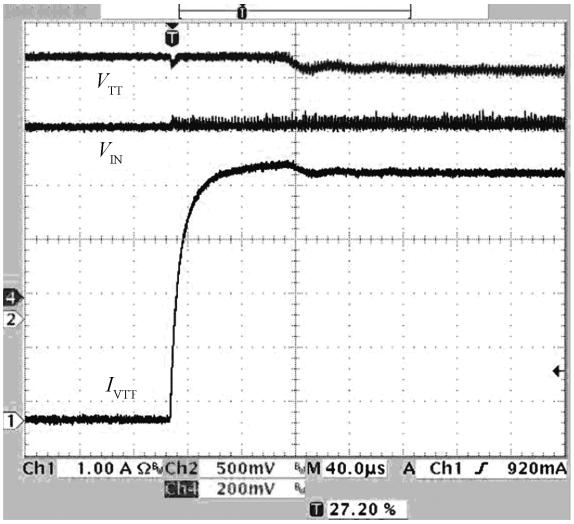

Fig. 7. Source loop current limit tested waveform.

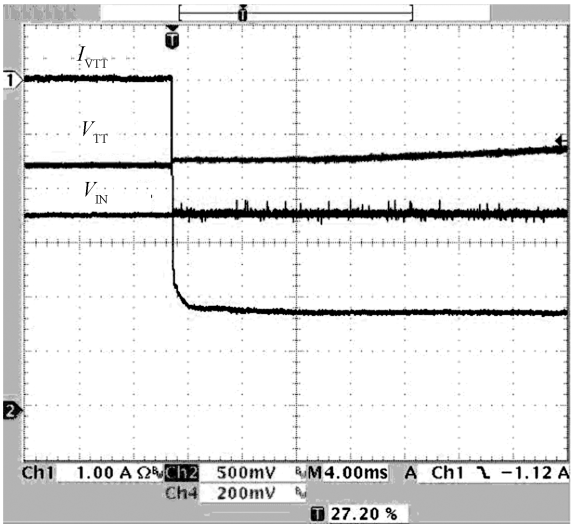

Fig. 8. Sink loop current limit tested waveform.

5. Design realization and experimental results

The presented linear regulator with 3-A source-sink current capacity has been integrated into a DDR memory power management IC with 0.6-μm 30 V BCD process successfully. Figure 4 shows the micrograph of the proposed regulator. The total area size is about 1 mm^2. The white frames indicate the location of two pass transistors, the error amplifier, and the current limit circuit in the layout.

In the testing and verification, the following parameters are used unless otherwise stated: V_{CC} = 5 V, V_{IN} = 1.8 V, V_{TT} = 0.9 V, C_{IN} = 10 μF, C_{OUT} = 20 μF. Frequency responses of the source and sink loops with different loads are shown in Figs. 5 and 6. The simulation results show that both the source and sink loops maintain the UGF between 70 to 800 kHz and the phase margin is about 60 degrees or more with the load ranging between 1 mA and 3 A. Figures 7 and 8 give the test waveforms of the current limit circuit in source and sink loops,

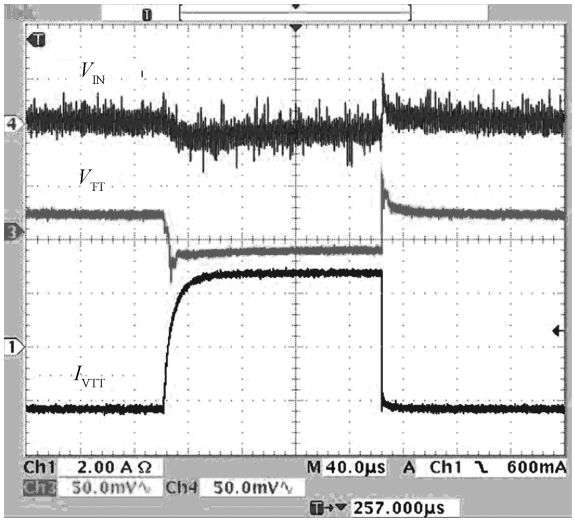

Fig. 9. Load transient response.

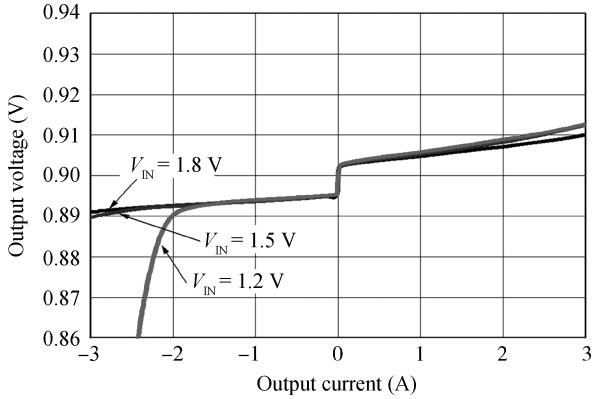

Fig. 10. Output voltage versus load current.

which shows the current is restricted at nearly 4.3 A and the current limiting response is stable. Figure 9 shows the waves of load transient response. The maximum over-shoot voltage variation is less than 30 mV with 2.5 A sink current steps to 2.5 A source current in 1 μs with 20 μF output capacitor.

Figure 10 illustrates the load regulation performance with 0.9 V output voltage and 1.8 V, 1.5 V, 1.2 V input voltages, respectively. From the data curve, it can be see that the offset voltage with no load is about $\pm$5 mV and the load regulation is about 10 mV/A. In addition, when the loading is over 2 A, the output voltage of source loop with 1.2 V input rapidly decreases, which is caused by the drop-out voltage limit. Figure 11 gives the curve of ground current versus load current. It is observed that the quiescent current is linearly increased with the increase of load current. The minimum value is about 350 μA at no load and the maximum is about 1 mA at 3-A load.

6. Conclusion

A linear regulator applicable to the bus terminal supply with high response speed and 3-A source-sink current ability has been designed and implemented. The use of an NMOS pass transistor not only guarantees output current capacity with low input voltage, but also improves the response speed of the regulator. The load current feedback technique and adaptive zero

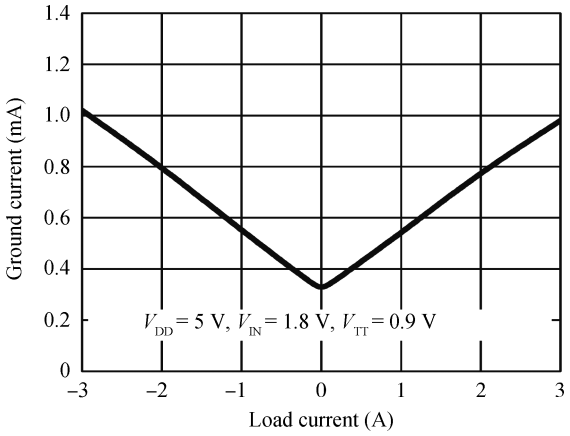

Fig. 11. Ground current versus load current.

compensation realizes loop stability over the whole load range for either the source or sink loop. In addition, the transconductance matching technique solves the conflict between the DC current of the output stage and the intrinsic offset voltage of the input stage. This regulator has already been integrated in a DDR memory power management IC and been fabricated with 0.6-μm 30 V BCD process successfully. Test results show that the variation of output voltage is less than $\pm$15 mV at the load range of $\pm$3 A, the offset voltage is approximately $\pm$5 mV, and that DC current of the output stage is less than 3 μA. Moreover, the maximum transient output voltage is within $\pm$30 mV with load step changes of $\pm$2 A.

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