A single-event-hardened phase-locked loop using the radiation-hardened-by-design technique*

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Abstract: A radiation-hardened-by-design phase-locked loop (PLL) with a frequency range of 200 to 1000 MHz is proposed. By presenting a novel charge compensation circuit, composed by a lock detector circuit, two operational amplifiers, and four MOS devices, the proposed PLL significantly reduces the recovery time after the presence of a single event transient (SET). Comparing with many traditional hardened methods, most of which endeavor to enhance the immunity of the charge pump output node to an SET, the novel PLL can also decrease its susceptibility in the presence of an SET in other blocks. A novel system model is presented to describe immunity of a PLL to an SET and used to compare the sensitivity of traditional and hardened PLLs to an SET. An SET is simulated on Sentaurus TCAD simulation workbench to model the induced pulse current. Post simulation with a 130 nm CMOS process model shows that the recovery time of the proposed PLL reduces by up to 93.5% compared with the traditional one, at the same time, the charge compensation circuit adds no complexity to the systemic parameter design.

Key words: phase-locked-loop; single event effect; SET; hardened by design; charge compensation

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1. Introduction

The phase-locked loop (PLL) is one of the most important blocks in a modern electronic system and is widely used in radio frequency transceivers, microprocessors, and DSPs. During the past several decades, the PLL has witnessed great developments. However, with the development of space technology and the ever-increasing demands on the reliability of electronic systems operating in complex electromagnetic environments, a PLL's immunity to radiation has become a current research focus.

In the past several years, many ideas have been proposed to mitigate SETs in a charge pump (CP). For instance, wider bandwidth PLLs are adopted in Ref. [1] to recover faster from loss of lock due to SET, but phase noise and system stability make this method very difficult to implement or are even impractical. Alternatively, a tri-state voltage-based charge pump (V-CP) has been developed in Refs. [2, 3], the basic idea behind this method is to increase the rate of charge sourcing and sinking and provide a mechanism to isolate the vulnerable nodes from the single-event (SE) sensitive capacitive nodes of the low pass filter (LPF). However, the dependence of current magnitude on the voltage on the LPF capacitors results in a non-linear response in the acquisition process. The large initial current also may cause voltage spikes in the power supply, so care must be taken to ensure safe operation against it. Reference [4] proposed a complementary current limiter circuit to compensate current when a single event strikes on the output node of a CP, however, the width of pulse current induced by a single event is approximately 100 ps, therefore, in order to detect the pulse current, the bandwidth of the operational amplifier (OP) must be higher than 10 GHz. In fact, OPs with such wide bandwidth are very difficult to design in modern prevalent 130 nm or 90 nm technology.

The idea proposed in this paper is based on the action of pulse current on LPF. By analyzing the action of pulse current induced by an SET on an LPF, it is found that the voltage difference between the top plates of C_1 and C_2 (which can be seen from Fig. 2 in the following section) can last for a relative longer period compared with the width of the SET. Therefore, it can be easily detected by the charge compensation circuit, and then the charge compensation circuit quickly compensates charge to the LPF until the voltage on the LPF recovers to its original value.

2. Single-event transient analysis and impact on the PLL

2.1. Single-event transient analysis

When high energy ionizing particles, protons or heavy ions, penetrate into semiconductor material, they lose energy and produce electron–hole pairs, which are collected under an inner electric field, resulting in a current pulse. As the feature size of process is ever-decreasing, the node capacitance of mixed-signal integrated circuits continues to decrease. Logic states in digital circuits can easily be inversed, and an SET can severely interfere with an analog signal. Therefore, for electronic systems operating in space and military environment, single-event effects have become a primary concern. Figure 1 shows the carrier distribution in an NMOS device (cross sec-

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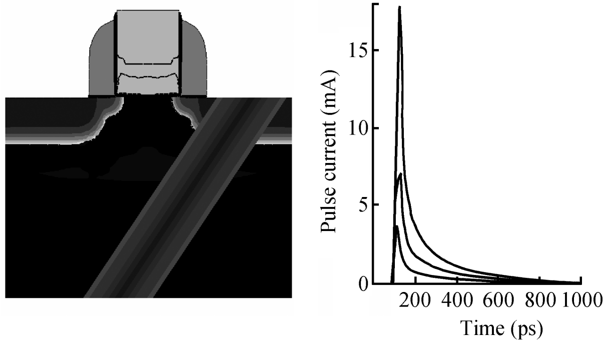

Fig. 1. Carrier distribution in an NMOS device diagram and induced pulse current in the presence of an SET on a drain.

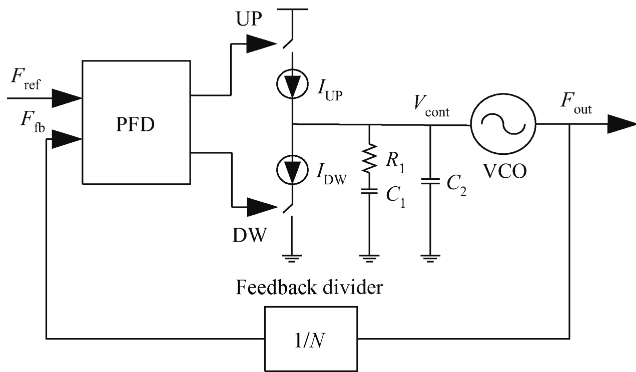

Fig. 2. Block diagram of conventional CPPLL.

tion of a 3-D device) and the induced current pulse in the presence of an SET on the drain, which are obtained from Sentaurus TCAD simulation, for the LET value of 20 MeV·cm^2/mg, 40 MeV·cm^2/mg, and 80 MeV·cm^2/mg, respectively. It is concluded from above analysis that an SET can be modeled as a double exponential current pulse in SPICE simulation[5].

2.2. Impact of an SET on a PLL

A typical PLL consists of five major blocks: phase frequency detector (PFD), charge pump (CP), loop pass filter (LPF), voltage-controlled oscillator (VCO), and frequency divider (FD), as shown in Fig. 2. The output of the FD, F_{fb}, is compared with F_{ref} in the PFD, generating an error signal equal to the phase difference between F_{fb} and F_{ref}, then a current proportional to the error signal is generated by the CP and integrated through the LPF, converting the phase error signal to control voltage, which is used to modulate the output frequency of the VCO, generating the desired frequency.

Previous literatures point out that the charge pump is the most sensitive module to an SET, which may result in at least two orders of magnitude higher output phase displacement than other modules in a PLL[2, 6–8]. As a high energy ionizing particle strikes in the CP, some quantity of charge is collected and a current pulse is induced, the quantity of collected charge depends on the energy of particles and semiconductor material, and so does the amplitude of the induced current pulse. As shown in Fig. 2, the LPF is consisted of two capacitors and a resistor. In order to ensure stability of the PLL system, the value of C_1 is set more than 20 times larger than that of C_2, and

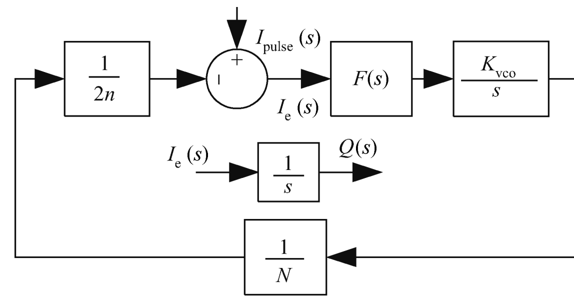

Fig. 3. Proposed model diagram describing the transfer function of the pulse current to charge accumulated on the LPF.

the value of R_1 is always several kilohms or larger, depending on C_1 and system parameters. Therefore, when a single event strikes on the output node of the CP, the induced pulse current charges or discharges C_2 first, because C_2 is always small, about several pF, and there is no resistor connects with it. These collected charge acting on the LPF will induce relatively larger voltage disturbance on the control line of the VCO, resulting in the loss of lock of the PLL.

Actually, the PLL will gradually recover through self loop feedback after lock loss. The recovery time depends on the system bandwidth and the maximum accumulated quantity of charge on the LPF. Fundamentally speaking, the recovery process is a charge compensation process. When the LPF is charged or discharges a certain quantity of charge by a single event, the feedback loop begins to compensate charge until the extra charge on the LPF collected when there has been an SET disappear. Then the VCO returns to its initial frequency.

2.3. Modeling of an SET in a PLL

It is pointed out in Section 2.2 that as a high energy ionizing particle strikes in the CP, some quantity of charge is collected, which accumulate on the LPF and disturb V_{ctrl}. Therefore, the quantity of the accumulated charge directly affects the immunity of a PLL to an SET. Based on above consideration, a novel model which describes the transfer function from pulse current to accumulated charge is proposed. Figure 3 is the proposed model diagram. It is can be seen from the diagram that the proposed model not only includes models of VCO, FD, CP, and LPF, but also includes a integration factor, which converts current to charge quantity. For traditional PLLs, the LPF consists of R_1, C_1, and C_2, as shown in Fig. 2. Equation (1) is the transfer function.

$$\begin{aligned}H(s) = \frac{Q(s)}{I(s)} &= \frac{1}{1+\dfrac{K_{\rm VCO}}{s}\dfrac{I_{\rm cp}}{2\pi}\dfrac{1}{N}F(s)}\frac{1}{s} \\ &= \left[R_1C_1C_2s^2+(C_1+C_2)s\right] \\ &\quad\times\Bigg[R_1C_1C_2s^3+(C_1+C_2)s^2 \\ &\quad+\left(\frac{I_{\rm cp}K_{\rm VCO}R_1C_1}{2\pi}+1\right)s+\frac{I_{\rm cp}K_{\rm VCO}}{2\pi}\Bigg]^{-1}. \quad (1)\end{aligned}$$

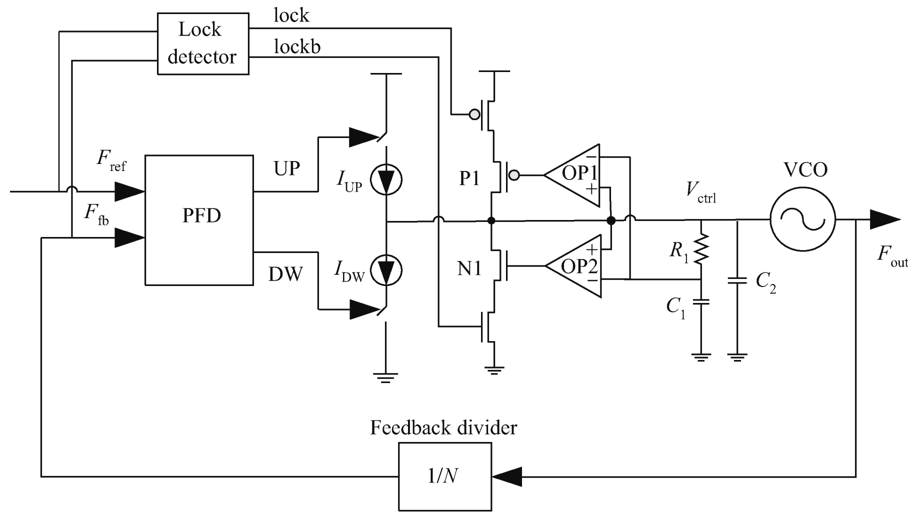

Fig. 4. Block diagram of the proposed CPPLL.

3. Proposed idea and circuit description

3.1. Basic idea of the proposed PLL

It is known from the above analysis that as high energy ionizing particles strike the CP, the induced pulse current charges C_2 first, converting current pulse into voltage on the C_2 top plate. In this paper, the values of R_1, C_1, and C_2 are 28 kΩ, 300 pF, and 15 pF, respectively. So the time constant of R_1C_1 is 8.4 μs, compared with the pulse current width, this time is very long, therefore, during the charging process, the voltage on the top plate of C_1 can be regarded as constant. Now, the voltage on the top of C_2 is charged to a certain value, while the voltage on the top plate of C_1 keeps its initial value. So an OP can be used to detect the voltage difference between C_1 and C_2, and pull the disturbed voltage on C_2 back to its initial value. Considering 1/200 of the time constant, which is 42 ns, an OP with 24 MHz is adequate to detect the voltage difference, compared with Ref. [4], this gives a great relaxation on the design of OP.

3.2. Circuit description of the proposed PLL

Figure 4 is block diagram of the proposed PLL, compared with conventional one, the proposed PLL adds a lock detector circuit, two OPs and four MOS devices. The DC offset voltage of the two OPs is set to ±5 mV and the delay time of the lock detector is set as 1 μs. During the PLL start phase, the lock detector determines if the system is out of lock. The logic states of lock and lockb are 1 and 0, respectively. If the charge compensation circuit is disconnected, the feedback loop starts in a normal way. When the time difference between the rising edges of F_{ref} and F_{fb} is less than 50 ps, the lock detector determines that the system is locked. The logic states of lock and lockb are 0 and 1, respectively in this design, and the voltage magnitude of ripple on the V_{ctrl} is no more than 1 mV when the system is locked. Therefore, the outputs of OP1 and OP2 are high and low, respectively, so the charging and discharging branch of the compensation circuit is also disconnected. When a positive pulse current injects on the LPF, if the disturbance voltage on C_2 is larger than 5 mV, in this paper the corresponding a single event with LET lager than 7 MeV·cm^2/mg, OP1 will turn on N1 to discharge the charge on C_2 induced by positive pulse current. If there is a negative pulse current, OP2 will turn P1 to compensate charge on C_2. The delay time of the lock detector is set to 1 μs because the following simulation shows that the recovery time of the system is no more than 1 μs, so during this delay time the PLL can recover completely.

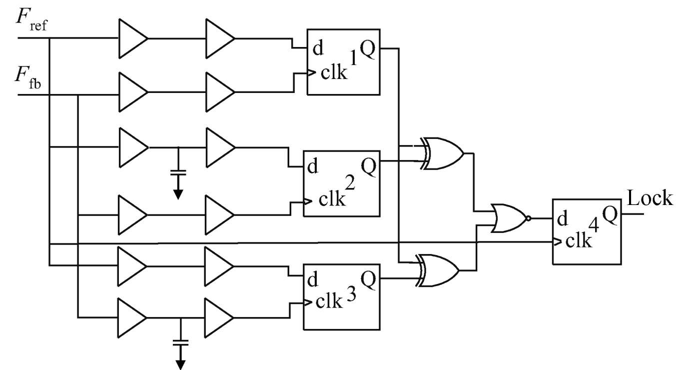

Fig. 5. Circuit of the lock detector.

Figure 5 is the lock detector circuit used in the proposed PLL. There are two different delay branches from F_{ref}/F_{fb} to the DFFs, two branches with a capacitor and four without a capacitor. The delay of every buffer in the branches is set 0.5 μs, and the delay difference between the two different delay branches is 50 ps. When the time difference between the rising edges of F_{ref} and F_{fb} is longer than 50 ps, the outputs of the three DFFs have the same state, logic 0 or 1, depending on which signal is leading. Then the output of NOR gate is logic 1. When the time difference between the rising edges of F_{ref} and F_{fb} is within 50 ps, the outputs of the second and the third DFF have the opposite logic state, no matter what the output state of the first DFF is, then the output of the NOR gate is logic 0, and the output of NOR is sampled by DFF4, which determines whether the system is locked is not. Compared with the lock detector proposed in Ref. [9], this lock detector adds DFF4 and eliminates misjudgement during the start of the system.

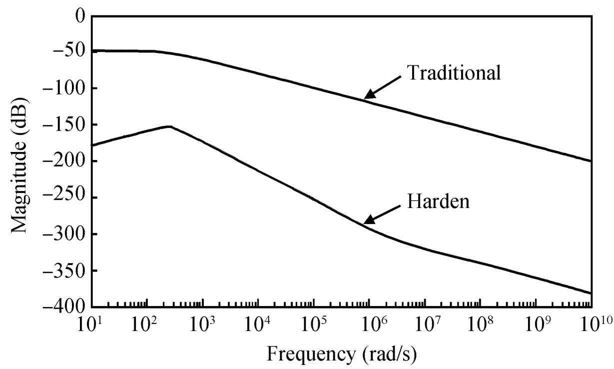

Fig. 6. Magnitude–frequency curve of hardened and traditional PLL charge transfer function.

3.3. System-level analysis of the SET in a hardened PLL

For the hardened PLL proposed in this paper, the LPF is modeled by R_1, C_1, C_2, and R_p. Here, R_p is used to model N1 or P1 in Fig. 4. It can be understood as follows, N1 or P1 is substituted by Rp because it provides a discharging or charging loop when a single event strikes on the CP output node. It should be declared that this model is only suitable when a single event strikes the CP. During normal operation, the model diagrams of hardened and traditional PLLs are same because the charging and discharging loops are disconnected. Equation (2) is the transfer function of the hardened PLL when a single event strikes the CP. Substituting system parameters into Eqs. (1) and (2), the magnitude–frequency curve of the charge transfer function can be obtained, as shown in Fig. 6. It can be seen that the accumulated charge on the LPF of a hardened PLL is greatly reduced when a single event strikes a CP compared with a traditional one. It is also illuminated that the immunity of the proposed PLL to SET is considerably increased.

$$\begin{aligned} H(s) &= \frac{Q(s)}{I(s)} = \frac{1}{1+\dfrac{K_\mathrm{VCO}}{s}\dfrac{I_\mathrm{cp}}{2\pi}\dfrac{1}{N}F(s)}\frac{1}{s} \\ &= \left[R_\mathrm{P}R_1C_1C_2s^2 + (R_\mathrm{P}C_1 + R_\mathrm{P}C_2 + R_1C_1)s + 1\right] \\ &\quad\times\left[R_\mathrm{P}R_1C_1C_2s^3 + (R_\mathrm{P}C_1 + R_PC_2 + R_1C_1)s^2\right. \\ &\quad\left.+\left(\frac{I_\mathrm{cp}K_\mathrm{VCO}R_\mathrm{P}R_1C_1}{2\pi}+1\right)s + \frac{I_\mathrm{cp}K_\mathrm{VCO}R_\mathrm{P}}{2\pi}\right]^{-1}. \end{aligned} \tag{2}$$

4. Simulation and results analysis

4.1. Simulation setup

First, a 130 nm NMOS device is constructed on a Sentaurus TCAD simulation workbench, then ions with different LET values, 20 MeV·cm^2/mg, 40 MeV·cm^2/mg, 80 MeV·cm^2/mg, strike the device's sensitive node (drain), respectively, and three different pulse currents are obtained. A double exponential current pulse is constructed according to the obtained pulse current to model the SET, which is used in the schematic simulation.

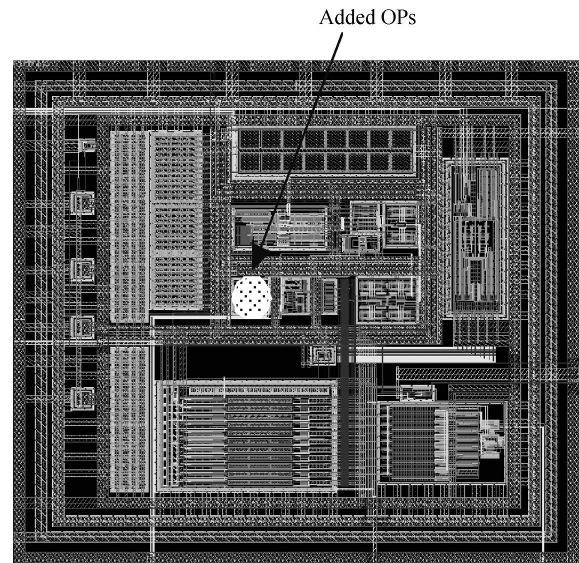

Fig. 7. Layout of the proposed PLL.

Layouts of two PLLs (conventional and proposed) were designed in a 130 nm CMOS process to confirm the expected effects. Figure 7 shows the layout of the proposed PLL, it can be seen that the added OPs used for charge compensation occupy a small layout area. Post simulations were performed on each individual by using a Synopsys HSPICE simulator. After the PLL was locked, the double exponential current pulse was injected into the sensitive node, the output of CP. For a single event with different LET values, the traditional and hardened PLLs were simulated three times, respectively. The recovery time for all cases were recorded. To simulate the enhanced immunity of other blocks in the PLL system to SET, a pulse current was placed on the output of one delay cell in the VCO.

4.2. Simulation results and analysis

Simulation results show that the hardened PLL can considerably reduce recovery time of the system after a single event pulse current. It can be seen from Fig. 8 that the recovery time of traditional and proposed PLLs after being struck on the CP output node by a single event with an LET value of 20 MeV·cm^2/mg is 5.37 μs and 0.68 μs, respectively, resulting in approximate 88.4% improvement. Figure 8 also shows the frequency variation of PLL in the presence of an SET on the CP output node. The recovery time required by different LET single events is recorded in Table 1. It can be seen from the table that with the increase of LET value, the recovery time of both PLL is increased. However, the increased time required by a traditional PLL is quite longer than that of a hardened PLL, which illuminates that the enhanced immunity of the proposed PLL to SET becomes more obvious with the increase of LET value, and the improvements are about 92.2% and 93.5%, respectively. Simulations also show that when a single event with an LET value of 80 MeV·cm^2/mg strikes on the VCO, the resultant disturbance of V_ctrl and its recovery time are both decreased, which also illuminates that the CP is the most sensitive block to an SET in a PLL. Nevertheless, the recovery

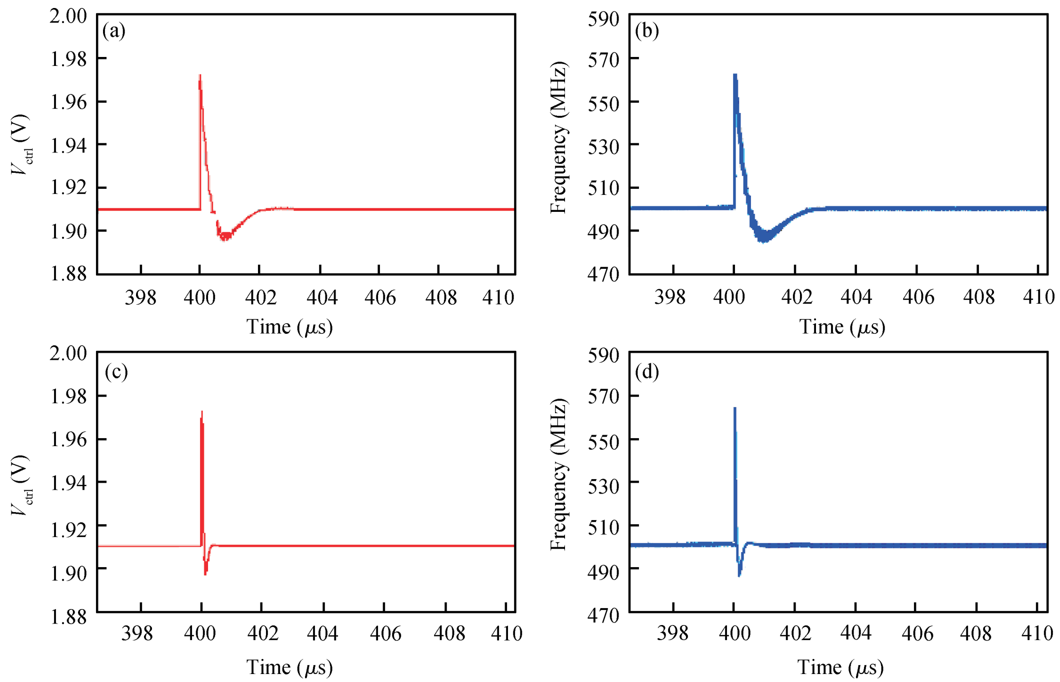

Fig. 8. (a) Variation of V_{ctrl} after a single event strikes in a traditional CP. (b) Variation of frequency after a single event strikes in a traditional CP. (c)Variation of V_{ctrl} after a single event strikes in the proposed CP. (d) Variation of frequency after a single event strikes in the proposed CP.

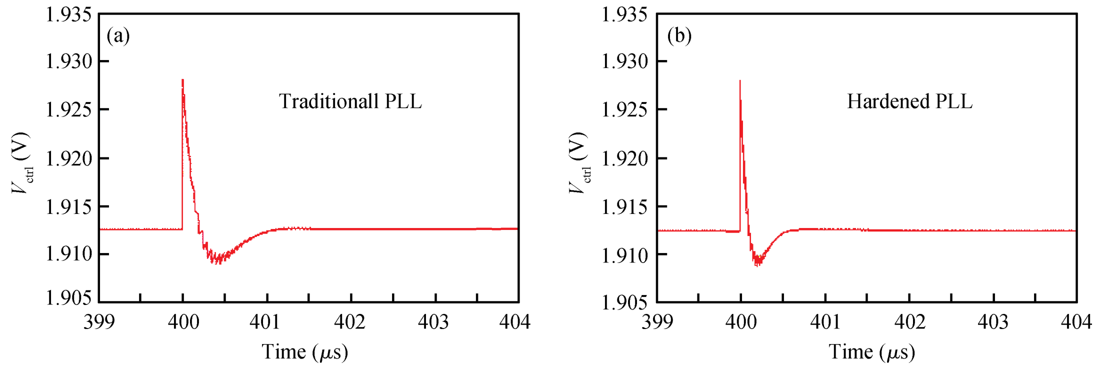

Fig. 9. (a) Variation of V_{ctrl} after a single event strikes in the VCO. (b) Variation of V_{ctrl} after a single event strikes in the VCO.

time reduces from 1.9 μs (traditional PLL) to 0.99 μs (hardened PLL), an approximatly 47.9% improvement, as shown in Fig. 9.

The sensitivity of the added circuit to SET is analyzed and simulated as follows. First, lock and lockb are insensitive to an SET, considering the worst case, when lock or lockb is upset by an SE, resulting in the corresponding switch to turn off, there is no effect on the normal operation of the PLL, because during the locked state, P1 and N1 are also turned off by OP1 and OP2. Second, research shows that the most sensitive nodes of the added circuit are the outputs of OP1 and OP2. We take the output of OP1 as an example and an SET simulation is performed. Figure 10 shows the variation of V_{ctrl} when an SE with an LET of 80 MeV·cm^2/mg strikes on output of OP1, the recovery time is approximately 50 ns. Compared to when a SE strikes on the output of the CP, the recovery time is dramatically reduced. This is because, on one hand, the transistor size is large, the voltage of OP1 output can be quickly driven back to its original level, on the other hand, even if the output voltage of OP1 changes by a large value, the charge compensation circuit itself can also effectively exert its function, providing

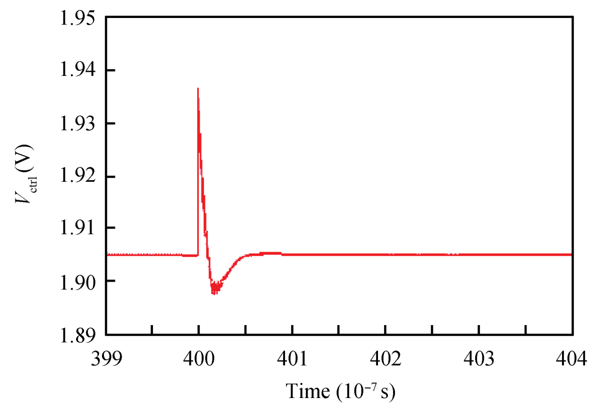

Fig. 10. Variation of V_{ctrl} after a single event strikes in the output of OP1.

Table 1. Recovery time of both PLLs after an SET with different LET value strikes on the CP output.

LET	Time (μs)	
	Traditional PLL	Hardened PLL
20 MeV·cm^2/mg	5.37	0.68
40 MeV·cm^2/mg	10.2	0.79
80 MeV·cm^2/mg	14.5	0.93

compensation charge and making system recover quickly. The power expense brought by the added charge compensation circuit is also simulated, the result of which shows that the total power of the traditional PLL and the proposed PLL is 2.93 mW and 3.07 mV, respectively.

All of above obtained improvements result from the charge compensation circuit. For single event strikes on CP, the induced large pulse current injects a mass of charges on the LPF during a very short time, leading to a voltage difference between the inputs of OP1 or OP2, driving N1 or P1 to compensate charge to the LPF. While for single event strikes on the VCO, the induced pulse current can only result in phase error, which is divided by the FD and compared with the reference signal. Then the phase error is converted to current, charging or discharging LPF, therefore, the magnitude of the current is limited by CP. That is why the VCO is relatively insensitive to an SET compared with the CP output node, so does other blocks. Despite this, if the phase error is large enough, it will also cause a disturbance of V_{ctrl} exceeding 5 mV, and force N1 or P1 to discharge or charge the LPF.

5. Conclusion

A novel radiation-hardened-by-design technique for enhancing the immunity of PLLs to SETs has been presented in this paper. By simulating SETs on a Sentaurus TCAD simulation workbench, a series of double exponential current pulses induced by SETs with different LET values are obtained. Through analyzing the actions of the pulse current on the LPF, it is found that during the very short time after an SET, the voltage on C_2 experiences a relatively larger transition because nearly all of those collected charges are injected and integrated on the top plate of C_2, while the voltage on C_1 almost keeps constant. Therefore, two OPs with moderate bandwidth are adequate to detect the voltage difference between C_1 and C_2, combined with four MOS devices and a lock detector circuit, forming charge compensation circuit to improve immunity of PLL to SET.

A novel system model is proposed and used to verify immunity of a PLL system to SETs. Traditional and proposed PLL systems are compared with this model and the improvement is confirmed. Post simulations are performed using 130 nm commercial CMOS process with single event strike represented by double exponential pulse current which is deduced from TCAD simulation. The charge compensation circuit greatly accelerates the re-lock process and reduces the recovery time by up to 93.5% when the strike occurs in the CP. For single event strikes on the VCO, the recovery time is reduced by approximately 47.9%, and all of the simulation results confirm the hardness of the proposed PLL. At the same time, the sensitivity of the added charge compensation circuit to SET is analyzed and simulated, results show that the added circuit is much less sensitive to SETs than the CP, and the recovery time is very short. The added OPs bring a very small area penalty, approximately 1/100 of the total area, while the consumed power is increased from 2.93 to 3.07 mW, illuminating that the extra power consumption induced by charge compensation circuit is very small.

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