A multi-mode multi-band RF receiver front-end for a TD-SCDMA/LTE/LTE-advanced in 0.18-μm CMOS process*

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Abstract: A fully integrated multi-mode multi-band directed-conversion radio frequency (RF) receiver front-end for a TD-SCDMA/LTE/LTE-advanced is presented. The front-end employs direct-conversion design, and consists of two differential tunable low noise amplifiers (LNA), a quadrature mixer, and two intermediate frequency (IF) amplifiers. The two independent tunable LNAs are used to cover all the four frequency bands, achieving sufficient low noise and high gain performance with low power consumption. Switched capacitor arrays perform a resonant frequency point calibration for the LNAs. The two LNAs are combined at the driver stage of the mixer, which employs a folded double balanced Gilbert structure, and utilizes PMOS transistors as local oscillator (LO) switches to reduce flicker noise. The front-end has three gain modes to obtain a higher dynamic range. Frequency band selection and mode of configuration is realized by an on-chip serial peripheral interface (SPI) module. The front-end is fabricated in a TSMC 0.18-μm RF CMOS process and occupies an area of 1.3 mm^2. The measured double-sideband (DSB) noise figure is below 3.5 dB and the conversion gain is over 43 dB at all of the frequency bands. The total current consumption is 31 mA from a 1.8-V supply.

Key words: receiver front-end; low noise amplifier; mixer; multi-mode; multi-band; CMOS
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1. Introduction

During the last decade, mobile communication technology has evolved continuously towards higher data rates and a larger cellular capacity. Currently, cellular systems of the second-generation (2G) and third-generation (3G) coexist in the global market, while research and development have stepped into the fourth-generation (4G) domain, which is defined as International Mobile-Telecommunications Advanced (IMT-Advanced) by the International Telecommunications Union (ITU). This January the ITU officially approved long-term-evolution-advanced (LTE-Advanced) and wireless-MAN-Advanced as the designation for 4G mobile technologies[1]. For China, TD-SCDMA and LTE/LTE-Advanced cellular systems are the focus of application and research. The frequency bands of TD-SCDMA are 1880–1920MHz and 2010–2025 MHz; and for LTE/LTE-Advanced standards, the candidate frequency bands are 2300–2400 MHz, 3400–3600 MHz, and also include TD-SCDMA bands[2]. In current and future applications, it is attractive for mobile terminals to support multiple cellular standards and multiple frequency bands. Thus a multi-mode/multi-band or configurable radio frequency (RF) transceiver is in great demand.

This paper presents a radio frequency receiver front-end for TD-SCDMA, LTE and LTE-Advanced standards. The front-end employs direct-conversion architecture, and consists of two differential tunable low noise amplifiers (LNAs) which cover all four frequency bands, a quadrature mixer, and two intermediate frequency (IF) amplifiers. The front-end has three gain modes to meet the receiver dynamic range requirements. Switched capacitor arrays are used to calibrate resonant frequency points of the LNAs. Selection of frequency band and gain modes and resonant frequency point adjustment are all digitally controlled by an on-chip Serial Peripheral Interface (SPI) module.

2. Design consideration

In a multi-mode/multi-band receiver, chip area and cost are of concern. It is advantageous to share as many building blocks as possible without degrading the system performance. Compared with super heterodyne architecture, the direct conversion receiver has fewer building blocks such as the mixer and voltage controlled oscillator (VCO), and especially does not require an expensive external image-reject filter. It is low cost, low power and flexible, hence it is more suitable for multi-mode/multi-band applications. In a direct conversion receiver, the RF signal is amplified by the LNA, and down converted to the IF signal by a quadrature mixer, then bandwidth-tunable low pass filters (LPF) will perform the channel selection function. In the direct conversion receiver front-end, the mixer can be easily reused, so the key issue is how to design a multi-band LNA.

Generally, there are three types of LNA structure to choose: multiple narrow-band LNAs in parallel, a wideband LNA and a tunable LNA. Narrow band LNA gives the best performance, such as lower power consumption, lower noise figures, and higher gain, and all of the parameters can be optimized independently for each operation mode and frequency band. However, its drawback is also evident, which is that each

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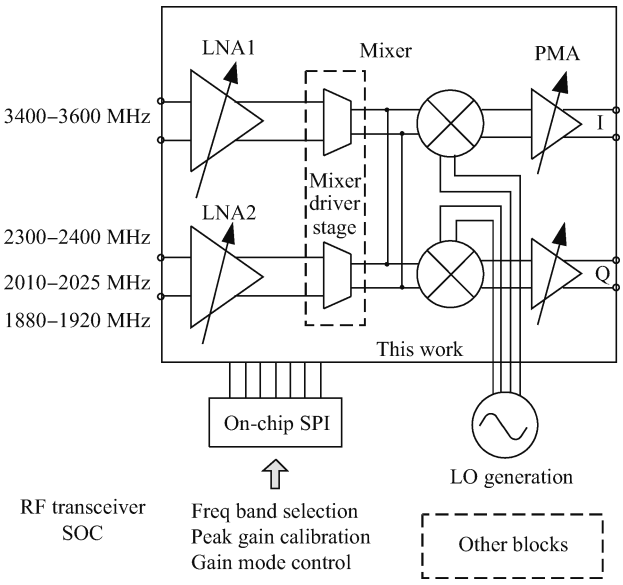

Fig. 1. Block diagram of the proposed RF receiver front-end design.

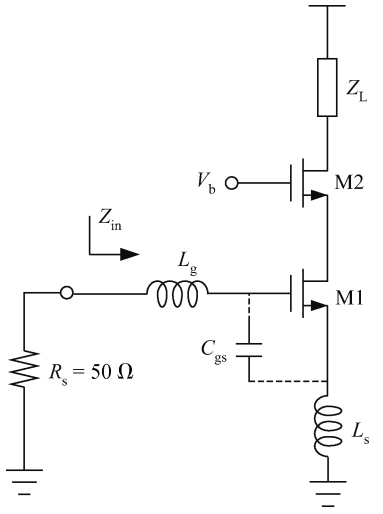

Fig. 2. Structure of the source inductor degenerated LNA.

LNA with several on-chip spiral inductors will take up too much area and increase the cost.

Though a wideband LNA covering all the bands saves costs, it has several disadvantages. Compared with a narrowband LNA, the Q values of the input matching network and load impedance of a wide band LNA are much lower, which degrade gain and noise performance, and increase the power consumption. The wideband LNA fabricated in the CMOS 0.18 μm process is hard to design to meet the NF requirement of cellular application[3–5]. Moreover, because of the wideband characteristics, it is more subject to large in-band interference and thus the linearity requirement is stringent.

Many tunable LNAs for multi-mode/multi-band receivers have been reported. In Ref. [6], the LNA for GSM and WCDMA standards used separated input paths to realize input impedance matching at different bands; cascode transistors combine and switch the signal current, while two load resonant networks comprised of inductor and switched-capacitors perform frequency band selection. But a single-end LNA is sensitive to bond wires; besides, the input gate inductor is not integrated in the chip, so in fact this design does not achieve its purpose of saving area. In Ref. [7], the tunable LNA realized wideband input impedance matched with a feedback transformer, and multi-tap spiral inductor and switched-capacitor LC tank tune the frequency band. However, the transformer and multi-tap inductor are not standard devices offered by a foundry, so careful EM simulation and modeling is required.

The proposed design uses two LNAs covering all the four frequency bands. LNA1 operates at frequency band of 3400–3600 MHz and LNA2 at 1880–2400 MHz. A switch in bias circuit determines the on and off state of the two LNAs, while load impedance networks perform the frequency band selection. This design helps to provide an adequate performance of the NF and gain to meet the cellular system specifications, with low circuit complexity, low power consumption, and moderate chip area. The two LNAs combine in a current mode at the driver stage mixer. It is simpler and better than using switches in the signal path, which will introduce loss. The receiver front-end design is shown in Fig. 1.

3. Circuit design

3.1. Low noise amplifier

The proposed LNAs are based on conventional inductively source degenerated structures, as shown in Fig. 2. L_g, L_s and transistor M1 match the input impedance to 50 Ω. The equivalent input impedance can be expressed as[8]

$$Z_{in} = s(L_g + L_s) + \frac{1}{sC_{gs}} + \frac{g_m}{C_{gs}}L_s, \tag{1}$$

where g_m and C_{gs} are the transconductance and gate–source capacitance of M1. The resonant frequency f_0 and Q value of the input matching network are

$$f_0 = \frac{1}{2\pi\sqrt{L_g + L_s}C_{gs}}, \tag{2}$$

$$Q = \frac{R_s}{2\pi f_0(L_g + L_s)} = 2\pi f_0 R_s C_{gs}. \tag{3}$$

When $\frac{g_m}{C_{gs}}L_s$ is equal to R_s at the frequency of f_0, input impedance matching is realized. A lower Q value implies a wider bandwidth. It is easy to realize impedance matching for the narrower band of 3400–3600 MHz; by increasing L_g, L_s and the gate finger width of M1, acceptable input matching ($S_{11} < -10$ dB) can also be achieved for the wider bandwidth of 1880–2400 MHz.

When the parasitic resistor of the gate inductor is neglected, the small signal gain and noise factor of the LNA can be expressed by

$$G_V = \frac{f_T R_L}{2fR}, \tag{4}$$

$$F = 1 + \frac{\gamma}{\alpha}\left(\frac{f}{f_T}\right)^2\left(\sqrt{g_m R_s} + \frac{1}{\kappa\sqrt{g_m R_s}}\right)^2 + \frac{\alpha\delta\left(1 - |c|^2\right)}{\kappa g_m R_s}, \tag{5}$$

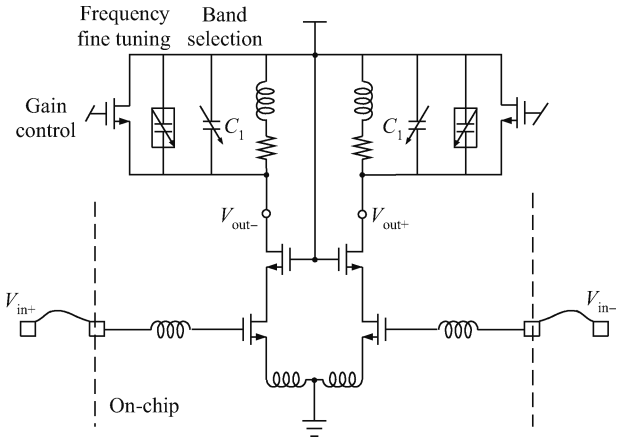

Fig. 3. Simplified structure of the proposed LNAs.

where f is LNA operation frequency, f_T is the cutoff frequency of M1, R_L is equivalent load resistance. γ, α, κ and δ are process parameters; c is gate noise and drain noise correlation coefficient. Hence a minimum noise figure can be acquired by choosing a certain g_m value.

The simplified schematic of the proposed LNAs is shown in Fig. 3. Differential structure can avoid the influence of bond wires on the source inductance and load impedance, whereas bond wires connected to the input port are utilized in order to decrease the value of the gate-series on-chip inductors, which can lower the noise figure and reduce the chip area as well. Load networks are composed of differential inductors, switched capacitors, and a gate-voltage-controllable NMOS transistor. A single switched capacitor of 1.2 pF in LNA2 is used for differentiating and switching bands of 1880–2025 MHz and 2300–2400 MHz. Biases and switched capacitors of the two LNAs are controlled by 2-bit data in the SPI. "10" enables LNA1 and disables LNA2, so the LNA operates at the upper frequency band of 3400–3600 MHz; "01" disables LNA1, enables LNA2, and switches off C1, so that LNA2 is tuned to a frequency band of 2300–2400 MHz; similarly, "00" switches on C_1, and LNA2 is tuned to the lower frequency band of 1880–2025 MHz.

When the LNA structure is complex, a long interconnection metal line is inevitable, which will add in amounts of parasitic capacitance and inductance. Due to the limited accuracy of the parasitic extraction (PEX) tool, the real resonant frequency of the load network might be different from the target value. As a result, calibration networks to perform peak gain point tuning are designed for both of the LNAs. Calibration networks are composed of seven identical switched capacitors classified into three groups, which is controlled by 3-bit data from the SPI module, as illustrated in Fig. 4. The relationship between resonant frequency variation and capacitance change can be expressed as

$$\Delta f = \frac{1}{2\pi\sqrt{LC}} - \frac{1}{2\pi\sqrt{L\,(C+\Delta C)}} \approx f_0\frac{\Delta C}{2C}, \tag{6}$$

where $f_0 = \frac{1}{2\pi\sqrt{LC}}$ is the target resonant frequency, and L, C are the inductance and capacitance of the load network.

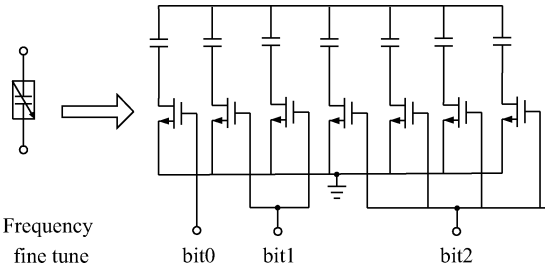

Fig. 4. Structure of the switched capacitor array.

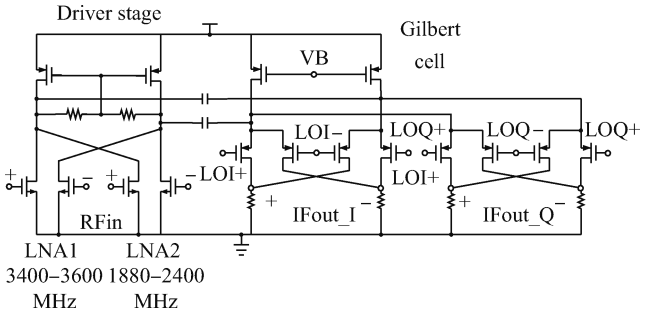

Fig. 5. Schematic of a folded double-balanced Gilbert mixer.

NMOS transistors parallel with the load RC tank are used to change the gain of LNA so as to improve the linearity performance when the input RF signal is large. The gate voltage of the transistor can be set to be high and low. When the gate voltage is low, it shuts off and exhibits high resistance, so has no effect on the gain; when the gate voltage is high, it is operating in the linear region and the LNA gain drops.

In high gain mode, the voltage gains of both LNAs are over 19 dB and the noise figure is below 2 dB by simulation; in low gain mode, the voltage gain is about 7 dB. The current consumption of the LNAs is around 14 mA.

3.2. Mixer

The mixer converts the RF signal into an IF signal. The IF bandwidth of the TD-SCDMA signal is 1.6 MHz, while the IF bandwidths of the LTE are varied, and are 5 MHz, 10 MHz, 15 MHz and 20 MHz. For the LTE-Advanced, the maximum IF bandwidth is 100 MHz. Therefore, the bandwidth of the mixer for the three modes should be designed to be 100 MHz.

The most common mixer architecture is based on the double balanced Gilbert cell. It is usually believed that the active mixers provide a higher conversion gain, while the passive mixers exhibit lower flicker noise and higher linearity. Passive mixers are used more and more frequently. However they have some drawbacks. Since a passive mixer provides no gain, the gain is always acquired though post mixer amplifiers (PMA). In the PMA, larger size transistors are needed to lower the flick noise and increase the gain, however it limits the IF signal bandwidth. Therefore, passive mixers are more applicable to narrow band systems rather than broadband systems. The proposed mixer adopts an active structure rather than a passive one.

LO switch pairs of the mixer are comprised of PMOS tran-

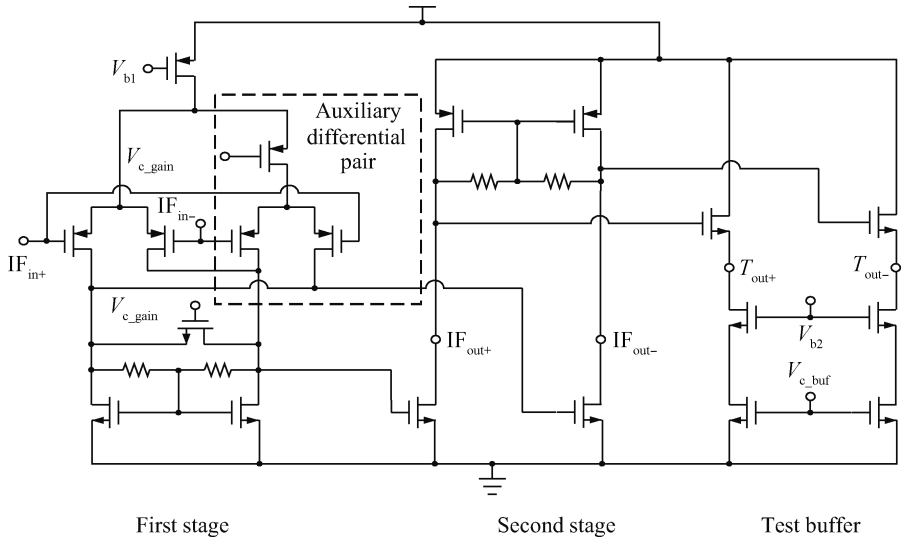

Fig. 6. Schematic of the post mixer amplifier.

sistors to reduce flicker noise, because of the lower hole mobility compared with the NMOS transistors[9]. A folded design is adopted for two reasons: firstly, it can solve the well-known trade-off issue between the conversion gain and noise figure in a basic Gilbert active mixer, and secondly, a NMOS transistor in the driver stage is more effective than a PMOS transistor. Additionally, the folded driver stage is also used to combine the output RF signals from LNA1 and LNA2. The amplified voltage signals are converted to current by the transconductance transistor and then added together at the drain. This combination method is simple and effective to switch between LNA1 and LNA2; it can also avoid interaction between the two LNAs. The schematic of the mixer is displayed in Fig. 5.

The mixer consumes DC currents of 10 mA and 11.8 mA for the lower and higher frequency band respectively, and provides a conversion gain of 6 dB, which has been optimized together with the post mixer amplifier to acquire the best IIP3. By the way, the gain of the mixer can be enhanced to 10 dB by increasing the load resistance if needed.

3.3. Post mixer amplifier

A post mixer amplifier is used to provide more gain in the receiver path and suppress the noise of succeeding circuits. It also sets the DC bias voltage for the low pass filter (LPF). Compared with the one stage amplifier, the proposed two-stage amplifier has a higher gain-bandwidth product and it is easier to achieve the DC output voltage of 900 mV. The gain of the PMA is controlled by a NMOS transistor by setting the gate voltage to high and low. The auxiliary differential pair and switch transistor are used to increase the IIP3 further. In the low gain mode, the auxiliary differential pair is off, when the total current of the amplifier is constant but the transconductance is lower, thus the IIP3 of the PMA is improved. Compared with only changing the load impedance of the amplifier, the IIP3 is improved by introducing a differential auxiliary pair. The PMA draws a DC current of 4 mA and exhibits a gain of 18 dB and 6 dB for the high and low gain mode. The schematic of the baseband amplifier is shown in Fig. 6.

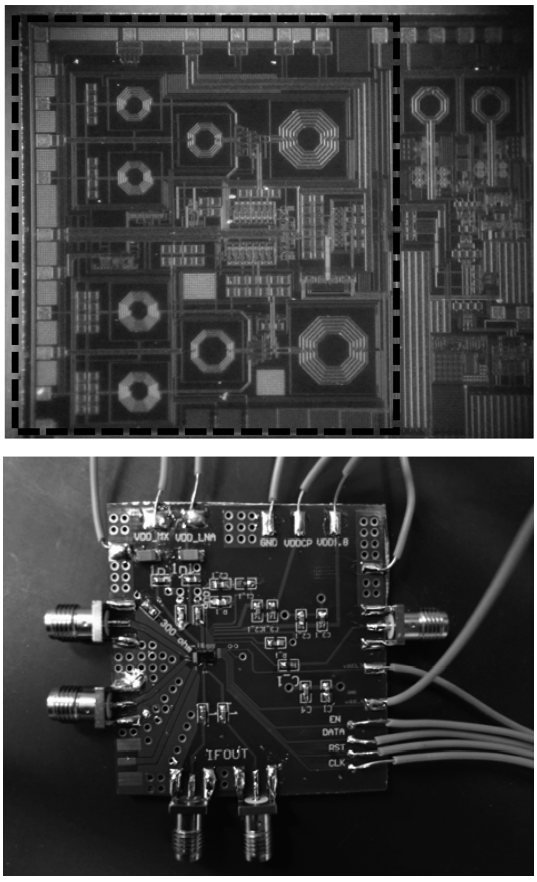

Fig. 7. Micrograph of the front-end and testing PCB.

4. Implementation and measurement results

The RF receiver front-end was fabricated in the TSMC 0.18-μm RF CMOS process. The chip area was 1.3 mm^2 including all bonding pads. The chip is bonded on a FR-4 printed circuit board (PCB) with external components mounted on the PCB, including SMA connectors, bias resistors and so on. The micrograph of the front-end chip and testing PCB are shown

Table 1. The front-end performance summary.

Parameter	Value		
Mode	TD-SCDMA	LTE & LTE-Advanced	
RF band (MHz)	1880–1920 2010–2025	2300–2400	3400–3600
S_{11} (dB)	–20	–15	–13
Gain (dB)	43/31/18	43/31/18	44/32/19
DSB NF (dB)*	3.4	3.5	3.5
P_{1dB} (dBm)**	–46/–18	–46/–18	–45/–17
IIP3 (dBm)**	–33/–20	–33/–21	–35/–22
Power (mW)	55.3	56.7	56.7
Supply voltage (V)	1.8	1.8	1.8
Area (mm^2)	1.3	1.3	1.3
Technology	CMOS 0.18 μm	CMOS 0.18 μm	CMOS 0.18 μm

* High gain mode; **High and low gain mode.

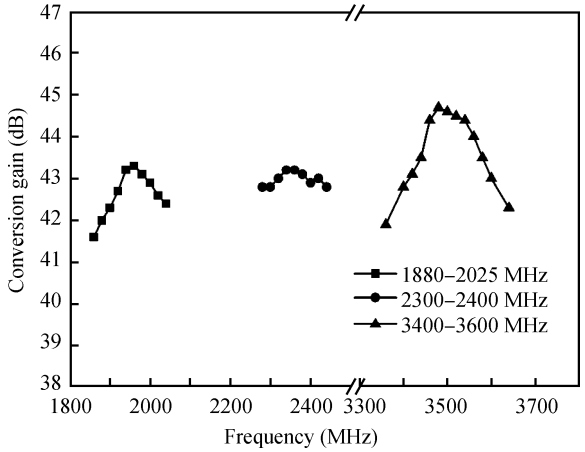

Fig. 8. Measured conversion gain at the three frequency bands.

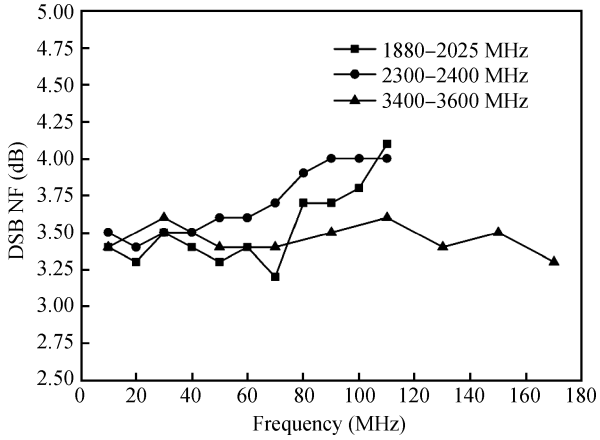

Fig. 10. Measured DSB noise figure of the front-end.

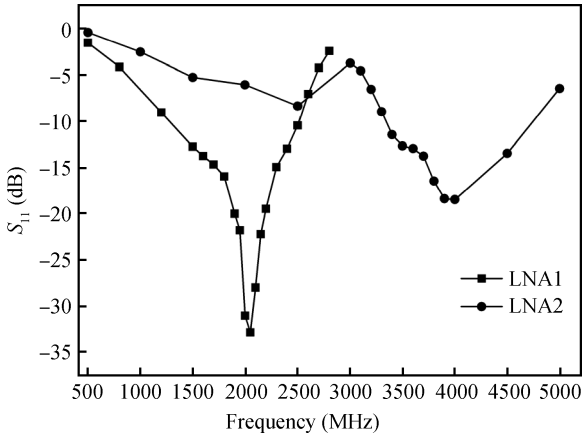

Fig. 9. Measured S_{11} for the two LNA.

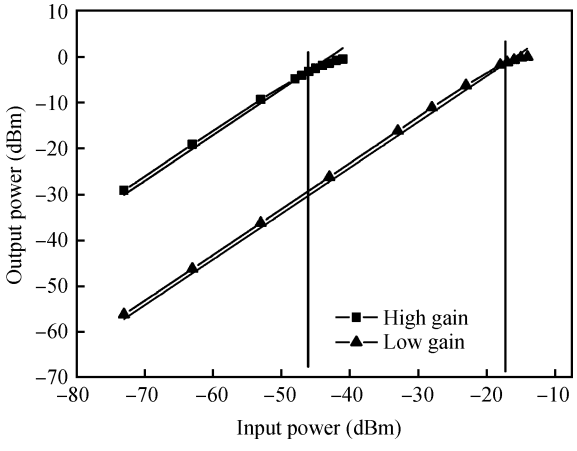

Fig. 11. Measured input 1 dB compression point in high and low gain modes at a 3400–3600 MHz frequency band.

in Fig. 7. The test equipment includes an Agilent S-parameter network analyzer 8720ES, a spectrum analyzer E4440A, a RF signal generator E4438C, a noise figure analyzer N8975A, and a N4002A noise source.

LO signal is generated by an on-chip frequency synthesizer, which is set to 1950 MHz, 2350 MHz and 3500 MHz respectively, for performance measurements at 1880–2025 MHz, 2300–2400 MHz and 3400–3600 MHz frequency bands. Two commercial baluns are used to divide the single-ended RF signal from Signal Generator into differential signals, which are LDB183G4510G-120 (muRata) operating around 3500 MHz with an insertion loss of 1.3 dB, and LDM181G9310CC001 operating at 1880–2400 MHz bands with an insertion loss of 0.9 dB.

Figure 8 shows measured conversion gains versus frequency in a high gain mode, which are better than 43 dB. The test buffer of the PMA introduced a loss of 7.5 dB by simula-

tion, which is calculated during the conversion gain measurement. The conversion gains of the middle gain mode and low gain mode are about 31 dB and 18 dB. It should be mentioned that in contrast to the post simulation results, the real peak gain frequency points move downward, and then are calibrated back in the measurement by the fine frequency tuning network. This variation results from more parasitic capacitance and inductance presenting in the RF signal path than the estimated value by the PEX tools.

The measured S_{11} of the front-end is below 11.5 dB, and the double side band (DSB) noise figure in high gain mode is about 3.5 dB, as shown in Figs. 9 and 10. Measured input 1dB compression points at 3400–3600 frequency bands in high and low gain modes are –45 dBm and –17 dBm, as shown in Fig. 11. The input third order intercept points (IIP3) of the front-end are measured by two tone tests. The power consumption is 55.3 mW and 56.7 mW for the TD-SCDMA and LTE/LTE-Advanced modes respectively. Table 1 summarizes all the measured performance of the RF receiver front-end.

5. Conclusions

In this paper, a RF receiver front-end for TD-SCDMA, LTE, and LTE-Advanced is presented. The front-end employs direct-conversion design, and consists of two differential LNAs, a quadrature mixer, and two IF amplifiers in the I/Q paths. It covers four radio frequency bands, which are 1880–1920 MHz and 2010–2015 MHz for the TD-SCDMA standard, 2300–2400 MHz and 3400–3600 MHz for the LTE and LTE-Advanced. The front-end has three gain modes to meet the receiver dynamic range requirements. Switched capacitor arrays are used to calibrate the resonant frequency point of the LNA compensating the inaccuracy of parasitic extraction. Frequency band selection, resonant frequency point adjustment and gain mode selection are all digitally controlled by an on-chip SPI module. The measured double-sideband (DSB) noise figure is below 3.5dB and the conversion gain is over 43dB. The front-end is fabricated in a TSMC 0.18-μm RF CMOS process and occupies an area of 1.3 mm^2. The total current consumption is 31 mA from a 1.8-V supply.

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