An embeddable SOC real-time prediction technology for TDDB*

Xin Weiping(辛维平)†, Zhuang Yiqi(庄奕琪), and Li Xiaoming(李晓明)

School of Microelectronics, Xidian University, Xi'an 710071, China

Abstract: This paper presents an embeddable SOC real-time prediction circuit and method for TDDB. When the SOC under test is fails due to TDDB, the prediction circuit is capable of issuing a warning signal. The prediction circuit, designed by using a standard CMOS process, occupies a small silicon area and does not share any signal with the circuits under test, therefore, the possibility of interference with the surrounding circuits is safely excluded.

Key words: TDDB; real-time; reliability; prediction; SOC

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1. Introduction

With the application of system on chip (SOC) in aviation and space technology, and with the rapid development of complex electronic systems towards miniaturization, high integration, and multi-function, more stringent requirements are set for the quality and reliability of the SOC. The reliability of a circuit or system is of more or less equal significance as its performance. While in some application fields, reliability becomes a concern even prior to the functions. Therefore, SOC reliability technology is considered as an important specification of high reliability electronic systems, and it is of more importance than ever. Meanwhile, how to ensure the reliability of such SOCs has become a growing challenge, one of the reasons is the lack of an effective testing method.

This paper presents a new circuit that is embeddable in SOC and a method that can predict the failure caused by TDDB in real-time. The circuit can be used as an IP embedded into the host circuit, which, together with the host circuit, can be produced, transported and used. This ensures that any of the factors that affect product reliability will also act on the prediction unit. As long as their working environment and stress parameters are the same, the failure rate will remain the same, which overcomes the limitations of traditional off-line testing and makes embedded real-time prediction possible.

2. TDDB real-time prediction theory

The bath curve in Fig. 1 is the relationship between the failure rate and the lifetime of electronic products. The useful lifetime region of the devices generally refers to a random failure region, while it is considered generally that a device will fail when its lifetime approaches the wear-out failure region.

Higher stresses are applied to the gate oxide of the TDDB failure prediction circuit than that of the operation conditions of the host, making the gate oxide of the prediction circuit fail prior to the SOC under test. Figure 1 shows the relationship of the lifetime of the TDDB failure prediction cell and that of the gate oxide of the SOC under test. When there is a predefined prediction interval from the lifetime of SOC under test to its wear-out failure region, the prediction circuit under higher stress has already approached its wear-out failure region, that is, the TDDB prediction cell has approached its failure point. At this time, the prediction cell issues a warning signal, so the purpose of TDDB failure prediction is achieved.

When greater stress is exerted on the prediction circuit MOS capacitor, the relationship between accelerated lifetime and its normal lifetime of the gate oxide is as follows:

$$\mathrm{AF} = T_{\mathrm{use}}/T_{\mathrm{stress}}. \tag{1}$$

It is generally believed that temperature, voltage and area acceleration factors are independent of each other in accelerated lifetime test, and then the total acceleration factor is:

$$\mathrm{AF(total)} = \mathrm{AF}(T)\cdot\mathrm{AF}(V)\cdot\mathrm{AF}(A), \tag{2}$$

where $\mathrm{AF}(T)$ is the temperature acceleration factor; $\mathrm{AF}(V)$ is the electric field acceleration factor; $\mathrm{AF}(A)$ is the area accelerating factor. Therefore, the lifetime of a device is:

$$T_{\mathrm{use}} = T_{\mathrm{stress}}\cdot\mathrm{AF(total)}. \tag{3}$$

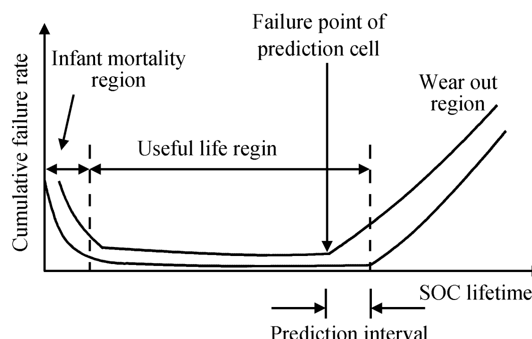

Fig. 1. Schematic figure of TDDB failure prediction.

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† Corresponding author. Email: xinweiping2004@163.com
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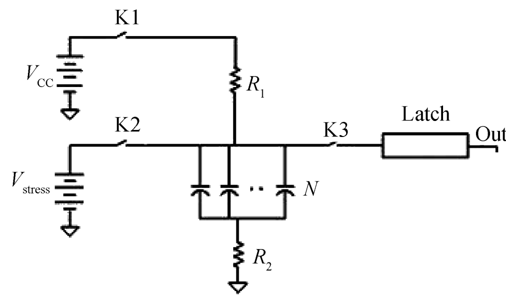
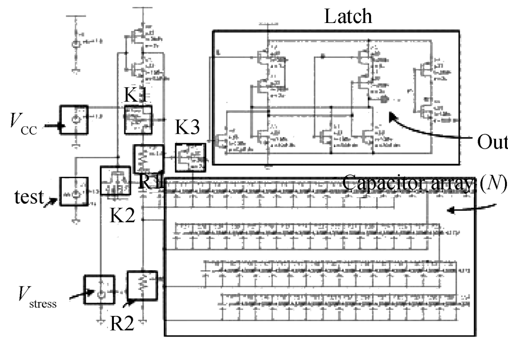


(a) Prediction circuit schematic



(b) Prediction circuit

Fig. 2. TDDB prediction cell circuit.

3. Circuit and method of TDDB real time failure prediction

Generally, more stresses (including the electrical stress and thermal stress) in conventional reliability tests are applied to MOS capacitors[1–4], so as to accelerate MOS capacitor failure, and then the MOS device lifetime is extrapolated. Such experiments can only be offline, and can not objectively reflect the stress experienced by the host circuit.

To realize the real-time lifetime prediction, a prediction circuit must:

(1) reflect the degradation of the host circuit gate oxide degradation with time;

(2) be able to transform degraded parameters into digital logic signals;

(3) be isolated from the host circuit and not interfere with the host circuit;

(4) consume less power and occupy less area.

3.1. Prediction circuit theory

According to the above requirements, the TDDB failure prediction circuit schematic and the corresponding circuit are shown in Fig. 2. The TDDB test structure in the prediction circuit consists of N MOS capacitors in parallel. These MOS capacitors are formed simultaneously with gate dielectrics of the host circuit. They not only undergo the same stress in the manufacturing process, but also work in the same environment, and they follow the same degradation model, too. So the prediction circuit can fully reflect the host circuit degradation. Pre-set voltage V_{stress} is applied to MOS capacitors. According to demands, K1, K2, K3 can switch between two operation modes. Read_out resistor R_1, stress resistor R_2 is polycrystalline resistance and $R_1 \gg R_2$.

The gate oxide failure prediction cell includes N capacitors in parallel. The capacitor's resistance is much higher than polysilicon's, so its anode level is high before breakdown. As long as one of the MOS capacitors under TDDB stresses fails, the gate current will increase suddenly, which indicates the MOS capacitors' resistance decreases sharply. So the capacitor anode level is low, and the prediction circuit will alarm.

3.2. Operation modes of the prediction circuit

The prediction circuit has two operation modes that can be switched according to the status of these three switches.

(1) Accelerated degradation mode: when test signal "test" is low, the switches K1, K3 off, K2 on, stress voltage V_{stress} is applied to N MOS capacitors in parallel. These capacitors keep degrading under V_{stress}, because V_{stress} is larger than V_{cc}, MOS capacitors will fail prior to the gate oxide of the host circuit. Stress resistor R_2, which connects in series with the MOS capacitors, serves as a protection resistor. When the gate oxide capacitor fails, the stress resistor will prevent the prediction circuit from short circuit.

(2) Detection of degradation made: when "test" is high, the switches K1, K3 on, K2 off, Read_out resistor R_1, MOS capacitors and stress resistor R_2 is in series. If none of the capacitors is failing, the latch input is "1", and its output is "0"; if there is a capacitor with low resistance due to degradation, the latch input is logic "0", and its output is logic "1".

3.3. Determination of N and stress voltage V_{stress}

At present, the type of defects that lead to gate oxide failure are inconclusive, as is the TDDB failure model. But the E model has been recognized widely, which is referred to as the thermo-chemical breakdown model, proposed by Crook *et al.*[5, 6]. The relationship between gate oxide TDDB lifetime and stress is:

$$\text{MTF} = A\exp(-\gamma E)\exp(E_a/KT), \tag{4}$$

where MTF is the TDDB mean lifetime of the gate oxide layer; A is a constant associated with the material; γ is the electric field acceleration parameter; E is the gate oxide electric field strength (in units of MV/cm); E_a is the activation energy (eV); K is the Boltzmann constant; T is absolute temperature.

From Eq. (4), we can get the electric field acceleration factor of the E model as:

$$\text{AF}(E) = \frac{g(V_{stress})}{g(V_{use})} = \exp[-\gamma(E_{stress} - E_{use})], \tag{5}$$

where E_{use} is the gate oxide electric field strength of the circuit under test; E_{pred} is the gate oxide electric field strength of the TDDB prediction cell.

After the accelerated lifetime test, the market lifetime can be solved by extrapolation, and the TDDB lifetime of the oxide layer is a random variable that follows the Weibull distribution[1, 7, 8]. Weibull distribution function is:

$$F(t) = 1 - \exp\left[-\left(\frac{t}{t_{1/e}}\right)^{\beta}\right], \tag{6}$$

where $t_{1/e}$ is characteristic lifetime; β is Weibull slope.

The gate oxide failure prediction cell includes N MOS capacitors in parallel (N is unknown). If only one of the N capacitors fails, there will be a large current across the gate oxide, and then these capacitors will be a resistor. Therefore, the time-to-breakdown $t_{\rm BD}$ of the first gate oxide capacitor is the lifetime of the prediction cell, which determinates the failure point of the prediction cell (as shown Fig. 1).

According to the calculation method concerning the reliability of the cumulative failure rate, the cumulative failure rate of the first failure of N capacitors is:

$$F(t_{1/N}) = 1/N. \tag{7}$$

The lifetimes of these N capacitors also follow the Weibull distribution, so we can conclude:

$$t_{\rm pred} = t_{1/N}\left(\ln\frac{N}{N-1}\right)^{-1/\beta}, \tag{8}$$

where $t_{\rm pred}$ is the characteristic lifetime of the TDDB prediction cell; $t_{1/N}$ is the alarm time of the TDDB prediction cell.

Generally, market lifetime is the duration of cumulative failure rate up to 0.1%, so we can conclude:

$$t_{\rm pred} = t_{\rm host}\left[\frac{-B}{NA\ln(1-0.1)}\right]^{1/\beta}\exp[-\gamma(E_{\rm stress}-E_{\rm use})], \tag{9}$$

where $t_{\rm host}$ is the market lifetime of the host circuit; B is the gate oxide area of the host circuit; A is the area of a single capacitor of the prediction circuit. By Eqs. (8) and (9), we can get N, the number of MOS capacitors and $V_{\rm stress}$, the stress voltage applied to the MOS capacitors.

4. Experiments

The TDDB lifetime test in this paper consists of two steps: (1) MOS capacitor group accelerated lifetime test, to obtain the model parameters and activation energy through experiments; (2) verify the function of the TDDB prediction cell.

The samples are achieved by MPW, using 0.18 μm CMOS process. The thickness of the MOS capacitor gate oxide is 4.0 nm with a single capacitor area of 0.5×0.2 μm^2.

4.1. High temperature and constant electric field TDDB reliability test

Gate oxide test methods include constant-current source, constant-voltage source, current ramp, and voltage ramp test[9]. The experiments in this paper choose the constant-voltage source test.

As modern SOCs and ultra-large-scale integrated circuits are getting smaller in feature size and consume more power, most of them work under high temperature, so electrical stress alone cannot assess a devices' lifetime at normal temperatures. Therefore, this test applies to the MOS capacitor high-temperature, constant electric field stress to evaluate the reliability of the gate oxide.

Figure 3(a) is a microphotograph of the test chip, and Fig. 3(b) is the NMOS capacitors array. At 130 ℃, the capacitor array is applied to 2.8 V, 3.0 V, 3.2 V voltage stress

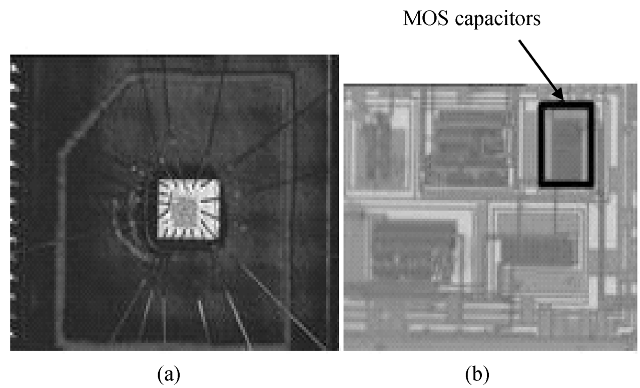


Fig. 3. (a) Microphotograph of the chip for reliability tests. (b) NMOS capacitors array in chip.

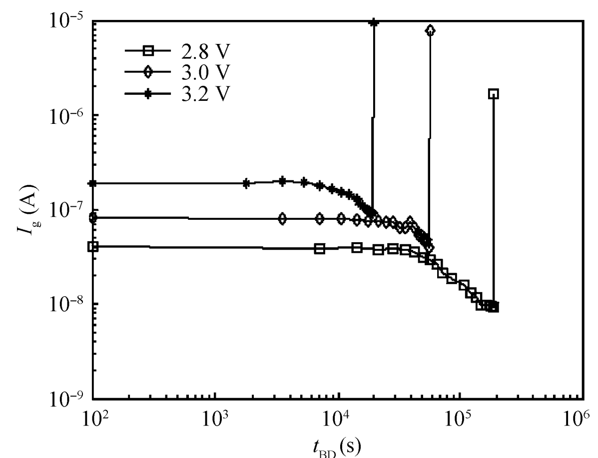


Fig. 4. Variation of gate current I_g of MOS capacitor with time under constant voltage bias.

to cause rapid failure. Low-frequency noise current amplifier SR570 and the noise analysis system of Xidian University are employed to measure the leakage current of the MOS capacitors and extract the specific values. Figure 4 is a MOS capacitor leakage current at different voltages versus time (characteristic lifetime) curve.

4.2. TDDB prediction cell functional verification

The capacitor array consists of 64 capacitors in parallel with the same size. Figure 5(a) is the TDDB prediction circuit chip, Figure 5(b) is the TDDB test board.

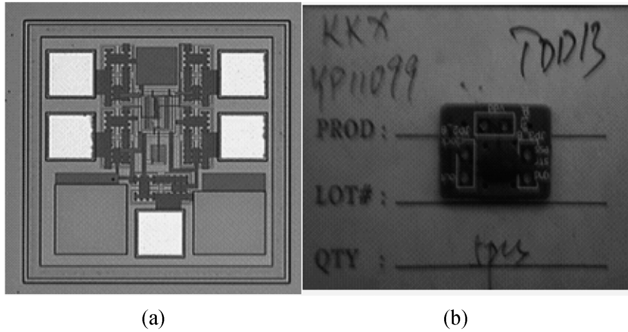
During functional verification, the capacitor array is applied to stress of 2.8 V, 130 ℃. Early on, the prediction circuit's output is low. After 90, 430 s, its output is high, indicating that the MOS capacitor has failed and the prediction circuit sends the alarm signal.

5. Results and discussion

During the experiment, all of the MOS capacitors are divided into 4 groups, and there are 20 capacitors in each group. At 130 ℃, capacitors are applied to 2.8 V, 3.0 V, 3.2 V voltage, respectively, and the value of its lifetime is obtained. Moreover, the lifetime of MOS capacitors is obtained under 110 ℃,

Table 1. TDDB accelerated lifetime experimental data.

Temperature (℃)	Electric field (MV/cm)	Electric parameter γ	Activation energy (eV)	Test lifetime (s)	Market lifetime (Y) (25 ℃)
130	7.0	3.0007	0.4805	89880	733.1
130	7.5	3.0007	0.4805	42600	732.8
130	8.0	3.0007	0.4805	20040	731.1
110	7.0	3.0007	0.4805	190920	733.5



(a) (b)

Fig. 5. (a) Microphotograph of the TDDB prediction circuit chip. (b) Test board.

3.0 V in order to get the temperature acceleration factor.

5.1. Results and discussion of high temperature and constant electric field TDDB test

As can be seen from Fig. 4, after the samples are applied to stress, the current I_g decreases slowly with time. Exceeding a critical value, the current increases suddenly and the samples experience breakdown. During experiments, there is no occurrence of the current saturation, which indicates that there are continuous new traps creations. Under stress, trap charge density in oxide layer increases due to charge trapping and new traps created by hot carrier injection in SiO_2. So, I_g under constant stress decreases due to trapped charge. The samples' lifetime diminishes with the increase of voltage stress, which is consistent with the theoretical expectation[10].

From Eqs. (3), (12), (14), we can get the slope of $\ln(t_{BD})$–E_{ox}, which indicates that the average electric parameter γ of module E is 3.0007, and in the same way, we can obtain the activation energy $E_a = 0.4805$.

From Eqs. (1) and (4), we can conclude the electric field accelerated factor:

$$\mathrm{AF}(E) = \frac{t_{BD}\left(E_{use}\right)}{t_{BD}\left(E_{test}\right)} = \exp\left[-\gamma\left(E_{use} - E_{test}\right)\right]. \quad (10)$$

In the same way, the temperature accelerated factor is:

$$\mathrm{AF}(T) = \frac{t_{BD}\left(T_{use}\right)}{t_{BD}\left(T_{test}\right)} = \exp\left[\left(\frac{1}{T_{use}} - \frac{1}{T_{test}}\right)\frac{E_a}{k}\right]. \quad (11)$$

Substituting γ and E_a into Eqs. (15) and (16), the electric field accelerated factor and temperature accelerated factor can be achieved, thus the market lifetime of the samples can be obtained by extrapolation.

It can be seen from Table 1 that the samples' market lifetime is basically same under different stresses, which is consistent with the facts.

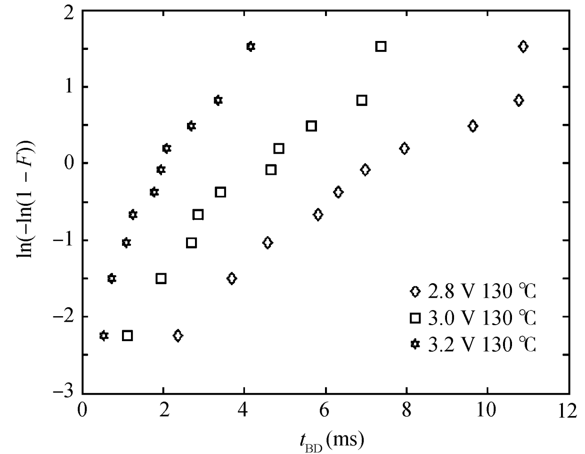


Fig. 6. Relationship of ln(−ln(1 − F)) with t_{BD} at 130 ℃.

5.2. Results and discussion of the TDDB prediction cell test

During the experiments of the TDDB prediction cell samples, the samples' average lifetime is 13800 s under 3.0 V, 130 ℃ when its failure rate is 0.1. At the same time, the TDDB prediction cell output is high.

It is achieved that the lifetime t_{BD} of the MOS capacitors, which relationship is shown in Fig. 6 with failure rate under three electric field stresses at 130 ℃. From Eq. (6), it can be derived:

$$\ln(-\ln(1-F) \propto \beta \ln t_{BD}, \quad (12)$$

where β is the Weibull slope. So we can get $\beta = 1.68$, which is consistent with the conclusion in Ref. [11]. In addition, we can know that the reduction of the gate dielectric lifetime is much quirkier as the increase of the stress voltage. Therefore, electric field is key factor of the TDDB lifetime in ICs.

From Eq. (9), it can be obtained that the prediction cell lifetime is 14315 s when its failure rate is 0.1, which is consistent with the experimental data.

The proposed TDDB embedded circuit for real-time prediction can accurately predict time-dependent dielectric breakdown, and does not occupy too much additional area and power because it covers only an area of 25 × 16 μm^2, and its energy consumption is only 458 μW at a stress voltage rated at 2.8 V. It only shares the power supply with the host, and does not cause signal interference to the host.

From the above, it can be known that the electric field acceleration factor AF(E) is much larger than the temperature acceleration factor AF(T). Therefore, the lower gate voltage and shorter time of voltage stress is an effective way to extend the lifetime of the gate dielectric if we only consider the TDDB effect during circuit design. If more attention is paid to other

failure mechanisms such as NBTI, it will be an important consideration to make power distribution more uniform.

6. Conclusions

This paper discloses a method and circuit that can be embedded in an SOC, and are capable of TDDB life prediction. It will help to minimize the security problems that are caused by element failures existing in application fields as aviation, aerospace, etc，which demand high reliability. It overcomes the traditional off-line test limitations, and provides a new precise method for the reliability evaluation and life prediction of electronic products.

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