A 1.4-V 48-μW current-mode front-end circuit for analog hearing aids with frequency compensation*

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Abstract: A current-mode front-end circuit with low voltage and low power for analog hearing aids is presented. The circuit consists of a current-mode AGC (automatic gain control) and a current-mode adaptive filter. Compared with its conventional voltage-mode counterparts, the proposed front-end circuit has the identified features of frequency compensation based on the state space theory and continuous gain with an exponential characteristic. The frequency compensation which appears only in the DSP unit of the digital hearing aid can upgrade the performance of the analog hearing aid in the field of low-frequency hearing loss. The continuous gain should meet the requirement of any input amplitude level, while its exponential characteristic leads to a large input dynamic range in accordance with the dB SPL (sound pressure level). Furthermore, the front-end circuit also provides a discrete knee point and discrete compression ratio to allow for high calibration flexibility. These features can accommodate users whose ears have different pain thresholds. Taking advantage of the current-mode technique, the MOS transistors work in the subthreshold region so that the quiescent current is small. Moreover, the input current can be compressed to a low voltage signal for processing according to the compression principle from the current-domain to the voltage-domain. Therefore, the objective of low voltage and low power (48 μW at 1.4 V) can be easily achieved in a high threshold-voltage CMOS process of 0.35 μm ($V_{\rm TON} + |V_{\rm TOP}| \approx 1.35$ V). The THD is below -45 dB. The fabricated chip only occupies the area of 1×0.5 mm^2 and 1×1 mm^2.

Key words: hearing aid; frequency compensation; state space; continuous gain; current-mode
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1. Introduction

Recently, hearing aid design issues have expanded to consider how to accommodate low-income individuals and the differences in performance optimization according to each individual user and comfortable level enhancement. That is, consideration of the user should be taken into account early on in the hearing aid design process. Generally, a digital hearing aid can incorporate the various factors by external gain fitting. However, digital hearing aids are very expensive due to their integrated dedicated A/D, D/A and DSP[1−3]. As to conventional analog hearing aids, the amount of gain discretely distributes between 0 dB and 40 dB[4]. So, a conventional analog hearing aid cannot offer accurate amplitude compensation to account for individual differences. Moreover, a conventional analog hearing aid cannot realize frequency compensation, which only appears in the DSP unit of a digital hearing aid in the field of the low-frequency hearing loss.

To overcome these problems, this paper introduces the current-mode technique and implements a low-power and low-voltage front-end circuit with the function of accurate amplitude compensation and frequency compensation. The circuit mainly includes a current-mode AGC unit and a current-mode adaptive filter. In the AGC unit, the current-mode technique makes the key MOS transistors work in the subthreshold region. With a varied voltage signal at the selected terminal of a MOS transistor, continuous gain with an exponential characteristic for accurate amplitude compensation can be easily implemented. In the current-mode filter, the current-mode technique allows the step gain for the frequency compensation in the field of low-frequency hearing loss. Namely, the gain of the filter is high in the low-frequency band (100–3000 Hz) and low in the high-frequency band (3–10 kHz). This property can meet the needs of most individual users and enhance the comfortable level. Moreover, the power and the voltage are low because the input current signal is compressed logarithmically to a low voltage signal for processing according to the compression principle of the current-mode technique. .

2. Architecture

The block diagram of the front-end circuit is shown in Fig. 1. The front-end circuit consists of an AGC, a filter, and a digital control interface. The AGC is used to realize the amplitude compensation. Also, it behaves as a limiter to ensure that the individual pain threshold is never reached. Namely, if the input sound level is more than the pre-set knee point, such as 0.3 μA, it is compressed based on a compression ratio which is determined by the digital control interface. The filter presents a step gain to perform the frequency compensation. The digital control interface is intended for calibrating the parameter

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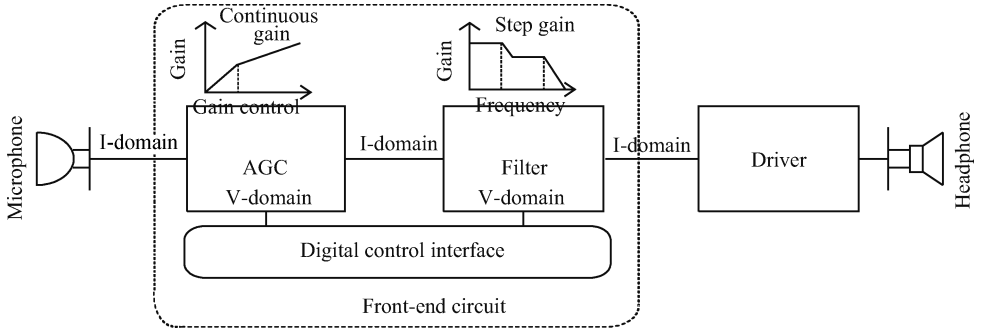


Fig. 1. Block diagram of the front-end.

of the front-end so that it can offer high flexibility in order to meet individual requirements.

The key MOS transistors of the front-end circuit work in the subthreshold region. In the subthreshold region, the transistor can work in two compression modes: gate compression (GC) and source compression (SC), shown in Eq. (1)[5].

$$I = F(V) = \begin{cases} I_S e^{-(V_{TO}+nV_{bias})/(nU_t)} e^{V/(nU_t)}, & \text{GC}, \\ I_S e^{(-V_{TO}+V_{bias})/(nU_t)} e^{-V/(U_t)}, & \text{SC}, \end{cases} \quad (1)$$

where V, I, and V_{bias} stand for the compressed voltage signal at the selected terminal, the current signal at the drain and the biasing reference for another terminal. And I_S and n are a constant and the subthreshold slope, respectively. It is seen that the current signal I is compressed to the voltage signal V logarithmically from current-domain to voltage-domain. Then, the voltage signal is processed in the front-end circuit. Finally, the voltage signal is released to a current signal. Therefore, the low-voltage and low-power front-end circuit can be implemented in a high threshold-voltage CMOS process. Moreover, a large input dynamic range is achieved.

3. The continuous-gain AGC circuit for amplitude compensation

For the conventional AGC circuits of hearing aid chips, it is difficult to present continuous gain for accurate amplitude compensation. The reason is that they implement the amplitude compensation by resistive feedback, equivalent resistive feedback, or programmable transconductor OTA, which inevitably leads to a discrete gain. Moreover, it is difficult for this type of AGC to achieve considerably low power in a high threshold-voltage CMOS process due to the voltage-mode architecture.

In order to solve this problem, a current-mode AGC as a part of the front-end circuit is proposed, shown in Fig. 2. The input current signal I_{in} is harvested from a microphone. Then the signal is amplified through a single-end current-mode amplifier at a certain gain, which is accordant with the individual differences. In addition, a rectifier and a peak detector are presented to sense the RMS amplitude I_{rms} of the output signal I_{out}. Then, the I_{rms} is compared with the preset knee point current I_{th}. If $I_{rms} > I_{th}$, a compression control voltage V_{log} is generated to adjust the amplifying gain according to the compression ratio, which is tuned by the digital control interface.

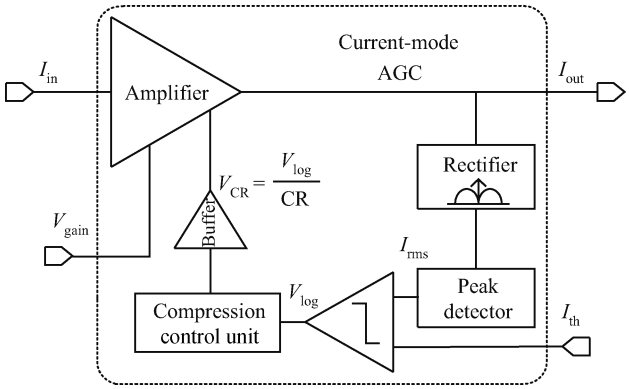


Fig. 2. Block diagram of an AGC.

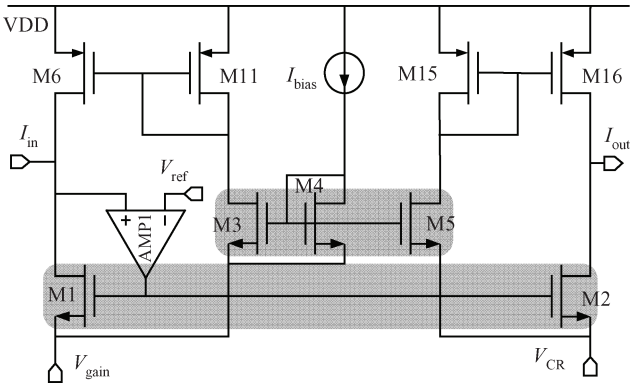


Fig. 3. Schematic diagram of the amplifier.

Otherwise, the I_{in} is just amplified without any process. Also, the peak detector offers the appropriate attack and release time to ensure protection against overshoots.

Figure 3 shows a detailed schematic diagram of the current-mode amplifier. The MOS transistors M1, M2, M3, M4, and M5 are biased in the subthreshold region. M4 is used to offer a bias current for M3 and M5. Then, M3 and M5 provide the bias current for M1 and M2, respectively. M1 and M2 are the key transistors and compose the basic unit of the current-mode amplifier. AMP1 aims at reducing the input impedance for the input signal. It is well known that this structure needs a compensation capacitor and the compensation circuit depends on the value of the bias current of M6. Here, the compensation can be cancelled because of the large transistor ratio of M1 and M2[7].

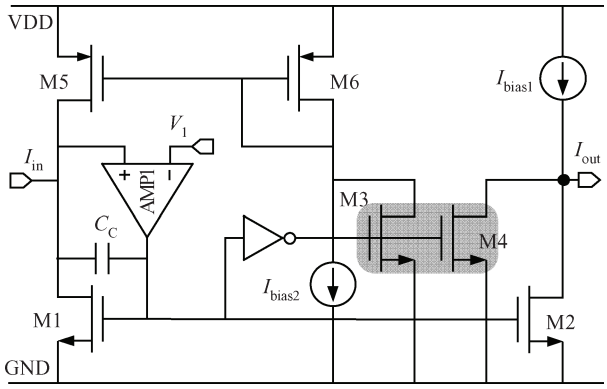


Fig. 4. Schematic diagram of the rectifier.

When the control voltage V_{gain} and V_{CR} vary, the gain of the amplifier also changes. Combined with Eq. (1), the detailed relationship is shown in Eq. (2)[6].

$$\text{Gain (dB)} = 20\lg\frac{I_{out}}{I_{in}} = 8.686\times\frac{V_{gain}-V_{CR}}{U_t}, \quad (2)$$

where U_t stands for the thermal potential. It is seen that the gain can vary continuously by adjusting the difference between V_{gain} and V_{CR}. It is seen that the gain in the log domain is proportional to the voltage. Thus, the gain is accordant with the dB SPL (a standard scale in the acoustic theory) and enhances the comfort level.

Figure 4 shows a schematic diagram of the rectifier. The MOS transistors M1 and M2 work at the boundary point between the saturation and linear region in order to make sure that the minimum peak-to-peak amplitude of I_{in} can be very small and the power can be low. M3 and M4 work in the subthreshold region. The AMP1 is used to clamp the drain voltage of M1. I_{bias2} is half of I_{bias1}. A compensation capacitor C_C is presented to make the phase margin large enough. A simple inverter is used to sense the polarity of the input signal I_{in}. If the input signal is positive, the gate voltage of M3 and M4 decreases so that positive part of I_{in} is mirrored to M2 though M1. If the input signal is negative, the gate voltage of M3 and M4 increases so that the negative part of I_{in} is copied to M4 through M3, M6, and M5.

Figure 5(a) shows a schematic diagram of the current-mode comparator[5]. The key MOS transistors M1 and M2 work in the subthreshold region. The switches are used to set the different knee points based on individual differences. According to the current mirror principle, the drain current of M2 has to be equal to or less than M1 and M7. Therefore, the source voltage V_{log} is zero and the compression mode is not triggered if $I_{in} < I_{th}$ (the knee point current). If $I_{in} > I_{th}$, the drain current of M2 is equal to I_{th} and less than I_{in} and the compression mode is triggered according to Eq. (2). The voltage V_{log} should no longer be zero because of the same gate voltage of M1 and M2. The detailed result is shown in Eq. (3) considering Eq. (1).

$$V_{log} = \begin{cases} 0, & I_{out} \leqslant I_{th}, \\ U_t \ln\dfrac{I_{out}}{I_{th}}, & I_{out} > I_{th}. \end{cases} \quad (3)$$

Figure 5(b) shows a schematic of the compression control unit. The amplifier is a two-stage amplifier, which offers a high

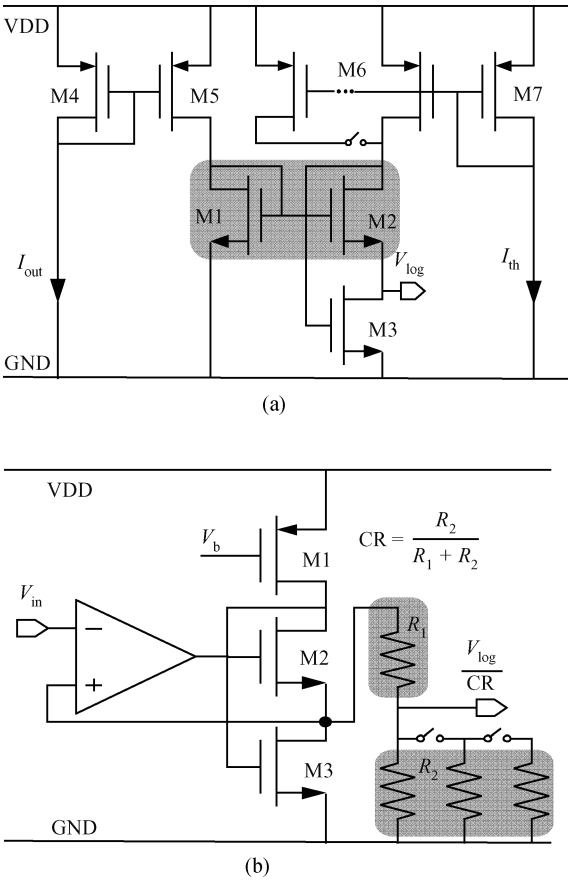


Fig. 5. (a) Schematic diagram of the current-mode comparator. (b) Schematic diagram of the compression control unit.

gain to reduce the distortion. The resistive array presents the different compression ratios. Combined with Eq. (1), the gain of the AGC is shown in Eq. (4).

$$\text{Gain}_{AGC} = \begin{cases} 8.686\dfrac{V_{gain}}{U_t}, & I_{out} \leqslant I_{th}, \\ 8.686\dfrac{V_{gain}}{\text{CR}\times U_t} + 20\lg\dfrac{I_{th}}{I_{out}}, & I_{out} > I_{th}, \end{cases} \quad (4)$$

where the CR and I_{th} stand for the compression ratio and knee point current, respectively. It is seen that the Gain_{AGC} is not only related to the CR but also to the output current signal I_{out} of the current-mode amplifier. This is different from the conventional AGC whose gain is only related to the CR and cannot automatically implement the secondary compression due to the I_{out}. This unique property can further improve the comfort level of individual users.

The peak detector is based on Ref. [8], shown in Fig. 6. The PMOS transistors M1, M2, M3, M4, and M5, are chosen to be biased in the subthreshold region. Certainly, NMOS transistors can also be applied. However, the NMOS must be presented in the deep well process in order to avoiding the influence of the voltage between the bulk and source. Therefore, the PMOS transistor is chosen in the peak detector unit.

If the input current signal I_{in} jumps from the low amplitude level to the high, the attack phase is triggered. The current of M3 increases so that the current of M4 decreases. This causes

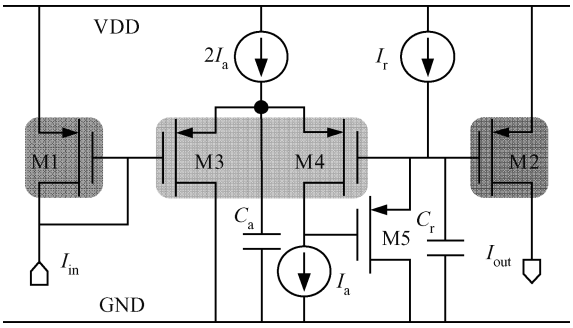


Fig. 6. Schematic diagram of the peak detector.

the gate voltage of M5 to decrease. The gate voltage of M4 is pulled down by M5. Then, the transistors M3 and M4 work in the SC mode. Combining with the capacitor C_a, an integrator whose time constant is equal to the attack time T_A is presented. If the input current signal I_{in} jumps from the high level to the low, the release phase is triggered. The gate voltage of M3 is held. Therefore, the gate voltage of M4 changes little and the transistors M2 and M4 work in the GC mode. Together with the capacitor C_r, an integrator whose time constant is equal to the release time T_R is implemented. The expression of the attack and release time is shown in Eq. (5).

$$\begin{cases} T_A = \dfrac{nC_aU_t}{I_a}, \\ T_R = \dfrac{C_rU_t}{I_r}. \end{cases} \tag{5}$$

In order to improve the comfort level of the individual users, the attack time is set about at 25 ms and the release time is set at about 85 ms.

4. The adaptive filter circuit for frequency compensation

A conventional analog hearing aid filter can only filter the audio signal with a constant gain. This type of filter does not focus on the human factor. Considering the common low-frequency hearing loss, this chapter proposes a current-mode adaptive filter, which can compensate the low-frequency hearing loss, shown in the Fig. 7[9].

It is seen from Fig. 7(a) that common hearing loss usually occurs in the low frequency band. Therefore, a current-mode adaptive filter responding to the most common hearing loss is presented where the first –3 dB frequency (ω_{c1}) and the second –3 dB frequency (ω_{c2}) can be adjusted adaptively according to the degree of hearing loss. The filter is designed through the state space equation theory which can realize the filter in the time domain and simplify the design flow. Moreover, the theory allows the state variable to be derived and the passive element resistor to be avoided. This property leads that to the die area being reduced and ω_1 and ω_2 can be adjusted easily. The detailed equation of the filter is expressed in Eq. (6).

$$\begin{cases} I_0 = A_0I_0 + B_0I_{in}, \\ I_{out} = C_0I_0 + D_0I_{in}, \end{cases} \tag{6}$$

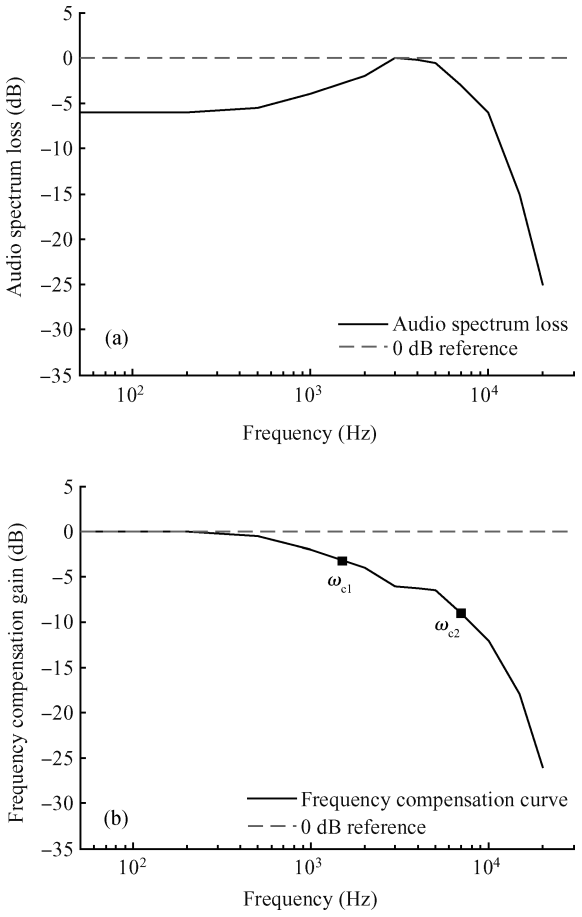


Fig. 7. (a) Diagram of hearing loss. (b) Diagram of frequency compensation.

where I_0, I_{in} and I_{out} stand for the initial state variable, the input current signal, and the output current signal, respectively. The matrixes A_0, B_0, C_0 and D_0 are the initial state matrixes, expressed as follows[10].

$$\begin{cases} A_0 = \begin{bmatrix} -\omega_{c1} & 0 \\ 0 & -\omega_{c2} \end{bmatrix}, \quad B_0 = \begin{bmatrix} 1 \\ 1 \end{bmatrix}, \quad D_0 = 0\ , \\ C_0 = \begin{bmatrix} \dfrac{\omega_{c1}\omega_{c2}\left(1-\dfrac{1}{r}\right)}{\omega_{c2}-\omega_{c1}} & \dfrac{\omega_{c2}\left(\dfrac{\omega_{c2}}{r}-\omega_{c1}\right)}{\omega_{c2}-\omega_{c1}} \end{bmatrix}, \end{cases} \tag{7}$$

where r is equal to ω_{c1}/ω_{c2}. Obviously, the matrixes are not simple, which should result in a complex circuit. So, some reversible optimization is taken to simplify the matrixes, shown in Eq. (8)[11,12].

$$\begin{cases} \dot{I} = AI + BI_{in}, \\ I_{out} = CI + DI_{in}, \end{cases} \tag{8}$$

where I is the state variable after the optimization. The matrixes A, B, C, and D are shown as follows.

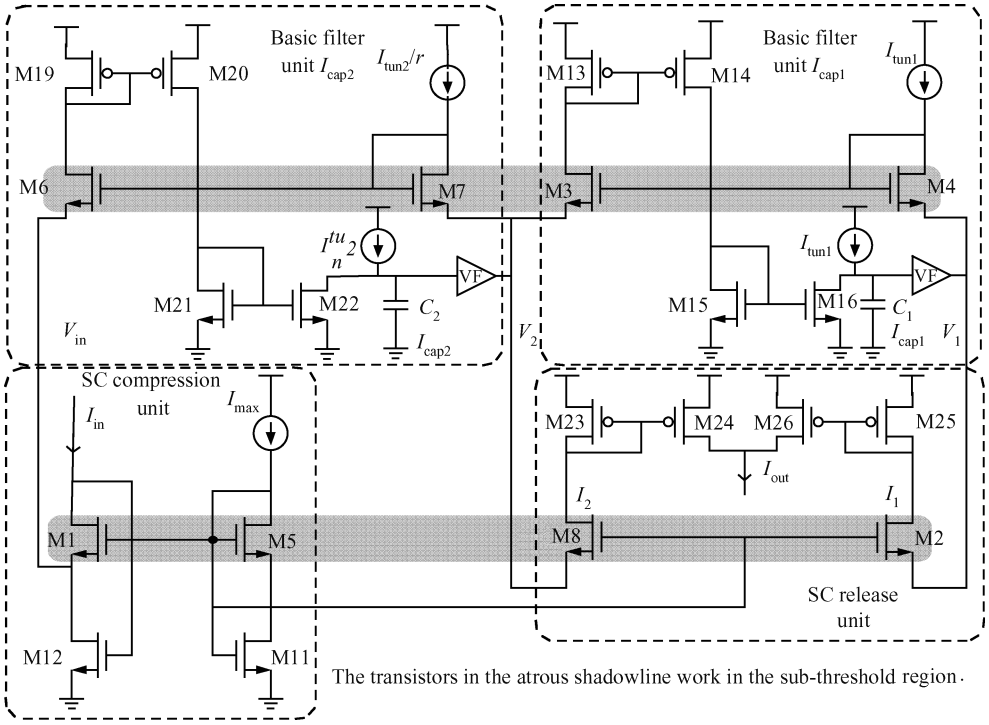
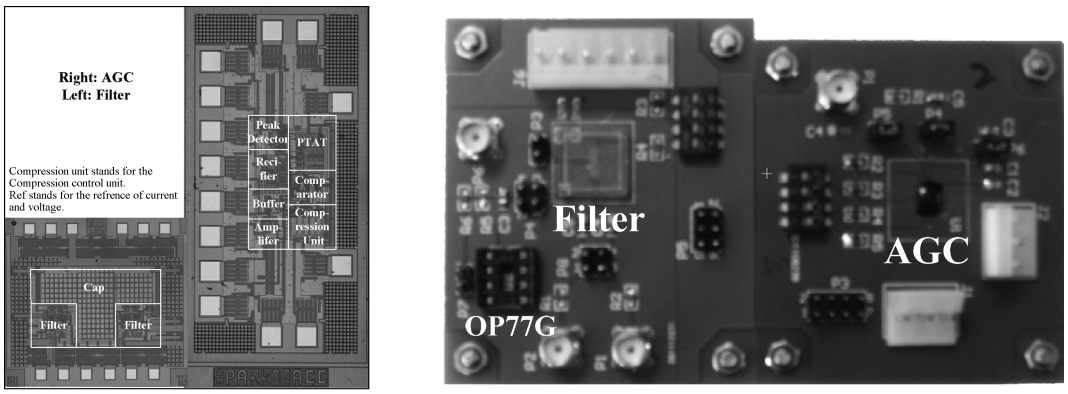


Fig. 8. Schematic diagram of the second-order filter.



(a) (b)

Fig. 9. (a) Die micrographic and (b) the PCB for measurement.

$$\begin{cases} A = \begin{bmatrix} -\omega_{c1} & \omega_{c1} \\ 0 & -\omega_{c2} \end{bmatrix}, \quad B = \begin{bmatrix} 0 \\ \dfrac{\omega_{c2}}{r} \end{bmatrix}, \\ C = [\ 1 \quad 1\ ], \quad D = 0. \end{cases} \tag{9}$$

It is seen that the matrixes are simpler than in Eq. (7). Substitute the two-order state variable $I = [I_1, I_2]$ into Eq. (8), we have the final state space equation of the adaptive filter, which can be directly transformed to the practical circuits, shown in Eq. (10).

$$\begin{cases} I_{cap1} = I_{tun1} - I_{tun1} e^{(V_1 - V_2)/U_t}, \\ I_{cap2} = I_{tun2} - I_{tun2}/r e^{(V_2 - V_{in})/U_t}, \\ I_{out} = I_1 + I_2, \end{cases} \tag{10}$$

where $I_{cap1} = C_1 dV_1/dt$, $I_{cap2} = C_2 dV_2/dt$, $I_{tun1} = U_t C_1\, \omega_{c1}$, $I_{tun2} = U_t C_2\, \omega_{c2}$. I_1, V_1 and I_2, V_2 have a relationship based on the SC mode of Eq. (1). The expression of I_{cap1} and I_{cap2} represents the basic state space equation responding to the basic circuit unit of the current-mode adaptive filter. The detailed circuit of the filter is shown in Fig. 8.

M1, M2, M3, M4, M5, M6, M7, and M8 work in the sub-threshold region. According to Eq. (1), M1, M2 and M8 generate the compression voltage V_{in}, V_1 and V_2 responding to the input signal I_{in}, the state variable I_1 and I_2, respectively. M3, M4, M13, M14, M15, M16, and C_1 realize the expression of I_{cap1} in Eq. (10): the current I_{tun1} transforms to $I_{tun1} e^{(V_1 - V_2)/U_t}$ through M3 and M4 and then is subtracted from I_{tun1} on the top plate of C_1. In the same way, M6, M7, M19, M20, M21, M22, and C_2 realize the expression of I_{cap2}: the current I_{tun2}/r transforms to $I_{tun2}/r e^{(V_1 - V_2)/U_t}$ through M6 and M7, and then

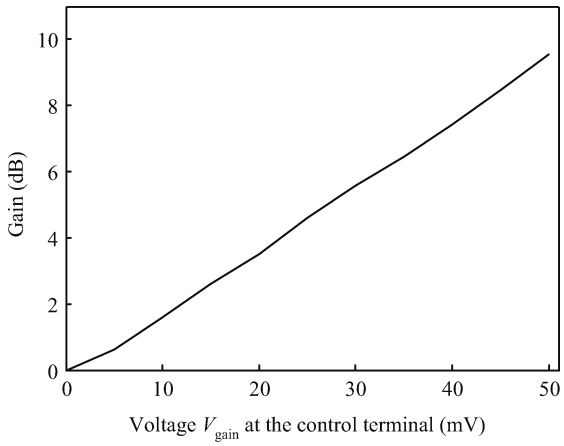


Fig. 10. Curve of continuous gain.

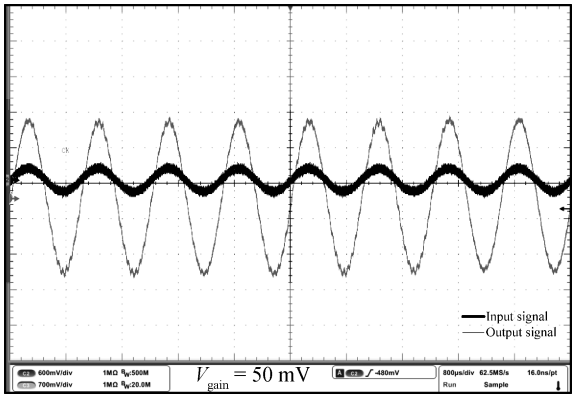


Fig. 11. Input versus output signal at $V_{gain} = 50$ mV.

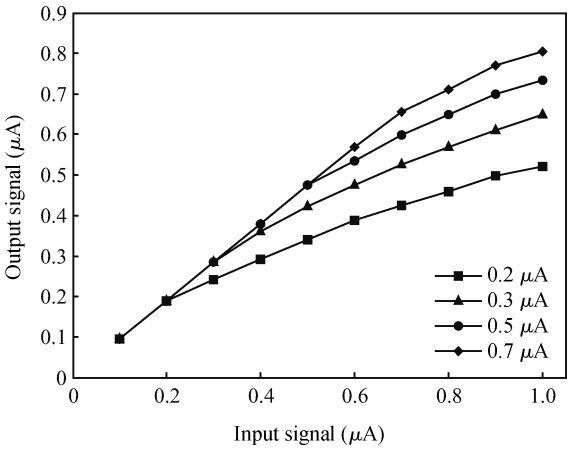


Fig. 12. Curve of knee point.

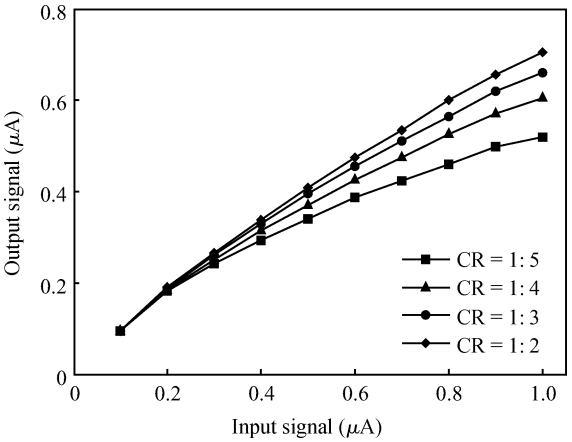


Fig. 13. Curve of compression ratio.

is subtracted from I_{tun2} on the top plate of C_2. Finally, the expression of I_{out} is realized by the current mirrors M23, M24, M25, and M26. When adjusting the value I_{tun1}, I_{tun2}, C_1 or C_2, the ω_{c1} and ω_{c1} can be changed in accordance with the individual difference based on the expression of $I_{tun1} = U_t C_1\ \omega_{c1}$ and $I_{tun2} = U_t C_2\ \omega_{c2}$.

5. Measurement results

The proposed current-mode front-end circuit of an analog hearing aid chip has been fabricated in a standard 0.35 μm CMOS process and occupies 1×0.5 mm^2 and 1×1 mm^2 active die area for the AGC circuit and the filter circuit, as shown in Fig. 9. The whole chip is mounted on a printed circuit board (PCB) and measured with 1.4 V supply voltage. For measurement convenience, some current signals are transferred to the responding voltage signal by an OP77G amplifier.

The identified property of continuous gain of the AGC is shown in Fig. 10. It is seen that a continuous gain with an exponential characteristic can be obtained by changing the voltage V_{gain} at the control terminal. The gain increases with the voltage V_{gain}. The exponential characteristic makes the continuous gain match the sound pressure level and achieves a large dynamic range. The relationship between input signal and output signal in the condition of $V_{gain} = 50$ mV is shown in Fig. 11. The programmability of the chip is improved through the digital control interface and illustrated in Figs. 12 and 13 where the data is measured in the condition of $V_{gain} = 0$. The chip has four knee points (0.2 μA, 0.3 μA, 0.5 μA, 0.7 μA mV) and four compression ratios (1 : 2, 1 : 3, 1 : 4, 1 : 5), which can be customized to suit individual needs based on different degrees of hearing loss.

With $C_1 = 110$ pF and $C_2 = 30$ pF, the frequency compensation function of the filter is illustrated in Fig. 14. It is seen that the gain is around 0 dB when the frequency range is between 100 to 1000 Hz. When the frequency range is between 3 kHz to 10 kHz, the gain is about –5 dB. The frequency range between 1 kHz to 3 kHz is the transition range according to the hearing loss curve in Fig. 7(a). This unique property can compensate for the most common low-frequency hearing loss. Combined with AGC, the knee point curve with frequency compensation is show in Fig. 15 with a typical input frequency of 1 kHz. Obviously, the intensity of the acoustic signal has been decreased, so that the individuals suffering hearing loss can feel more comfortable when the input amplitude is large.

The power consumption at the different gain control voltage V_{gain} is shown in Fig. 16. It is seen that the power consumption increases with the voltage V_{gain}. The minimum power consumption can achieve 40 μW when $V_{gain} = 0$. Figure 17 shows the THD at the different gain control voltages V_{gain}. Clearly, the worst THD is still below −45 dB (peak THD −52 dB @ V_{gain}

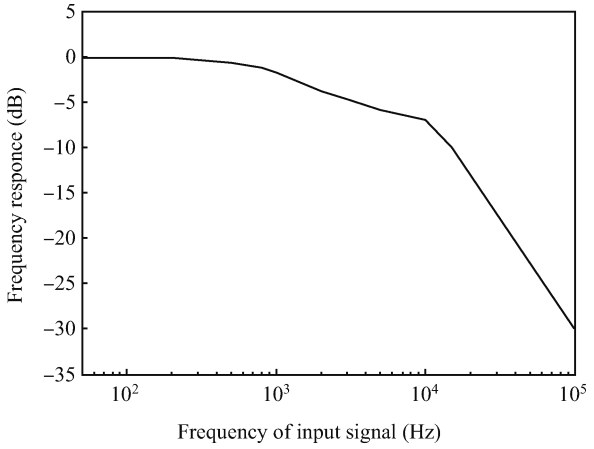


Fig. 14. Curve of frequency compensation.

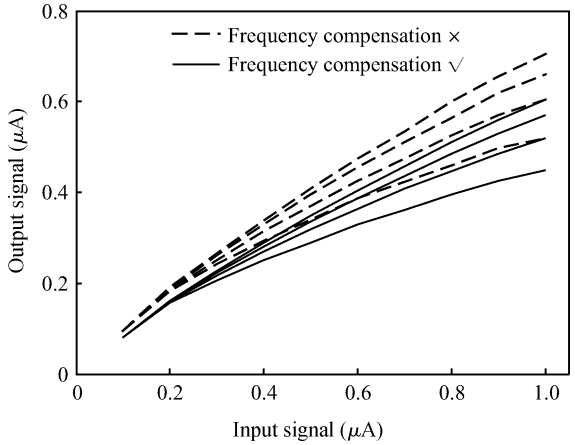


Fig. 15. Knee point curve with frequency compensation versus without frequency compensation.

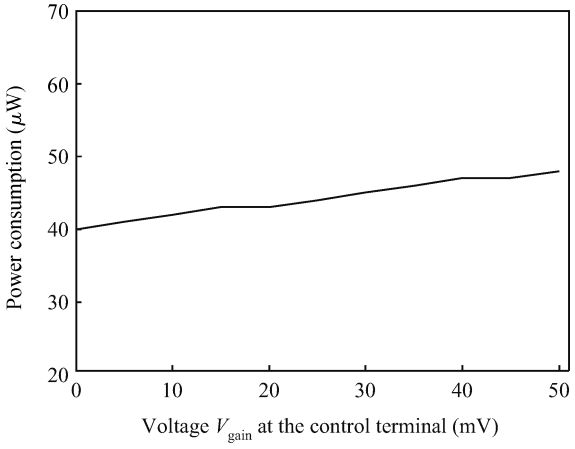


Fig. 16. Curve of power consumption.

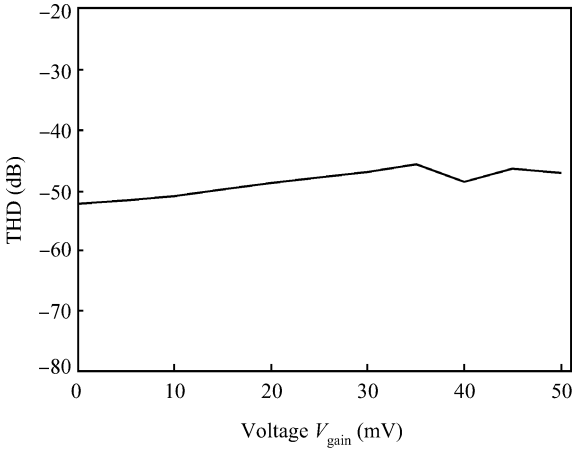
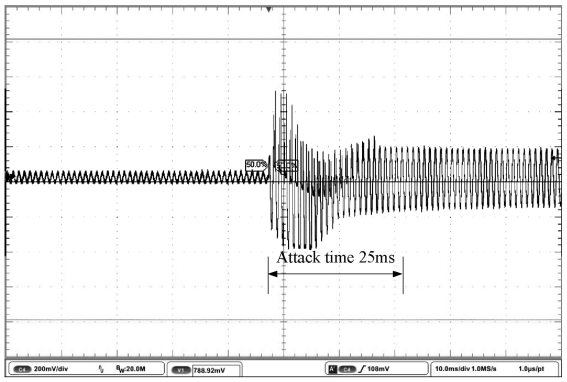
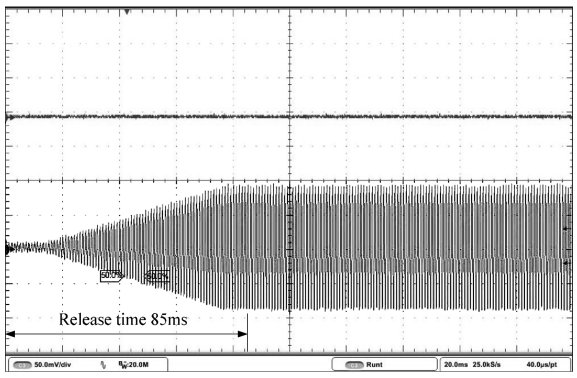


Fig. 17. THD at the different gains.



(a)



(b)

Fig. 18. (a) Diagram of attack time. (b) Diagram of release time.

$= 0$), which is smaller than the critical threshold THD -26 dB according to the acoustic theory. The attack and release time diagram is shown in Fig. 18. With an external capacitor of 60 nF and an internal capacitor of 10 nF, the chip enables the implemention of $T_A = 25$ ms and $T_R = 85$ ms to enhance the comfort level.

The performances compared with other front-end hearing aid circuits are summarized in Table 1. The front-end circuit of this work has the unique function of frequency compensation, which only appears in the DSP unit of the digital hearing aid. Then, the performance of the analog hearing aid can be upgraded in the field of the most common low-frequency hearing loss. Moreover, the continuous gain is presented to be taking advantage of the current-mode technique comparing with the voltage-mode counterparts. Furthermore, the power consumption is below 48 μW with a 1.4 V supply voltage in a high threshold-voltage CMOS process of 0.35 μm due to the compression principle of the current-mode technique. Generally, the supply voltage of the voltage-mode circuit in the 0.35 μm

Table 1. Performance comparison.

Reference	Ref. [12]	Ref. [13]	Ref. [14]	Ref. [15]	This work
Supply voltage (V)	1	0.9	1.2	3	1.4
THD (dB @ 1 kHz)	–35	N/A	–40	–74	–52
Frequency compensation	×	×	×	×	√
Continuous gain	√	×	×	×	√
Power (μW)	300	67	67	835	48
Technique	Current-mode	Voltage-mode	Voltage-mode	Voltage-mode	Current-mode
Process (μm)	1.2	0.25	0.25	0.35	0.35

CMOS process is 3.3 V, which is higher than 1.4 V[15]. The THD is below -45 dB and the minimum THD is -52 dB.

6. Conclusion

A complete low-voltage and low-power front-end circuit of analog hearing aid has been designed and integrated in a standard 0.35 μm CMOS process with a high threshold-voltage ($V_{\rm TON} + |V_{\rm TOP}| \approx 1.35$V) using the current-mode technique. Introducing this technique, the unique function of continuous gain and frequency compensation is implemented. The continuous gain function can meet any degree of amplitude hearing loss. And the frequency compensation function can upgrade the performance of the analog hearing aid in the field of the ambient low-frequency hearing loss attributing to the state space design method. With a 1.4 V supply voltage, the power consumption is only 48 μW and the THD is below -45 dB. Moreover, the chip is very flexible providing four knee points and four compression ratios and is accordant to the human factor with the attack time of 25 ms and release time of 85 ms. Conclusively, the front-end circuit can provide superb performance for normal hearing loss considering the human factors.

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