Charge transfer efficiency improvement of a 4-T pixel by the optimization of electrical potential distribution under the transfer gate*

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Abstract: The charge transfer efficiency improvement method is introduced by optimizing the electrical potential distribution under the transfer gate along the charge transfer path. A non-uniform doped transfer transistor channel is introduced to provide an ascending electrical potential gradient in the transfer transistor channel. With the adjustments to the overlap length between the R1 region and the transfer gate, the doping dose of the R1 region, and the overlap length between the anti-punch-through (APT) implantations and transfer gate, the potential barrier and potential pocket in the connecting region of transfer transistor channel and the pinned photodiode (PPD) are reduced to improve the electrical potential connection. The simulation results show that the percentage of residual charges to total charges drops from $1/10^4$ to $1/10^7$, and the transfer time is reduced from 500 to 110 ns. This means the charge transfer efficiency is improved.

Key words: CMOS image sensor; charge transfer efficiency; non-uniform doped transfer transistor channel; potential barrier; potential pocket

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1. Introduction

The CMOS image sensor (CIS) has been experiencing explosive growth in recent years, thanks to its lower cost, lower power consumption, higher integration, and the ability to integrate sensing with analog and digital processing down to the pixel level[1, 2]. The photo-detectors generally used in CIS include photogates (PGs), photodiodes (PDs), and pinned photodiodes (PPDs). Compared with the PD and the PG, the structure of a PPD provides an improved blue light response[3]. Moreover, the PPD exhibits a high dark current characteristic by separating the charge storage region from the Si/SiO_2 interface[4]. The absence of true correlated double sampling (CDS) in three-transistor (3-T) pixels and five-transistor (5-T) pixels leads to high noise[5]. So, the four-transistor (4-T) pixel with PPD photo-detector is the most popular CIS architecture at present.

The CIS has been widely applied in surveillance, scientific research, and medical and industrial imaging. Many fields demand not only high sensitivity, high full well capacity, low dark current, and noise but also no image lag and a fast readout of hundreds or even thousands of frames per second[6, 7]. Image lag refers to the residual signal charges in a PPD after readout, which can be extracted again during successive readings of the pixel. This leftover information degrades the image quality seriously. Image lag and the readout speed of a 4-T pixel are mainly determined by the charge transfer efficiency. Charge transfer efficiency of a 4-T pixel is the percentage of signal charge which is successfully transferred from the PPD to floating diffusion (FD) during the readout operation, and the charge transfer time.

Charge transfer efficiency is determined by the electrical potential distribution along the transfer path from the PPD to the FD, including the PPD, the transfer transistor channel, and the connecting region between them. The electrical potential distribution in a PPD can be optimized by using multi n-type implants or triangular-shaped photodiodes[8, 9]. The electrical potential distribution in a transfer transistor channel and the connecting region between the transfer transistor channel and the PPD can be optimized by using a peninsula-shaped or L-shaped transfer gate layout[10, 11]. The corner located near the maximum potential of the PPD is received, but at the cost of lowering fill factor and sensitivity.

In this paper, optimization of the electrical potential distribution under a transfer gate is introduced to improve the charge transfer efficiency. Two techniques are implemented for this purpose. The non-uniform doped channel optimizes the electrical potential distribution in the transfer transistor channel, and adjustments to the R1 region and anti-punch-through (APT) implantations optimize the electrical potential distribution in the connecting region between the transfer transistor channel and the PPD. All the simulations were based on 0.18-μm CMOS process.

2. Electrical potential distribution optimization in the transfer transistor channel

All improvements in this paper are based on a CMOS four-transistor (4-T) pixel structure, as shown in Fig. 1. The four-transistor pixel includes a pinned photodiode (PPD), a transfer transistor (MTG), a floating diffusor (FD), a source follower (SF), a reset transistor (MRST), and a row select transistor

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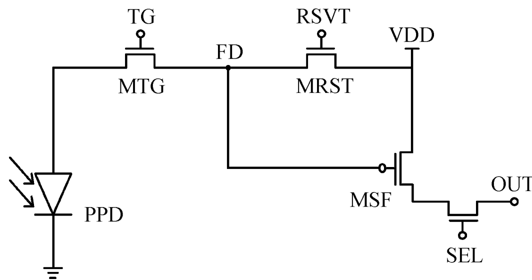

Fig. 1. Structure of the 4-T pixel.

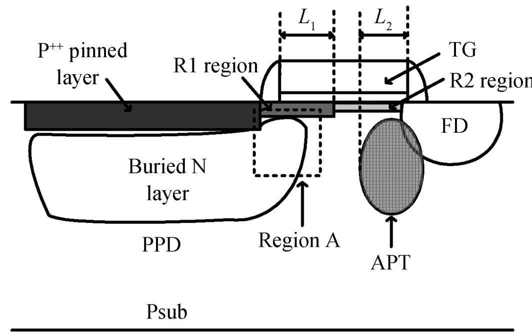

Fig. 2. Architecture of the PPD and the transfer transistor.

(SEL).

Theoretically, the photosensitive region of a PPD converts incident electromagnetic energy into accumulated signal electrons. A PPD consists of a P^{++} pinned layer, a buried N layer, and a p-type substrate, as shown in Fig. 2. Signal electrons are stored in the buried N layer by the force of the electric field in the depleted region. Region A, which is shown in Fig. 2, is the connecting region between the transfer transistor channel and the PPD. When the transfer gate (TG) turns on, electrons are first extracted to region A, then the channel, and then finally move to the FD. The excellent electrical potential distribution required for high charge transfer efficiency should be gradually ascended along the transfer path from the PPD to the FD. This ascending electrical potential gradient pushes electrons step by step, and enhances the transfer.

The electrical potential in a conventional conducting transfer transistor channel does not vary apparently, and the lateral electric field in the channel pulling the electrons to the FD is not strong. Signal carriers are extracted solely by the high electrical potential in the FD. This may result in the channel being unable to remove all the electrons in the PPD and increase occurrences of image lag. An electrical potential gradient in the channel ascended from the PPD to the FD can overcome this obstacle. The ascending potential gradient forms the lateral electric force which pushes electrons to the FD. Therefore, the signal electrons in the channel receive a lateral force to move, and charge transfer is improved.

It can be proved that the threshold voltage is

$$V_{\mathrm{TH}} = \phi_{\mathrm{MS}} + 2(kT/q)\ln(N_{\mathrm{A}}/n_{\mathrm{i}}) + \frac{Q_{\mathrm{dep}}}{C_{\mathrm{ox}}}, \quad (1)$$

where ϕ_{MS} is the difference between the work function of the poly-Si gate and the silicon channel, q is electron charge, N_{A}

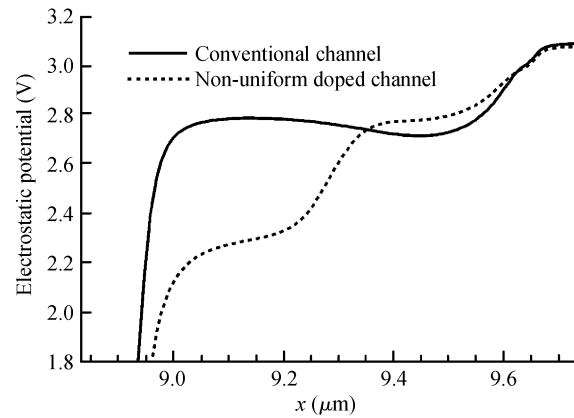

Fig. 3. Potential profile of the non-uniform doped channel and the conventional uniform doped channel.

is the channel doping concentration, n_{i} is the intrinsic carrier concentration, Q_{dep} is the charge in the depletion region, and C_{ox} is the gate oxide capacitance per unit area, which appears fixed in a given process. From PN junction theory, $Q_{\mathrm{dep}} = \sqrt{4q\varepsilon_{\mathrm{si}}\left|(kT/q)\ln(N_{\mathrm{A}}/n_{\mathrm{i}})\right| N_{\mathrm{A}}}$, where $\varepsilon_{\mathrm{si}}$ denotes the dielectric constant of silicon. A conclusion which can be drawn by Eq. (1) is that the high threshold voltage can be obtained by the high doping concentration. When the applied voltage is sufficient for forming an inversion layer, a high doping concentration leads to a low electrical potential in the channel.

Compared with the conventional uniform doped channel, the ascending electrical potential gradient is formed by the non-uniform doped transfer transistor channel with two different implants. The non-uniform doped channel region divides into two sub-regions, as shown in Fig. 2. The first sub-region close to the PPD with the first high doping dose implant is called the R1 region and the second sub-region close to the FD with the second low doping dose implant is called the R2 region. When TG turns on, the non-uniform doped channel forms the potential gradient ascended from the R1 region to the R2 region. On the other hand, when TG turns off, the relatively high doping concentration of the R1 region can raise a potential barrier to prevent the inversion carriers from drawing back to the PPD. These inversion carriers will increase the dark current induced by the partition noise of the TG[12]. The electrical potential gradient is shown in Fig. 3.

As the ascending electrical potential gradient in the channel forms, the signal electrons are extracted more easily than in the conventional channel. Figure 4 shows the residual charge density of different transfer transistor channels at coordinate $x = 5$ μm, which is in the middle of an 8 μm length of the simulated PPD. TG voltage is set to 3.3 V for a long time so that the density of the electrons in the PPD keep steady. This means all the signal electrons which can be extracted have been moved to the FD. In the same charge density before transfer, the maximum residual charge density after transfer drops from 2.92×10^{11} to 2.24×10^{8} cm^{-3}. With the ascending electrical potential gradient, there are fewer residual electrons, and the percentage of transferred electrons to total electrons becomes larger. Charge transfer efficiency is improved.

The non-uniform doped channel is obtained by twice different implants, but the anti-punch-through (APT) implanta-

Table 1. Maximum density of residual electrons in the PPD. Unit: cm^{-3}

Doping dose / Doping energy	3×10^{12} cm^{-2}	4×10^{12} cm^{-2}	5×10^{12} cm^{-2}	6×10^{12} cm^{-2}
50 keV	2.24×10^{8}	8.11×10^{8}	1.00×10^{9}	1.38×10^{9}
30 keV	8.12×10^{8}	9.92×10^{9}	1.40×10^{9}	2.02×10^{9}
10 keV	8.73×10^{10}	3.02×10^{11}	8.19×10^{11}	1.97×10^{12}

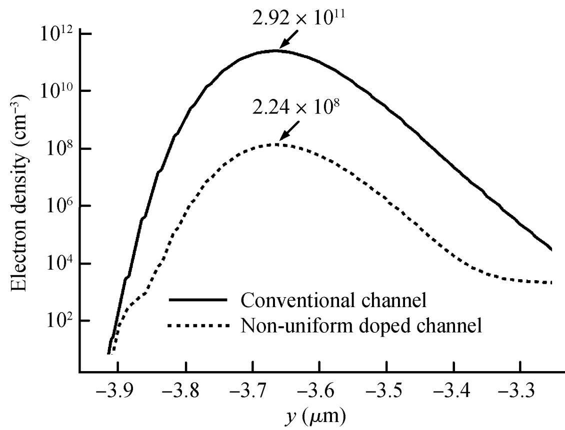

Fig. 4. Residual charge density at $x = 5$ μm.

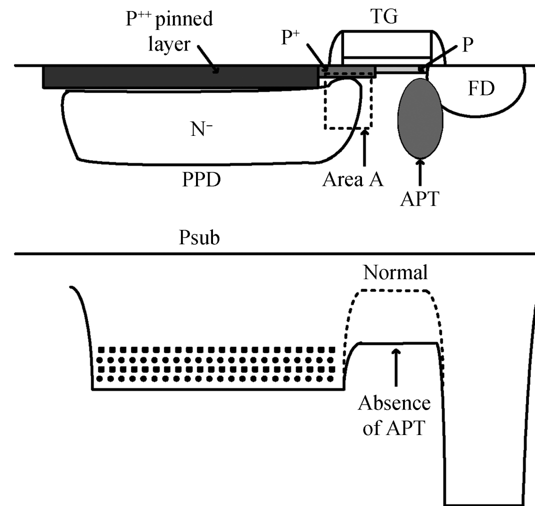

Fig. 5. Electronic potential energy diagram for the effect of APT implantations in guaranteeing FWC.

tions will affect this channel. The full well capacity (FWC) limits both the dynamic range (DR) and the maximum signal to noise ratio (SNR) of the CIS[13]. The potential barrier height, which is disposed between the PPD and the FD, limits the improvement of FWC. A potential barrier is a low potential region as well as a high electronic potential energy region. When the TG turns off, photo-generated electrons in the PPD with more energy than the barrier energy may be extracted to the FD by the attraction of the high electrical potential in the FD. The low potential barrier can hardly prevent the loss of signal electrons. It forms the leakage current before the intended transfer period and leads to the shrinking of FWC.

According to PN junction theory, the built-in voltage is

$$V_{\mathrm{D}} = \frac{k_0 T}{q} \ln \frac{N_{\mathrm{D}} N_{\mathrm{A}}}{n_{\mathrm{i}}^2}, \tag{2}$$

where N_{D} is the doping concentration of N-type impurities, N_{A} is the doping concentration of P-type impurities, q is electron charge, and n_{i} is the intrinsic carrier concentration. It concludes that the high doping dose of P-type impurities improves the built-in voltage. The high doping concentration between the PPD and the FD can raise a high potential barrier. The p-type APT implantations disposed under the transfer transistor channel close to the FD meet the high doping concentration requirement. APT implantations consist of multi implants to provide an adequate junction depth for a wide range of potential barriers. The absence of APT implantations leads to the low potential barrier between the PPD and the FD, and the FWC shrinks. APT implantations guarantee the FWC. It is shown in Fig. 5.

The top implant in APT implantations will affect the ascending potential gradient in a channel. Low doping energy will lead to the diffusion of the p-type impurities to the channel, especially with the high doping dose. The diffusion increases the doping concentration in the R2 region, and reduces the difference with R1 region. This leads to a potential barrier even eliminating the ascending electrical potential gradient in the transfer transistor channel.

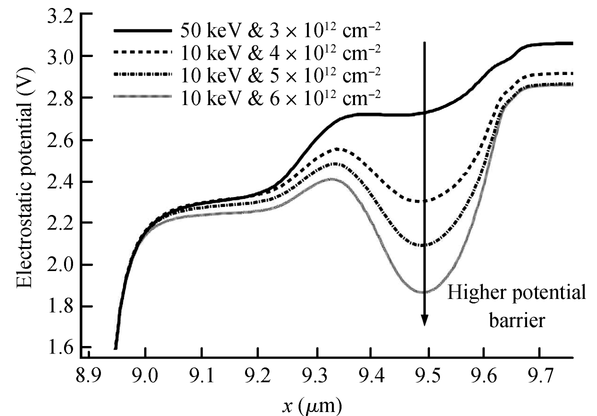

Fig. 6. Channel potential profiles for top APT implant doping dose and doping energy optimization.

The channel electrostatic potential profile of 10 nm below the surface with doping energy and doping dose split of the top APT implant is shown in Fig. 6. It shows that the lower doping energy with a higher doping dose results in a higher potential barrier. Table 1 shows the maximum density of residual electrons in the PPD with different doping dose and energies of the top APT implant. It can be concluded that the lower doping energy and higher doping dose lead to more residual electrons and a smaller percentage of transferred electrons. The impact of doping energy is more significant. Therefore, the top APT implant should employ low doping energy with a low doping dose to ensure that there is no potential barrier in the ascending electrical potential gradient channel.

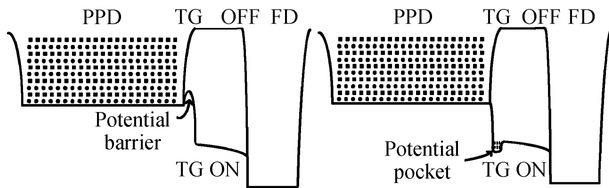

Fig. 7. Potential barrier and potential pocket in the connecting region between the transfer transistor channel and the PPD.

3. Electrical potential distribution optimization in the connecting region between the transfer transistor channel and the PPD

Another limitation to improve charge transfer efficiency is the potential barrier and potential pocket in the connecting region between the transfer transistor channel and the PPD, which is depicted in Fig. 7. The potential barrier prevents electrons with lower energy than that of the barrier moving to the transfer channel. The potential pocket is a high potential region, as well as electronic potential energy well, which accumulates electrons. Any potential barrier or potential pocket in the connecting region (region A as shown in Fig. 2) will weaken the electrical potential connection between the transfer channel and the PPD, prolong the charge transfer time, and deteriorate the charge transfer efficiency.

Too low electrical potential in region A induces a potential barrier, on the country a potential pocket. The electrical potential in region A is mainly determined by the R1 region and APT implantations. The electrical potential lands from the TG through the R1 region. The change of R1 region induces a variation of electrical potential. APT implantations can pinch off the potential from the FD side, lower the electrical potential and induce a potential barrier. Therefore, the optimization of both the R1 region and APT implantations will be of great help.

3.1. R1 region overlap length adjustment

The overlap length of the R1 region is L_1, as depicted in Fig. 2. A long L_1 length can pinch off the potential from the top side of region A, and induces a potential barrier. This potential barrier weakens the lateral electric filed applied to the photo generated electrons in the PPD and the electrical potential connection between channel and PPD. It causes a lack of motivation for carriers to transfer and an increase in image lag. However, a short L_1 length causes hot-carrier induced impact ionization and trap-induced leakage current, which degrade the sensor performance severely[14].

When the TG is switched on for a long time, the transfer time will be taken as the time that the residual signal charge density in the PPD stays steady after readout. The percentage of residual charges to total charges reduced to $1/10^7$ will be taken as the complete charge transfer, and the corresponding charge transfer time will be regarded as the complete charge transfer time. For example, one result of a two-dimensional simulation for transient analysis of the readout operation is shown in Fig. 8. It represents the transition of signal electrons in the PPD within 400 ns from the start of the readout operation. In the early period of readout operation within 120 ns, the electrons

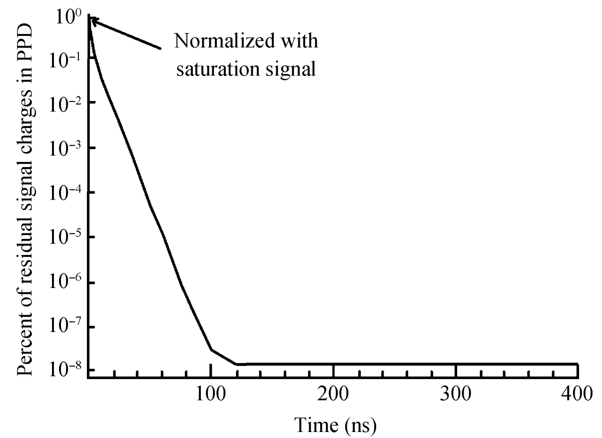

Fig. 8. Transient readout operation.

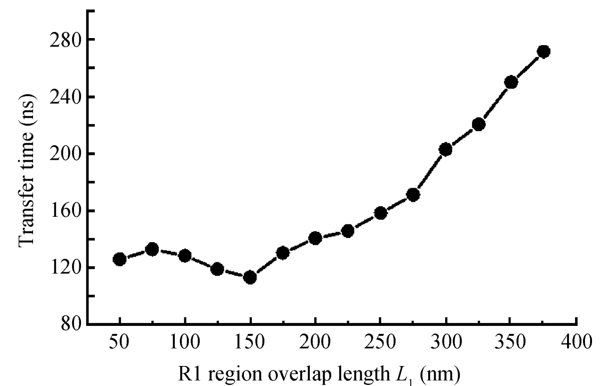

Fig. 9. Complete charge transfer time for R1 region overlap length optimization.

decreased, and after that, the transition stayed steady. So the transfer time could be taken as 120 ns. While the percentage of signal electrons decreased to $1/10^7$, 120 ns could be regarded as the complete charge transfer time. The simulations were based on a large sized pixel with an 8 μm length of PPD. All the transfer time and complete transfer time simulation methods in this paper are the same.

Complete charge transfer time with a split of L_1 is depicted in Fig. 9. The results show that a short L_1 length prolongs the transfer time due to potential pocket, while a long L_1 length also extends the transfer time depending on the potential barrier. Only an appropriate L_1 length can reduce the complete charge transfer time and improve charge transfer efficiency.

3.2. R1 region doping dose adjustment

The R1 and R2 regions compose the non-uniform doped channel. The doping dose of the two regions represents the channel potential gradient. The more the doping dose two regions differ, the greater gradient for charge transfer is obtained. However, the high dose of the R1 region will pinch off the potential in region A, and cause a potential barrier to extend the transfer time. On the contrary, a low-dose of the R1 region not only weakens the ascending electrical potential gradient in the channel, but also increases the dark current. It causes a potential pocket which accumulates signal electrons, and prolongs the complete charge transfer time.

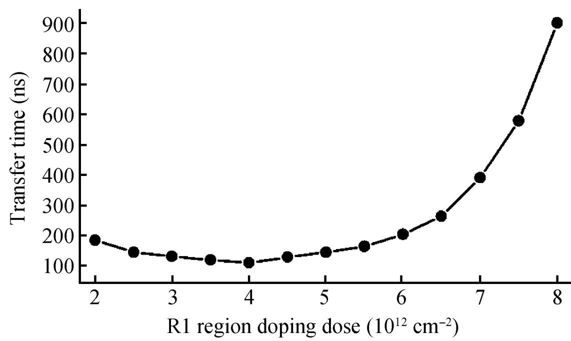

Fig. 10. Complete charge transfer time for R1 region doping dose optimization.

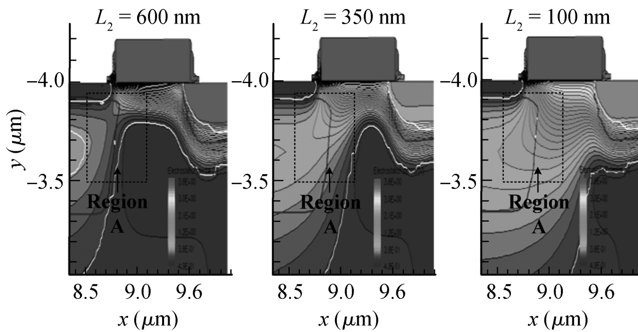

Fig. 11. Electrostatic potential profiles during charge transfer under the TG for APT implantation overlap length optimization.

Figure 10 depicts the complete charge transfer time when the R1 region doping dose varies from 2×10^{12} to 8×10^{12} cm^{-2}. It is concluded that more time is needed for a low doping dose because of the potential pocket, and the same applies to a high doping dose due to the potential barrier. The minimum complete charge transfer time is obtained at the doping dose of 4×10^{12} cm^{-2}.

3.3. APT implantations overlap length adjustment

Depending on its deep junction, which prevents the leakage current, APT implantations can pinch off the potential of region A from the FD side in a wide range and induce a potential barrier. The overlap length between APT implantations and the TG is L_2, as shown in Fig. 2. Given the much higher doping concentration in the FD, if L_2 is too short, it will be covered and lose the effect of avoiding leakage. Compared with the R1 region, APT implantations can pinch off the electrical potential of region A from the FD side in a wider range, and raise a much higher potential barrier. The height of the potential barrier mainly depends on the length of L_2.

Figure 11 shows the electrostatic potential profile with different length of L_2, split as 100 nm, 350 nm, and 600 nm. The electrical potential of region A was pinched off starting at 350 nm and completed pinched off at 600 nm. The path to transfer is totally cut off. It suggests that the increasing length of L_2 contributes to an increase in height of the potential barrier.

Figure 12 shows the effect of avoiding leakage and complete charge transfer time with different L_2 overlap lengths. The electrons in Fig. 12 were obtained when the FD was reset

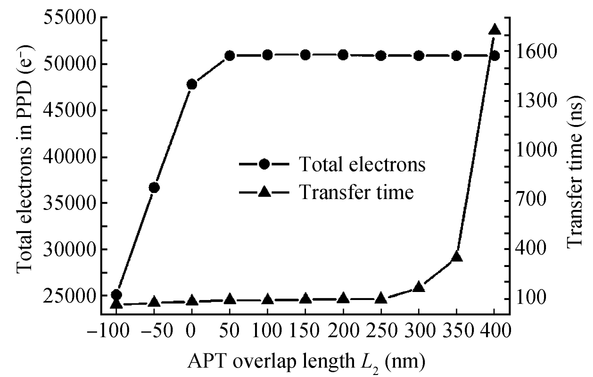

Fig. 12. Residual electrons and complete charge transfer time for APT implantation overlap length optimization.

by MRST. Because of the highest potential of the FD throughout the whole frame, it is the worst situation for the role of APT implantations. The initial total electrons are 50700 and a length of L_2 less than 50 nm reduces the effect of avoiding leakage. The complete charge transfer time with the split of L_2 is also shown in Fig. 12. It fluctuates within a small range when L_2 is less than 250 nm, while complete transfer time increases considerably when L_2 was longer than that due to the potential barrier. Therefore, complete charge transfer time is almost the same when L_2 is between 50 nm to 250 nm. Given the misalignment of APT implantations, the optimization of L_2 will be taken as 150 nm.

4. Simulation results and discussion

The electrical potential distribution in the transfer transistor channel is optimized by the ascending electrical potential gradient with a non-uniform doped transfer transistor channel. Twice different implantations of the R1 and R2 regions form the non-uniform doped transfer transistor channel. The adjustment to the top implant in the APT implantations avoids an additional potential barrier in this channel region at the FD side. The electrical potential distribution in the connecting region between the transfer transistor channel and the PPD is optimized by the reduced potential barrier and potential pocket, with the adjustments to the overlap length between R1 region and TG, the doping dose of R1 region, and the overlap length between APT implantations and the TG. A short overlap length and low doping dose of the R1 region will induce a potential pocket, and on the contrary the potential barrier. Only an appropriate overlap length and doping dose can reduce the potential pocket and the potential barrier. Based on the role of avoiding leakage, an appropriate overlap length between APT implantations and the TG will lower the potential barrier.

The optimal process conditions after optimization are shown in Table 2. Table 3 shows comparisons with an optimized pixel, a conventional pixel before optimization, Ref. [11], and Ref. [15]. The order of charge density in the PPD drops from 10^{15} to 10^{11} cm^{-3} after transfer for the conventional pixel, while the order of charge density drops from 10^{15} to 10^{8} cm^{-3} for the optimized pixel. The percentage of residual charges to total charges is $1/10^{4}$ for the conventional pixel, and this percentage is $1/10^{7}$ for an optimized pixel. This means

Table 2. Optimal process conditions.

Parameter	R1 region	R2 region		APT implantation	
Doping impurity	BF2	BF2	Boron	Boron	Boron
Doping dose (cm^{-2})	4×10^{12}	1×10^{12}	3×10^{12}	2×10^{12}	1×10^{12}
Doping energy (keV)	15	15	50	110	170
Overlap length (nm)	150	550	150	150	150

Table 3. Comparisons with the optimized pixel, conventional pixel, and related references.

Parameter	Optimized pixel	Conventional pixel	Ref. [11]	Ref. [15]
Length of PPD (μm)	8	8	< 7.4	NA
The order of residual charge density (cm^{-3})	10^8	10^{11}	NA	NA
The percentage of residual charges to total charges	$1/10^7$	$1/10^4$	$1/10^7$	NA
Transfer time (ns)	110	500	NA	1000

a larger percentage of transferred charges to total charges after optimization. The simulated pixel in Ref. [11] has the same percentage of residual charges to total charges, which is $1/10^7$, but with a short length of PPD. The length of the pixel in Ref. [11] is 7.4 μm, and the PPD length is not available, but it must be shorter than the pixel length. A long PPD length has a weakened lateral electric field in the PPD, which is difficult for charge transfer. So, the optimized pixel is better than Ref. [11]. On the other hand, with the optimization, the charge transfer time is reduced from 500 to 110 ns. The typical measured transfer time is 1 μs[15]. The charge transfer efficiency is improved by a larger percentage of transferred charges to total charges and a smaller transfer time.

5. Conclusion

The electrical potential distribution under the transfer gate in a transfer transistor channel and the connecting region between a transfer transistor channel and a PPD is the critical factor for charge transfer efficiency improvement. Two techniques are investigated to optimize the potential distribution. The first one is using a non-uniform doped transfer transistor channel to form the ascending electrical potential gradient in the channel. The second one is using the reduced potential barrier and potential pocket in the connecting region between transfer channel and the PPD to optimize the electrical potential distribution, with adjustments to the R1 region and APT implantations. A larger percentage of transferred charges to total charges and a smaller transfer time are obtained by using these two techniques. The charge transfer efficiency is improved. Compared with the conventional 4-T pixel process, the whole optimization can be achieved at the expense of one more mask for non-uniform doped transfer transistor channel implantations, which is easy for process purposes. The simulation results can be used by pixel designers to improve the charge transfer efficiency of 4-T pixels.

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