An integrated CMOS high data rate transceiver for video applications*

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Abstract: This paper presents a 5 GHz CMOS radio frequency (RF) transceiver built with 0.18 μm RF-CMOS technology by using a proprietary protocol, which combines the new IEEE 802.11n features such as multiple-in multiple-out (MIMO) technology with other wireless technologies to provide high data rate robust real-time high definition television (HDTV) distribution within a home environment. The RF frequencies cover from 4.9 to 5.9 GHz: the industrial, scientific and medical (ISM) band. Each RF channel bandwidth is 20 MHz. The transceiver utilizes a direct up transmitter and low-IF receiver architecture. A dual-quadrature direct up conversion mixer is used that achieves better than 35 dB image rejection without any on chip calibration. The measurement shows a 6 dB typical receiver noise figure and a better than 33 dB transmitter error vector magnitude (EVM) at –3 dBm output power.

Key words: CMOS; RF transceiver; WLAN; wireless HDTV
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1. Introduction

In recent years, the remarkable explosive growth in personal wireless communications continues to stimulate advances on multiple fronts. A strong demand for wireless distribution of analog and digital TV signals has pushed wireless local area network (WLAN) devices to be rapidly adopted in many high data rate applications[1−7]. However, existing WLAN technologies such as IEEE 802.11a/b/g have problems in real time video streaming applications with a high quality of service (QoS) and are not suitable for time jitter sensitive multimedia applications where a guaranteed constant throughput is required. Most of the standard multimedia processors, such as the moving pictures experts group (MPEG) 2/4, H.264, and WM9 encoder/decoder, do not support data streams with the TCP/IP protocol. Thus, WLAN solutions always need additional "glue" logics, or so-called transcoding, to bridge the TCP/IP data protocol to the video transport stream (TS) before it can interface with standard video processors[8,9]. Ultra wideband (UWB) or IEEE 802.15.3a is another standard proposal for wireless connectivity of multimedia devices. Its physical (PHY) layer only supports a short range of a few meters. The lack of penetration through objects such as walls and the human body makes the UWB solution unsuitable for wireless multimedia distribution over large distances.

WiVi^{TM} technology is Amedia Networks' proprietary technology for broadband wireless multimedia distribution technology. The PHY layer of WiVi^{TM} technology shares the same foundation of that in 802.11n and employs MIMO space-time coding technology[10]. The media access control (MAC) layer of WiVi^{TM} technology employs the same isochronous architecture and time-division-multiple-access (TDMA) networking technology as in UWB to guarantee a high QoS for real-time video[10, 11]. This unique "hybrid" architecture has made WiVi^{TM} technology the only 5 GHz wireless solution capable to deliver high QoS video over a long distance (up to 70 m) while maintaining the original quality.

This paper presents a 4.9 to 5.9 GHz CMOS RF transceiver developed for Amedia's high quality wireless video/audio distribution solution. Like the IEEE 802.11a/g standards, the RF channel spacing is 20 MHz; the modulation is orthogonal frequency division multiplexing (OFDM) with 52 sub-carriers. The technical requirements of the RF transceiver are very similar to the one for IEEE 802.11a applications.

2. Radio architecture

Due to the unrelenting demand for simultaneous improvements in performance, cost, and power consumption, we have adopted this low power 5 GHz CMOS RF transceiver design in a 0.18 μm RF-CMOS process. A block diagram of the RF transceiver is shown in Fig. 1. We utilize a single conversion low IF architecture to form the two identical receivers. The IF frequency has been selected as 10 MHz, which can minimize the complexity of the IF channel selection low pass filter and satisfy the image rejection requirements of the RF image rejection mixer. The transmitter employs a direct up conversion topology due to the requirements that the transmitting EVM should be better than –30 dB and that the image rejection should be a minimum of 35 dB[2, 3, 5, 8, 9]. As we know, using conventional single quadrature up conversion image rejection mixers without the automatic on-chip calibration of transmit I/Q mismatch causes major yield losses in mass production due to process and temperature variations. For this reason, we choose the dual quadrature up conversion mixer topology, as shown in Fig. 2. The dual quadrature up conversion mixer topology with a 2-stage RC polyphase filter (PPF) can substantially reduce the requirements on transmit I/Q mismatch and

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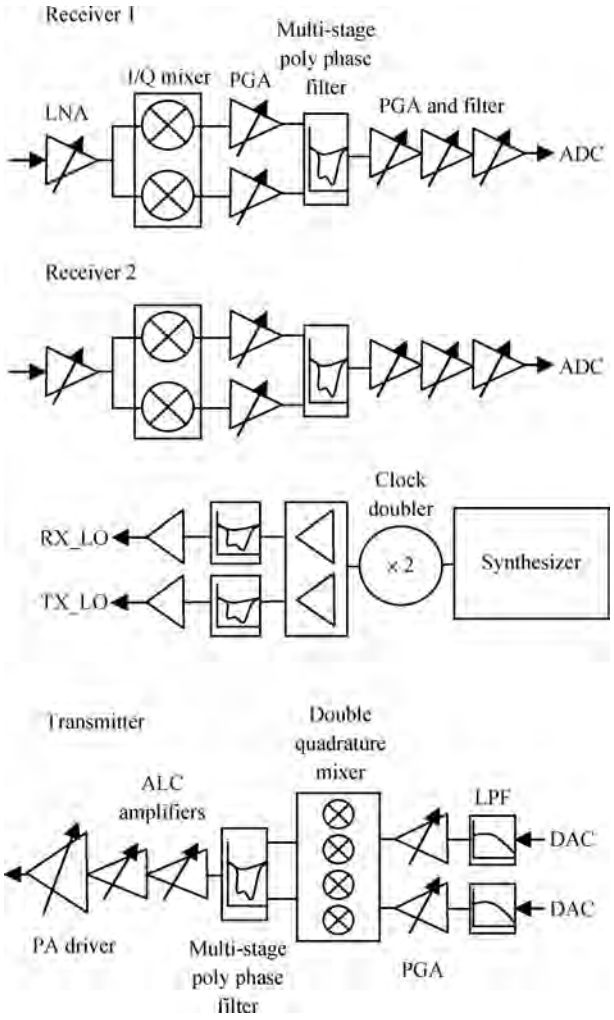


Fig. 1. Dual-receiver radio block diagram.

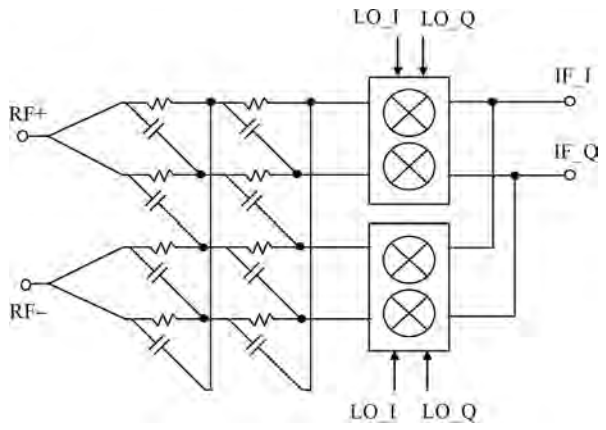


Fig. 2. Dual quadrature up conversion mixer schematic.

achieve the 35 dB image rejection, without on-chip I/Q mismatch calibration.

3. Receiver design

The receiver low noise amplifier (LNA) and image rejection mixer schematic is shown in Fig. 3. A common-source differential LNA with inductive degeneration is used. By switching the output current to either the inductive load or the power supply, the LNA gain can be switched from 20 to 14 dB. Binary switchable capacitors are used as part of the load capacitance for changing the LNA frequency response to optimize its performance in different RF bands. Passive ring mixers are used as the image rejection down conversion mixer. The NMOS switches used in the mixer are carefully biased to track process and temperature variations in order to minimize the impacts of these variations on the mixer's conversion gain and IP3 performance, while minimizing the needed local oscillator (LO) drive levels.

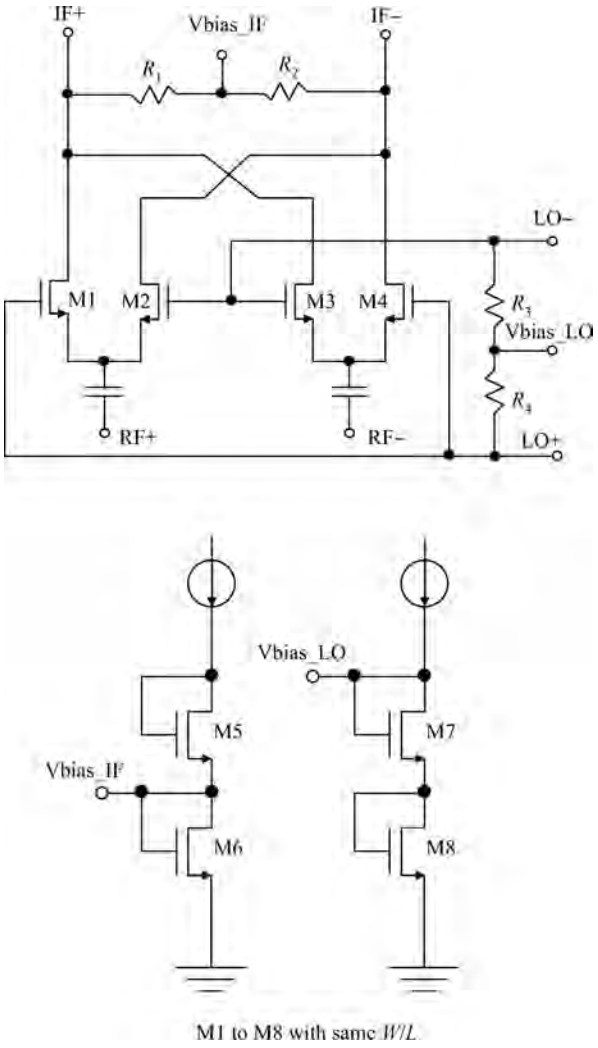


Fig. 3. Dynamically biased down-conversion mixer.

A 6th order lowpass filter is used as the baseband channel selection filter. It has been implemented as a cascade of three Sallen-key biquads using a simple source follower as the unity gain buffer. Four programmable gain amplifier (PGA) stages are used to provide more than 60 dB gain control range with a 1.5 dB gain step at IF frequency. Each Sallen-key biquad is followed by one PGA stage, in order to obtain the best trade-off of noise, IP3, and power consumption performance for each of these filter and PGA circuit blocks. An analog received signal strength indicator (RSSI) circuit monitors the broadband signal levels at the first PGA output, before channel selection filtering. This RSSI signal is converted by an on-chip 8-bit ADC and

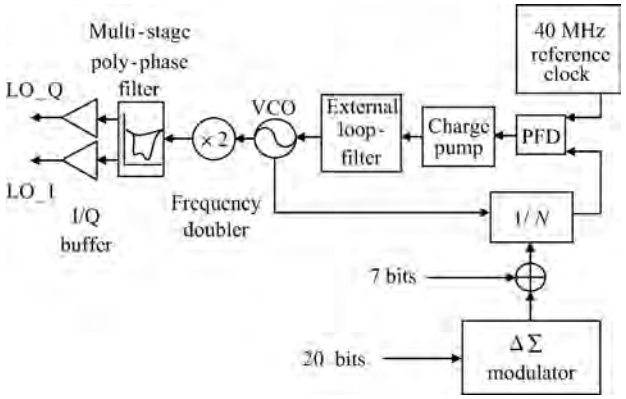


Fig. 4. Frequency synthesizer block diagram.

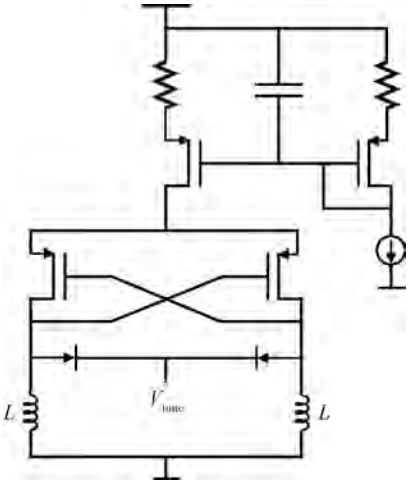


Fig. 5. PMOS only VCO.

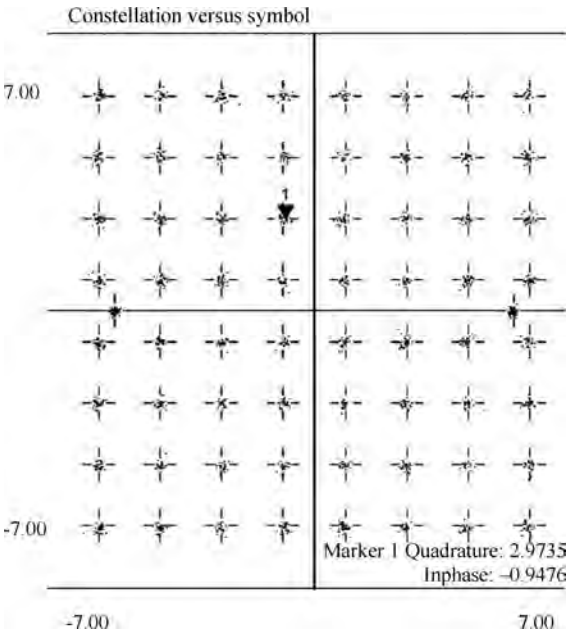


Fig. 6. 64-QAM constellation measurement results at 5.5 GHz.

then used by a digital automatic gain control (AGC) to appropriately set the gain control bits for the LNA and the first stage PGA. The gain of the last three PGA stages is controlled by the companion baseband digital application specific integrated circuit (ASIC). A similar lowpass filter design schematic has been used for the transmitter part.

4. Frequency synthesizer

A delta-sigma based fractional-N frequency synthesizer combined with an RF frequency doubler and an RC polyphase I/Q splitter is used to generate I/Q LO signals to cover the 4.9 to 5.9 GHz frequency range for both the transmitter and the receiver. Figure 4 shows the block diagram of the charge pump based RF frequency synthesizer. A 2nd-order, 3-level output modulator controls the feedback divider. A 3rd-order, 4-bit output modulator is also included on the chip as an alternative. Measurement results indicate that the synthesizer produces large and worst fractional spurs for near-integer dividing ratios, using either modulator. These spurs can be reduced to a small contribution of the total inband spur levels by adding or subtracting a few LSBs from the modulator input. However, the 2nd-order modulator has significant advantage in loop filtering requirements, producing a better inband phase noise performance for a given loop filter. Lower fractional spur levels are also observed using a 3-level output instead of a multi-bit output for the modulator. The synthesizer is designed to have a bandwidth of 250 kHz to meet the 16 μs transmitter (TX) to receiver (RX) switching time requirement in a 10 MHz frequency step, and to minimize the inband phase noise.

5. Voltage control oscillator (VCO) design

Figure 5 shows the VCO schematic. A single cross-coupled PMOS pair is used to provide the negative impedance at half LO frequencies to the on-chip LC tank, which is biased at DC ground[12]. In order to minimize the charge pump and loop filter noise contributions to the synthesizer, the VCO gain should be minimized. This also helps to reduce the reference spur levels. However, for a given supply voltage, the VCO has to have enough gain to cover the required operation frequency range and process variations. A 6-bit controlled switched-capacitor bank is used as part of the LC tank to meet the above requirements. An accumulation mode MOS varactor acts to continuously tune the VCO output frequency between each switched-capacitor LSB binary controlled output frequency step. The output from the VCO then goes to an RF frequency doubler and an internally buffered polyphase I/Q splitter to generate I/Q LO signals from 4.9 to 5.9 GHz.

6. Measurement results

Figure 6 shows the measured transmit output constellation under 64-QAM (quadrature amplitude modulation) mode with the measurement settings listed in Table 1.

Figure 7 gives the EVM measurement result of 52 individual sub-carriers with the measurement settings listed in Table 2. The measurement results show that, at –3 dBm output power, the EVM is better than 33 dB.

Figure 8 shows the measurement result of the synthesizer phase noise performance at 5.44 GHz. The integrated phase

Table 1. Constellation measurement settings.

Parameter	Value
Frequency	5.55 GHz
Single level	–2.9 dBm
External Att	0 dB
Sweep mode	Single
Trigger mode	Power
Trigger offset	–20 μs
Burst type	Direct link burst
Modulation	54 Mbps 64 QAM
No of date symbols	1/1366

Table 2. EVM measurement settings.

Parameter	Value
Frequency	5.55 GHz
Single level	–2.9 dBm
External Att	0 dB
Sweep mode	Single
Trigger mode	Power
Trigger offset	–20 μs
Burst yype	Direct link burst
Modulation	54 Mbps 64 QAM
No of date symbols	1/1366

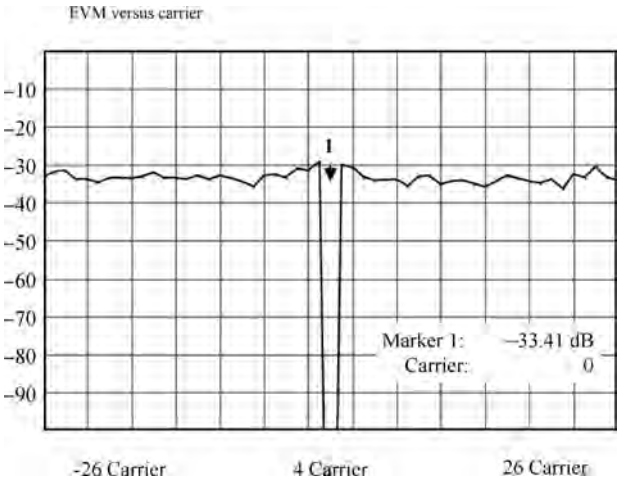
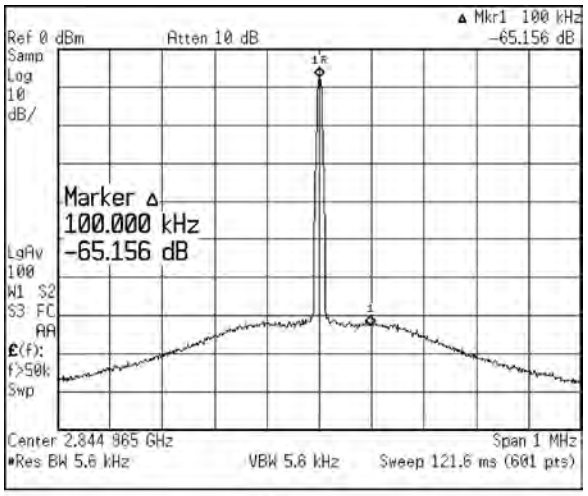


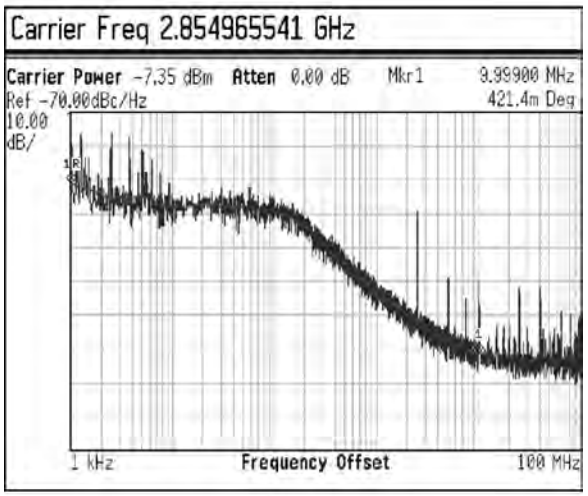
Fig. 7. EVM measurement results of 52 individual sub-carriers.

noise from 1 kHz to 10 MHz is less than 0.5 degrees RMS, exceeding the specification by more than 3 dB. The 40 MHz reference spurs are below –50 dBc.

A single 3.3 V supply is used for the chip to interface directly with the baseband digital ASIC. On-chip individual 1.8 V regulators are used wherever necessary to provide additional supply rejection and isolation of different circuit blocks. The measured receiver noise figure, not including board losses, is better than 5 dB. The chip includes 2 simultaneously active receivers and one transmitter. Total current consumption is 240 mA and 220 mA in TX and RX mode, respectively. A chip die photo is shown in Fig. 9. The total die size is 3.5 mm by 3.6 mm in 0.18 μm CMOS technology. A comparison to other published CMOS RF transceiver designs for WLAN application in the 5 GHz band is list in Table 3.



(a)



(b)

Fig. 8. (a) Synthesizer output spectrum at half LO. (b) PLL close-loop phase noise.

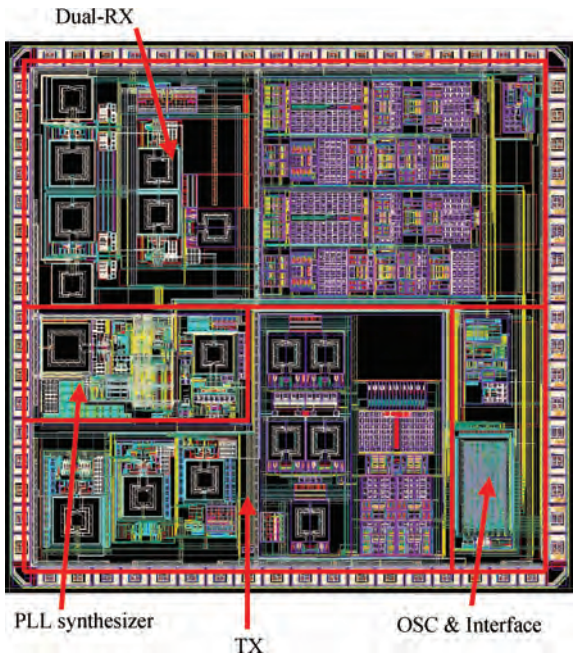


Fig. 9. Chip die photo.

Table 3. Performance comparison.

Reference	Ref. [3]	Ref. [4]	Ref. [5]	Ref. [6]	Ref. [8]	Ref. [9]	This work
Standard	802.11 a/b/g	802.11 a/b/g	802.11 a	802.11 a/b/g	802.11 n	802.11 n	802.11 a
Technology (μm)	0.18	0.25	0.18	0.18	0.13	0.18	0.18
Supply voltage (V)	1.8	2.5	1.8	1.8	1.2	1.8	1.8
Tx EVM	–33 dB @ –5 dBm output power	–30 dB @–5 dBm output power	2.6% @ –10 dBm output power	2.5% @ –7 dBm output power	–31.5 dBc @–4 dBm output power	–40 dB @–5 dBm output power	–33.4 dB @–3 dBm output power
Tx current consumption (mA)	110	—	65	137	—	280	240
Rx current consumption (mA)	140	—	60	118	—	275	220
Rx noise figure (dB)	6.5	5.5	4.4	5.6	6	4.5	6
Die size (mm^2)	17	23	17.2	12	36	18	3.5 × 3.6

7. Conclusion

A low power 5 GHz wireless transceiver in 0.18 μm RF-CMOS technology has been presented in this paper. The RF frequencies cover from 4.9 to 5.9 GHz ISM band with 20 MHz RF channel bandwidth. The measurement results show a 6 dB typical receiver noise figure and better than 33 dB transmitter EVM at –3 dBm output power.

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References

[1] Lee T H, Wong S S. CMOS RF integrated circuits at 5 GHz and beyond. Proc IEEE, 2000, 88(10): 1560

[2] Zhang P, Nguyen T, Razavi B, et al. A 5-GHz direct-conversion CMOS transceiver. IEEE J Solid-State Circuits, 2003, 38(12): 2232

[3] Zhang P, Der L, Razavi B, et al. A single-chip dual-band direct-conversion IEEE 802.1la/b/g WLAN transceiver in 0.18-μm CMOS. IEEE J Solid-State Circuits, 2005, 40(9): 1932

[4] Zargari M, Terrovitis M, Wooley B A, et al. A single-chip dual-band tri-mode CMOS transceiver for IEEE 802.11a/b/g wireless LAN. IEEE J Solid-State Circuits, 2004, 39(12): 2239

[5] Maeda T, Yano H, Hori S, et al. Low-power-consumption direct-conversion CMOS transceiver for multi-standard 5-GHz wireless LAN systems with channel bandwidths of 5–20 MHz. IEEE J Solid-State Circuits, 2006, 41(2): 375

[6] Ahola R, Aktas A, Ismail M, et al. A single-chip CMOS transceiver for 802.11a/b/g wireless LANs. IEEE J Solid-State Circuits, 2004, 39(12): 2250

[7] Rao K R, Wilson J, Ismail M. A CMOS RF front-end for a multistandard WLAN receiver. IEEE Microwave Wireless Compon Lett, 2005, 15(5): 321

[8] Zargari M, Nathawad L Y, Wooley B A, et al. A dual-band CMOS MIMO radio SoC for IEEE 802.1ln wireless LAN. IEEE J Solid-State Circuits, 2008, 43(12): 2882

[9] Carter K A, Chien H M, Wu S, et al. A fully integrated MIMO multiband direct conversion CMOS transceiver for WLAN applications (802.11n). IEEE J Solid-State Circuits, 2007, 42(12): 2795

[10] Wireless LAN MAC and PHY specifications: enhancements for higher throughput. IEEE Draft P802.11n/D.2.00, Feb. 2007

[11] Wi-Fi Alliance Website. [Online]. Available: http://www.wi-fi.org/80211n-draft2.php.

[12] Jerng A, Sodini C G. The impact of device type and sizing on phase noise mechanisms. IEEE J Solid-State Circuits, 2005, 40(2): 360