A digitally controlled power amplifier with neutralization capacitors for Zigbee™ applications

Jia Fei(贾非), Diao Shengxi(刁盛锡)†, Zhang Xuejuan(章雪娟), Fu Zhongqian(傅忠谦), and Lin Fujiang(林福江)

Department of Electronic Science and Technology, University of Science and Technology of China, Hefei 230027, China

Abstract: This paper presents a single chip CMOS power amplifier with neutralization capacitors for Zigbee™ system according to IEEE 802.15.4. A novel structure with digital interface is adopted, which allows the output power of a PA to be controlled by baseband signal directly, so there is no need for DAC. The neutralization capacitors will increase reverse isolation. The chip is implemented in SMIC 0.18 μm CMOS technology. Measurement shows that the proposed power amplifier has a 13.5 dB power gain, 3.48 dBm output power and 35.1% PAE at P_{1dB} point. The core area is 0.73×0.55 mm^2.

Key words: power amplifier; Zigbee™; CMOS; digital control; neutralization

DOI: 10.1088/1674-4926/33/12/125002 **EEACC:** 1205; 1220

1. Introduction

The IEEE 802.15.4 standard defines the physical layer for wireless short-range devices[1], one of whose important applications is Zigbee™. Cost and area considerations are driving implementations towards single-chip solutions with external components as little as possible, so a PA without an off-chip component is needed. To prolong battery life, a low power consumption system is critical. A high efficiency PA is the key to constructing a low power consumption system as a PA is power hungry. In practice, the distance between two wireless devices is uncertain, so to reduce the power consumption and relieve the difficulty of the receiver, dynamic output power is necessary. If baseband signal can be used to control the output power directly, DAC will be eliminated, so the power consumption and area of the transmitter will be reduced. Besides, it can provide a better support to the EER transmitter for QAM modulation[2]. Based on all this, we focus on an integrated PA design with high efficiency and digital interface.

In this paper, a two-stage differential class-AB CMOS PA for Zigbee™ application is presented. To increase the reverse isolation and stability, neutralization capacitors are employed. Without any off-chip components, output matching fully implemented on chip is analyzed in detail. To gain higher efficiency and maintain relatively good linearity, the PA uses push-pull topology and FETs work in deep class-AB mode.

In Section 2, the neutralization capacitors technique employed is described. Section 3 shows pros and cons of some proposed CMOS PAs. In Section 4, a fully integrated linear CMOS PA with digital interface in 0.18 μm CMOS process is presented. In Section 5, the measurement result is discussed, which proves that the proposed PA achieves good power efficiency and precise gain controllability.

2. Basic neutralization principle

As shown in Fig. 1, parasitic capacitance C_{gd} between input signal and output signal provides a feedback path to reduce the amplifier's gain (i.e., the Miller effect) and results in poor isolation between input and output. The gain of the PA in Fig. 1 can be expressed as:

$$A_{V1} = \frac{g_m - j\omega C_{gd}}{j\omega(C_L + C_{gd}) + 1/j\omega L + 1/R}, \quad (1)$$

where g_m is the equivalent transconductance of NMOS transistor M1 and M2, and C_{gd} is the parasitic capacitance of M1 and M2. There are two zeros and two poles in Eq. (1), and one zero g_m/C_{gd}, which located in the right half plane, will degrade the isolation and stability.

A cascode topology will increase the isolation but will reduce the headroom and efficiency. Moreover, in most situations, the common-gate FETs work in the linear region for a PA, where these FETs are equivalent to a small resistance, so the isolation increment is limited.

Providing compensation current to cancel this unwanted feedback is called neutralization[3] as shown in Fig. 2. Neutralization is easily realized in a differential amplifier with two

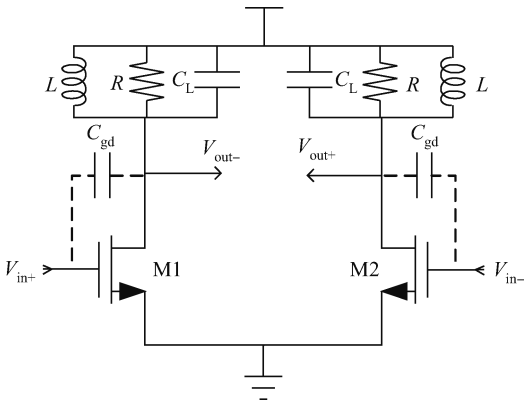


Fig. 1. Basic topology of pseudo differential PA.

† Corresponding author. Email: diaosxi@ustc.edu.cn
Received 7 April 2012, revised manuscript received 2 July 2012

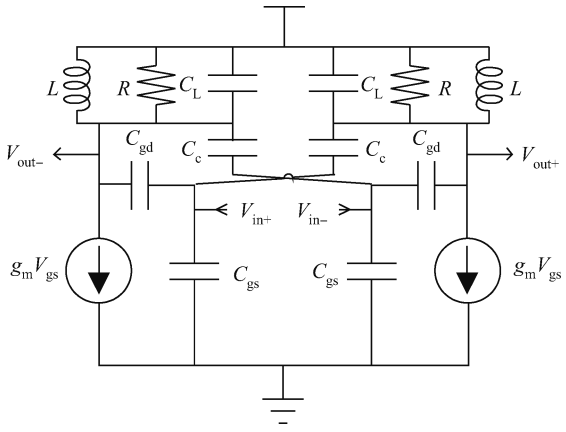


Fig. 2. Small signal equivalent circuit of a pseudo-differential pair with neutralization.

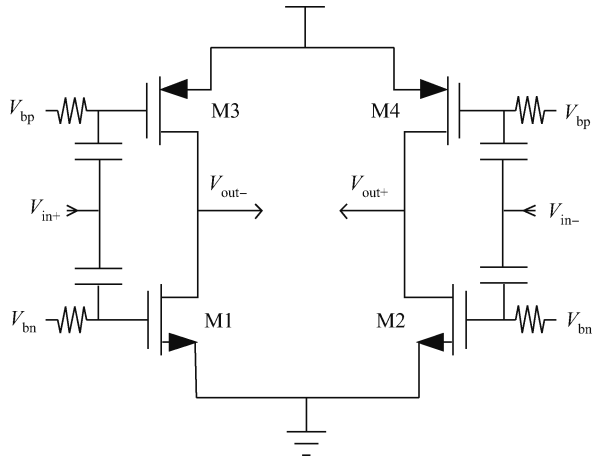


Fig. 3. PA schematic, simplified.

additional capacitors C_c cross-connected between the gate and the drain terminals. The voltage gain of the circuit in Fig. 2 is

$$A_{V2} = \frac{g_m - j\omega(C_{gd} - C_c)}{j\omega(C_L + C_{gd} + C_c) + 1/j\omega L + 1/R}, \quad (2)$$

where C_c is the neutralization capacitor. From Eq. (2), we can eliminate the zero in right half plane by setting C_c equal to C_{gd}. So, neutralization will increase the reverse isolation and the stability.

3. Topology analysis of PA

The maximal output power P_{out} of the PA is determined by the load impedance R_{opt}, the supply voltage V_{dc} and the knee voltage V_{knee} as follows.

$$P_{out} = \frac{(V_{dc} - V_{knee})^2}{2R_{opt}}. \quad (3)$$

So the optimal load resistance R_{opt} is

$$R_{opt} = \frac{(V_{dc} - V_{knee})^2}{2P_{out}}. \quad (4)$$

The supply voltage of the PA is limited by the process to be 1.8 V. If the value of V_{knee} is normalized to the DC supply voltage, a value of 0.1 will represent a realistic value for many practical cases[4], so we choose 0.15 V here as the value of V_{knee} for 0.18 μm CMOS process. The maximum output power is about 3 dBm to fit the requirement of the Zigbee™ system.

If the differential structure is adopted as shown in Fig. 1, the differential R_{opt} is about 2520 Ω. So, the impedance transformation ratio is very high (from 100 to 2520 Ω), which means a narrow bandwidth and high loss.

Wolfram Kluge proposed a solution[5] to solve this problem, as shown in Fig. 3. This topology can reduce the output swing of one path from $2V_{DD}$ to V_{DD} (ignoring the V_{knee}). The limited output swing reduces the impedance transformation ratio to one fourth of the original (the optimal output impedance is 630 Ω and the impedance transformation ratio is about 6), so this structure improves the bandwidth and reduces the loss.

The circuit in Ref. [5] adopts a pseudo differential push-pull topology and input FETs are biased in deep class AB mode

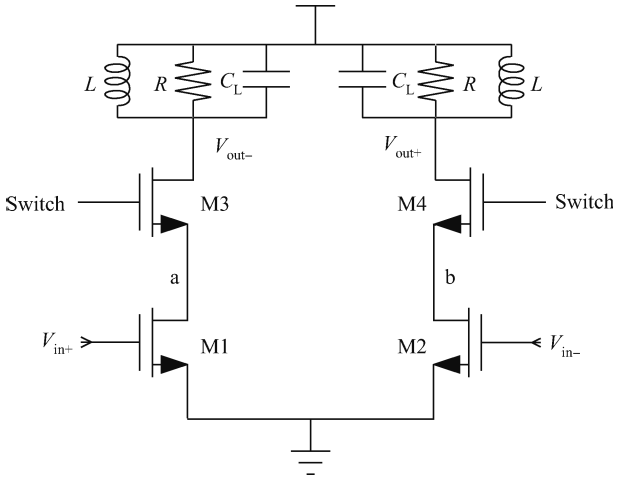


Fig. 4. Basic topology of pseudo differential PA.

(to avoid cross distortion) independently. This structure is good for achieving a low output power PA as it has a drain efficiency like class B when keeping the linearity close to class A. The ideal efficiency of class AB is

$$\eta_{max} = \frac{\alpha - \sin\alpha}{2[2\sin(\alpha/2) - \alpha\cos(\alpha/2)]}, \quad (5)$$

where the α is the conduction angle. As α changes from π to 2π, the efficiency changes from 50% to 78.5%.

But in this structure, PMOS will contribute bigger parasitic capacitance C_{gd} compared to NMOS. So the reverse isolation is unacceptable and the stability needs be carefully designed. One traditional solution is using a cascode topology[6] in Fig. 4. However as mentioned in Section 2 this solution will decrease efficiency and the enhancement to isolation is not significant. Besides, the linearity of the cascode structure is poor, not just because it will reduce the headroom but also because the common gate transistors' on-resistance will keep changing.

Generally, common-gate transistors work as switches. When the switch is on, the voltage on the gate is VDD. The voltage at points a and b follows the input signals V_{in+} and V_{in-} with opposite phases. As the large input swing will lead to large variation of V_{gs} of M3 and M4, equivalent on-resistance

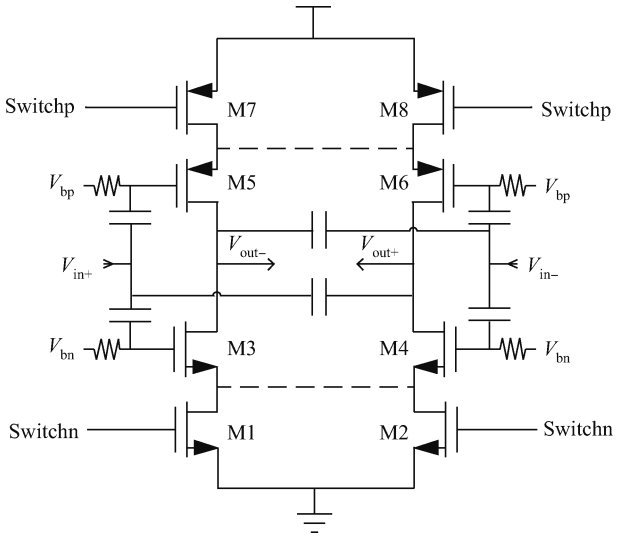


Fig. 5. PA with neutralization capacitor and switches.

will change dramatically in a period. As a result, the linearity will deteriorate.

4. Proposed PA

4.1. Circuit design of digitally controlled PA

To solve problems mentioned above, a novel structure is proposed. Compared to Ref. [5], we adopt neutralization capacitors and use a common-source transistor as switches. Our proposed structure is shown in Fig. 5. Corresponding NMOS and PMOS switches are on or open at the same time. M1, M2 are NMOS switches and M7, M8 are PMOS switches, and the control signal Switchn and Switchp have opposite phases. In traditional cascode topology, the common-gate FETs show a low resistance when they are on, but a high resistance when they are open. If we adopt neutralization in cascode structure, we face a problem that the equivalent impedance between input nodes and output nodes will be totally different when the switches are in different states. So the neutralization capacitor must be adaptive, which is difficult to achieve. For the circuit shown in Fig. 5, no matter whether the switches are on or not, the capacitance between input nodes and output nodes is almost the same, so this topology is compatible with neutralization. However if we just adopt a common-source transistor as switches, then the circuit is the same as a source negative feedback circuit, which will degrade the equivalent transconductance g_m, so is the gain of the PA. One simple solution is to connect the drain of M1, M2 together, and the drain of M7, M8 together, shown as a dotted line, then we get a virtual ground at the source of M3, M4 and the source of M5, M6. So, this topology has better gain and efficiency.

4.2. Matching network

A differential tapped capacitor resonator matching network is shown in Fig. 6. Compared to L matching network, this topology is more robust, because the transformation ratio is roughly determined by the ratio of the capacitor, as shown below. Compared to π matching network, DC block capacitor is not needed, which means less loss and smaller area.

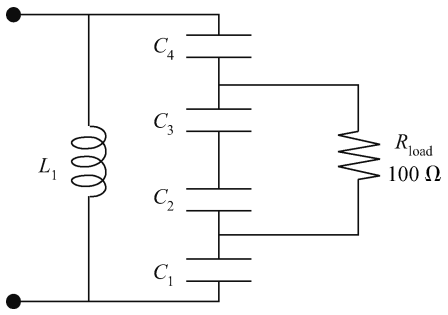


Fig. 6. Differential tapped capacitor resonator matching network.

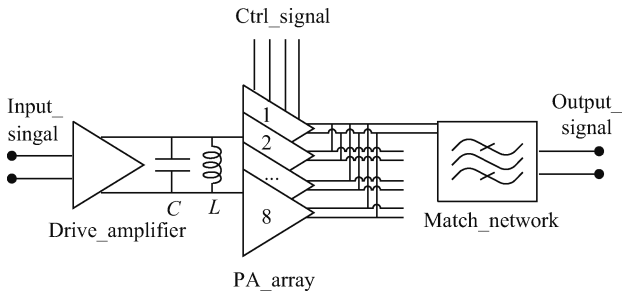


Fig. 7. Schematic of the proposed PA (biasing not shown).

The admittance of the circuit shown in Fig. 6 is[7]

$$Y_{in} = \frac{j\omega C_1 - \omega^2 R_{load} C_1 C_2}{j\omega R_{load}(C_1 + C_2) + 1}, \tag{6}$$

where C_1 is equal to C_4, and C_2 is equal to C_3. To show the symmetry of the differential topology and simplify the calculation, C_2 and C_3 are separated. But in fact, one smaller capacitor can be used to save the area. The real part of Eq. (6) is

$$G_{in} = \frac{\omega^2 R_{load} C_1^2}{\omega^2 R_{load}^2 (C_1 + C_2)^2 + 1}. \tag{7}$$

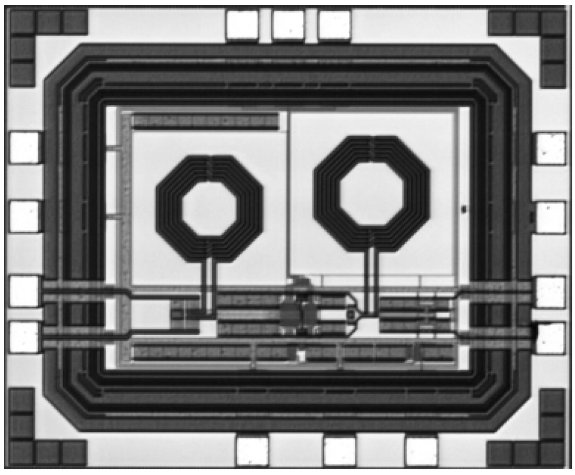
At high frequencies or when the capacitor is large enough ($\omega^2 R_{load}^2 (C_1 + C_2)^2 \gg 1$), the equivalent shunt conductance simplifies to

$$G_{in} \approx \frac{\omega^2 R_{load} C_1^2}{\omega^2 R_{load}^2 (C_1 + C_2)^2} = G_{load} \left[\frac{C_1}{C_1 + C_2}\right]^2. \tag{8}$$

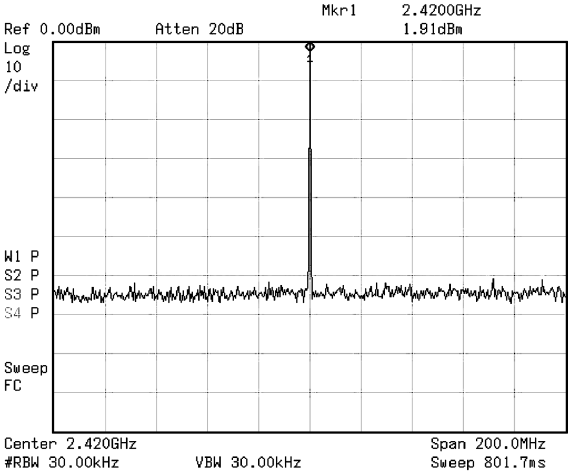
The imaginary part of the admittance at high frequencies:

$$B_{in} = \omega \frac{C_1 C_2}{C_1 + C_2}. \tag{9}$$

We can get the ratio of $[(C_1/(C_1 + C_2)]^2$ equal to one over transformation ratio from Eq. (8) . For a given frequency, if the inductor is fixed, we can get B_{in}, as the admittance of the inductor equal to negative B_{in} in ω_0. Then through Eq. (9) we can get the proper capacitance of C_1 and C_2. The choice of inductor is a trade-off between loss, Q, and area, which needs careful consideration.

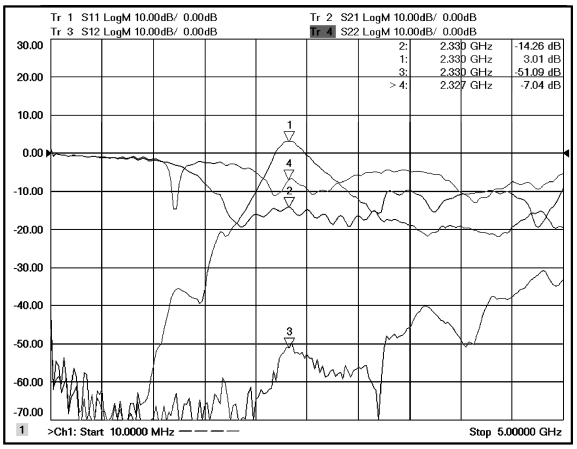


(a)

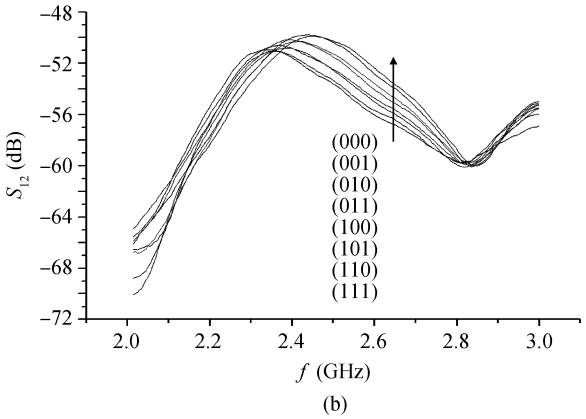


(b)

Fig. 8. (a) Chip photograph. (b) The output spectrum without de-embedding.



(a)



(b)

Fig. 9. (a) Measured S-parameter of the PA in the highest gain mode (111). (b) Measured S_{12} in different modes.

4.3. Two-stage PA

Figure 7 shows the complete proposed two-stage PA diagram for Zigbee™ transmitter. The modulated signal from VCO is not able to drive the major power amplifier array directly, so a driver amplifier is needed to amplify the signal first. The schematic of the driver amplifier is similar to the circuit as shown in Fig. 5, but without the neutralization capacitor, because the feedback of the driver amplifier is so small that it can be ignored here. To achieve a digital baseband directly controlled PA, we construct a PA array with 3 bits accuracy and each sub-PA like the one in Fig. 5. We adopt thermometer-coded strategy to control the output current which is equivalent to controlling the output power. We construct a PA array with eight identical sub-PAs, so we get 8 steps of output power. The schematic of the matching network is shown in Fig. 6. The output power is transmitted towards balun or differential antenna.

5. Measurement result

The PA is implemented in SMIC 0.18 μm process. Figure 8(a) shows the chip photograph. The core area occupies 0.73 × 0.55 mm^2. RF interconnect asymmetry could cause phase jumps when altering the amplitude control words (ACW), so to keep the integrity of the signal, the signal should reach the sub-PA synchronously. In this chip, as the size of FETs is quite small, the distribution effect is limited and the FETs are redrawn, instead of RF FETs supplied by foundry, for reducing the area of layout and optimizing the connection. So the distribution effect will be alleviated to a great extent, as a result of less parasites of interconnection.

Figure 8(b) shows the output power without de-embedding, which is 1.91 dBm (the power is de-embedded in the following content). The main contribution of loss is from balun and coaxial cable, in total 1.58 dB, both in the input and output port. From 2.4 to 2.485 GHz, the minimum of output power is larger than 1.6 dBm after de-embedding.

S-parameters are measured by an Agilent E8364C PNA from 10 MHz to 5 GHz, as shown in Fig. 9(a). Good input matching is achieved in broadband, which is below –14 dB from 2 to 3 GHz. S_{21} reaches a peak value of 3 dB at 2.33 GHz, which is below the desired frequency 2.45 GHz due to inaccurate parasitic extraction and process variation. S_{21} needs to be de-embedded, because a 100 Ω resistor is put between differential input ports, which is used to simplify the input matching and will not be integrated into the practical transceivers. The input impedance ZM1 without the resistor is 1.12 kΩ, which means the input power should be smaller by 10.5 dB and considering the loss caused by balun and cables, the small signal gain should be 16.5 dB. S_{21} reflects the behavior of a small sig-

Table 1. Summary and performance comparison.

Parameter			Ref. [5]	Ref. [8]	Ref. [9]	Ref. [10]	Ref. [11]	Ref. [12]	This work
Technology (μm)			0.18	0.18	0.18	0.18	0.18	0.18	0.18
Supply voltage (V)			1.8	1.8	1.8	3.3	2.5	1.8	1.8
Frequency band (GHz)			2.4–2.485	2.4–2.485	2.4–2.485	2.4	2.45	0.9	2.4–2.485
Power gain (dB)			N/A	N/A	N/A	19	17.5	23.3	13.5
Output power (dBm) @ P_{1dB}			3	0	3	20.2	20.5	18.4	3.5
PAE (%)	@ P_{1dB}		30	33	21	30.2	37	29.2	35.1
	@ Back off	4 dB	N/A	N/A	N/A	21	21	20	21
		8 dB	N/A	N/A	N/A	12	12	12	9
Matching network			On-chip	Off-chip	Off-chip	On-chip	On-chip	Off-chip	On-chip
Core size (mm^2)			0.2*	0.5*	0.2*	1.53	1.34	0.66	0.4

* Estimated from the paper.

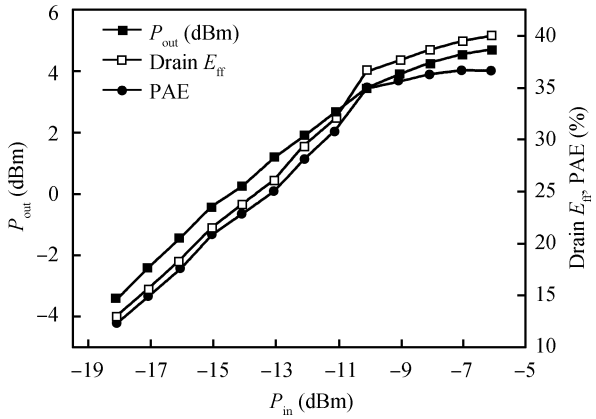


Fig. 10. Output power, drain efficiency and PAE change with input power.

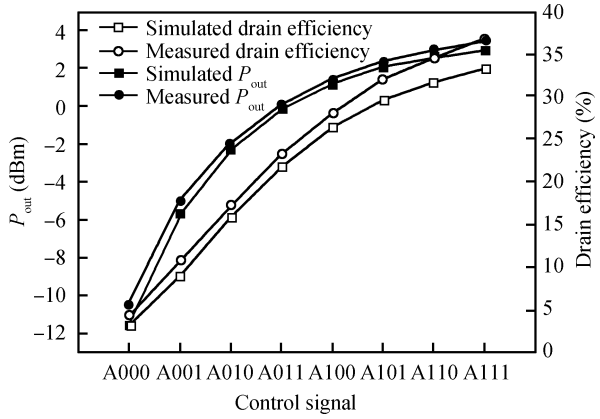


Fig. 11. Output power and drain efficiency change with amplitude control words.

nal rather than a large signal. S_{12} is below –49 dB in the desired band, which is 11 dB better than Ref. [12]. S_{22} is –7 dB, which is acceptable, because the power matching is more important than conjugate matching for PA design[4].

As mentioned in Section 4, the proposed circuit can increase the reverse isolation of the PA in different modes, which is show in Fig. 9(b). Even in the worst case of the eight modes, the S_{12} is better than –49 dB from 2 to 3 GHz. A point worth noting is that, in simulation, the reverse isolation (S_{12}) is about –79 dB, but the measured reverse isolation is about –49 dB (worst case), which is worse than simulation but still good enough to prove neutralization effective. The deterioration of reverse isolation may be as a result of PCB coupling, or the mismatch of the neutralization capacitor. In the simulated condition the neutralization could cancel the C_{gd} perfectly, supposing the mismatch between the neutralization capacitor and C_{gd} is 0.2%. But in reality, as the process varies, the capacitance of the capacitor may change 5% or even more, which means the S_{12} will deteriorate more than 28 dB.

An Agilent N9310 and N9030A PXA are used for power measurement. Figure 10 shows the output power, drain efficiency and PAE as input power is increasing. During measurement, we fixed the power of input signal and swept the frequency, then we found the maximal power is achieved at 2.42 GHz. The input P_{1dB} is –10 dBm, the output power is 3.48 dBm and power gain is 13.5 dB at 1 dB compression point. As the power gain is more than 20, the input power is negligible compared to the output power, so the trace of drain efficiency and PAE is close.

Figure 11 shows the variation of output power and drain efficiency with the amplitude control words (ACW). The input signal is constant as we modulate ACW, instead of altering the input power, to control the output power of the PA directly. The relationship between ACW and output power is

$$P_{\text{out}} = 10\lg P_0 + 20\lg(\text{ACW} + 1), \tag{10}$$

where the P_0 is the output power of one sub-PA. When the ACW are 000, there is only one sub-PA working, and when the ACW are 001, there are two sub-PAs working, so the output power could increase 6 dB, as a result of doubling the current. When the ACW is 010, there are three sub-PAs working, so the output power continues to increase 3.5 dB (20lg(3/2)), and so on. But as mentioned in Ref. [13], the output resistance R_0 of sub-PA will affect the relationship between ACW and output power, so Equation (10) needs be modified to

$$P_{\text{out}} = 10\lg P_0 + 20\lg\left[(\text{ACW}+1)\frac{R_0 + R_{\text{L}}}{(\text{ACW}+1)R_0 + R_{\text{L}}}\right], \tag{11}$$

where R_{L} is the load resistance seen by the PA. Besides, the gain will be compressed as the output power increases, so the increment of output power by ACW will be lower than the theoretical estimation in Eq. (11). As shown in Fig. 11, the difference of simulated output power and measured output power is less than 1dB, which means acceptable priori control accuracy.

If we continue increasing the number of bits, we can further improve the control accuracy. The dynamic range is 14 dB from –10.52 to 3.48 dBm.

In a Zigbee^{TM} transceiver, the output power is fixed during transmission but the PA should support static adjustment of output power for different applications. Here, we show that this circuit has the capability to tune the output power by digital interface, but the dB-linear capability is not achieved as it is not necessary for the Zigbee^{TM} transceiver. However, to support non-constant envelop modulation like QAM, the dB-linear capability is indispensable, so adaptive digital predistortion (DPD) is a reasonable solution[13]. By using the actual measured AM distortion, a look-up table (LUT)-based DPD system could be implemented in a DSP simulation environment to support adaptive DPD, but the ACW should be as high as 10 bits[13]. To simplify the layout of the proposed structure, 3 bits level control is adopted in this chip, which is not enough to support the linearization of a digitally controlled PA, but if more bits are adopted, the linearization is totally feasible. A dB-linear PA is achieved in the next version.

We can find that the measured result is a little better than simulation, but it is within the process variation range.

Table 1 shows the comparison between this work and other reported works. This work has a better power efficiency at P_{1dB} than others. In Ref. [10], dual modes strategy is used, and in Refs. [11, 12], the output power is controlled by altering the input power. In this work, the adoption of digital interface will reduce the quiescent bias current at back off, thus will increase the drain efficiency, but the input power is constant independent from back off, so the PAE will deteriorate at very low output power. Considering that the proposed PA supplies other benefits like totally implemented on chip and digital interface, this topology is beneficial and effective.

6. Conclusion

In this paper, a digitally controlled power amplifier design has been proposed. The matching network is realized on chip, so no off-chip component is needed. The PA is verified with SMIC 0.18 μm 1P6M CMOS process. The two-stage PA delivers 3 dBm power with 35.1% PAE at the P_{1dB} point and has 13.5 dB gain. Measurements show that the two-stage PA has good reverse isolation better than –49 dB and the output power can be controlled by digital baseband properly and directly. This work gives a feasible integrated PA solution for SOC system and has the potential to support high order modulation.

References

[1] IEEE 802.15.4 Standard, Draft P802.15.4b/D3, Oct. 2005
[2] Kavousian A, Su D K, Hekmat M, et al. A digitally modulated polar CMOS power amplifier with a 20-MHz channel bandwidth. IEEE J Solid-State Circuits, 2008, 43(10): 2251
[3] Grebene A B. Bipolar and MOS analog integrated circuit design. New York: Wiley, 1984, Chapter 8
[4] Cripps S C. RF power amplifiers for wireless communications. 2nd ed. Norwood: Artech, 2006, Chapter 8
[5] Kluge W, Poegel F, Roller H, et al. A fully integrated 2.4-GHz IEEE 802.15.4 compliant transceiver for ZigBee^{TM} applications. IEEE J Solid-State Circuits, 2006, 41(12): 2767
[6] Chee Y H, Rabaey J, Niknejad A M. A class A/B low power amplifier for wireless sensor networks. Proceedings of the International Symposium on Circuits and Systems, 2004: 409
[7] Lee T H. The design of CMOS radio-frequency integrated circuits. 2nd ed. Cambridge: Cambridge University Press, 2004, Chapter 3
[8] Choi P, Park H C, Kim S, et al. An experimental coin-sized radio for extremely low-power WPAN (IEEE 802.15.4) application at 2.4 GHz. IEEE J Solid-State Circuits, 2003, 38(12): 2258
[9] Kim Y J, Hwang I C, Baek D. A switchless zigbee frontend transceiver with matching component sharing of LNA and PA. IEEE Microw Wireless Compon Lett, 2010, 20(9): 516
[10] Oh H S, Kim C S, Yu H K, et al. A fully-integrated +23-dBm CMOS triple cascode linear power amplifier with inner-parallel power control scheme. Radio Frequency Integrated Circuits (RFIC) Symposium, 2006
[11] Kang J, Yoon J, Min K, et al. A highly linear and efficient differential CMOS power amplifier with harmonic control. IEEE J Solid-State Circuits, 2006, 41(6): 1314
[12] Han Kefeng, Cao Shengguo, Tan Xi, et al. A 900 MHz, 21 dBm CMOS linear power amplifier with 35% PAE for RFID readers. Journal of Semiconductors, 2010, 31(12): 125005
[13] Presti C D, Carrara F, Scuderi A, et al. A 25 dBm digitally modulated CMOS power amplifier for WCDMA/EDGE/OFDM with adaptive digital predistortion and efficient power control. IEEE J Solid-State Circuits, 2009, 44(7): 1883