Switched-capacitor multiply-by-two amplifier with reduced capacitor mismatches sensitivity and full swing sample signal common-mode voltage*

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Abstract: A switched-capacitor amplifier with an accurate gain of two that is insensitive to component mismatch is proposed. This structure is based on associating two sets of two capacitors in cross series during the amplification phase. This circuit permits the common-mode voltage of the sample signal to reach full swing. Using the charge-complement technique, the proposed amplifier can reduce the impact of parasitic capacitors on the gain accuracy effectively. Simulation results show that as sample signal common-mode voltage changes, the difference between the minimum and maximum gain error is less than 0.03%. When the capacitor mismatch is increased from 0 to 0.2%, the gain error is deteriorated by 0.00015%. In all simulations, the gain of amplifier is 69 dB.

Key words: multiply-by-two amplifier; mismatch-insensitive amplifier; full swing; switched-capacitor circuits
DOI: 10.1088/1674-4926/33/11/115003 **EEACC:** 2570

1. Introduction

Switched-capacitor multiply-by-two (MBT) amplifiers are widely used in some high-resolution analog-to-digital converters (ADCs), such as pipeline or cyclic ADCs. Since the accuracy of gain blocks seriously affects the linearity of ADCs, self-calibration[1, 2] or capacitor error-averaging techniques[3, 4] were proposed to improve the linearity of ADCs. But these solutions usually increase the circuit complexity or take multiple cycles to enhance the accuracy of amplification.

In recent years, many resolutions were proposed to enhance the accuracy of MBT blocks, so that a high-resolution ADC can be achieved with a simpler structure. In recent resolutions[5, 6], a valid output is generated within two clock cycles. In another resolution[7], two operational amplifiers (OPAs) are necessary to obtain the gain of two. In resolution [8], the gain is based on the value of resisters. In this brief, one OPA is used to achieve the gain of two in only one cycle. Compared with solution [9], the proposed solution uses fewer capacitors and permits the common-mode voltage of the sample signal to reach full swing. Another resolution insensitive to component mismatches is presented in Ref. [10]. Four clock phases are needed in this circuit. In the proposed circuit, only one clock cycle is needed.

This paper first reviews the conventional MBT amplifier circuit, and analyzes the sensitivity to capacitor mismatches. Then this paper presents a proposed MBT amplifier circuit, and analyzes the effects of nonidealities.

2. Conventional MBT amplifier circuit

The conventional MBT amplifier circuit is shown in Fig. 1. In the first phase, switches Φ1 are closed and all capacitors sample the differential input signal. In the second phase, switches Φ2 are closed and the bottom plate of C_{ax} is connected to the output terminal. So the charge stored in C_{bx} will move to C_{ax}. Assuming that capacitor mismatch exists, the capacitor can be expressed as $C_{a1} = C(1+\varepsilon_{a1})$, where ε is the mismatch factor. Then the differential gain of the circuit is

$$V_{op} - V_{on} = \frac{1}{2}\left(V_{ip} - V_{in}\right)\left(\frac{2+\varepsilon_{a1}+\varepsilon_{b1}}{1+\varepsilon_{a1}} + \frac{2+\varepsilon_{a2}+\varepsilon_{b2}}{1+\varepsilon_{a2}}\right). \tag{1}$$

The conventional MBT amplifier circuit is realized in a 0.18 μm CMOS technology. The gain is simulated with ε ranging from 0 to 2%, and the result is shown in Fig. 2. A folded cascade OPA with gain of 69 dB is used in these simulations.

3. Proposed MBT amplifier circuit

3.1. Basic circuit

The basic proposed MBT amplifier circuit is shown in Fig. 3(a). C_{fx} and C_{bx} are sample capacitors. The left parasitic capacitor of C_{bx} is C_{lx}, and the right one is C_{rx}. In order to

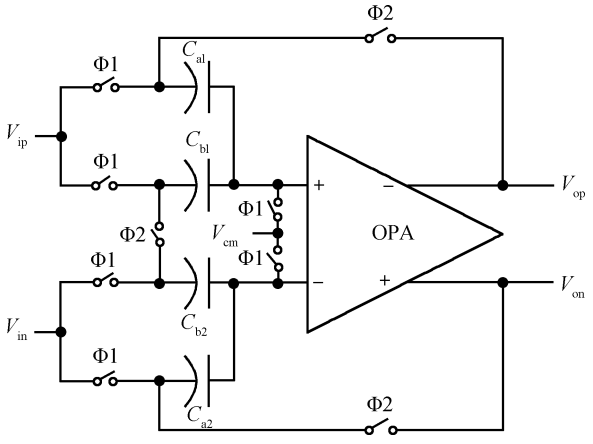

Fig. 1. Conventional MBT amplifier circuit.

* Project supported by the National Natural Science Foundation of China (Nos. 61036004, 61076024).
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Received 10 April 2012, revised manuscript received 31 May 2012

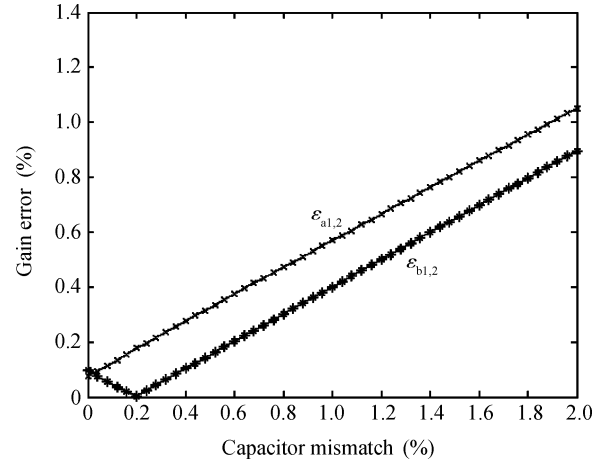

Fig. 2. Gain error versus capacitor mismatch of conventional circuit.

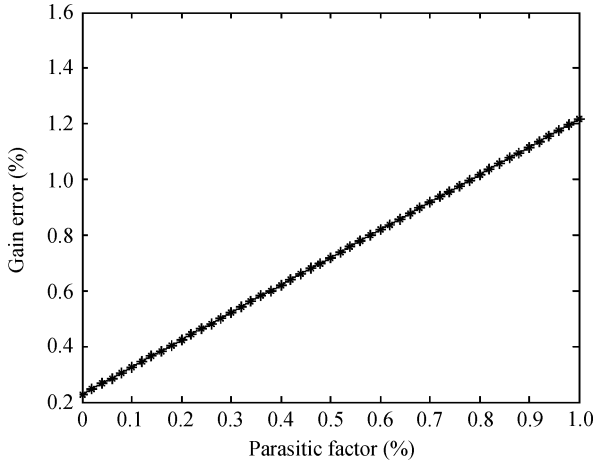

Fig. 4. Gain error versus parasitic factor of the basic proposed circuit.

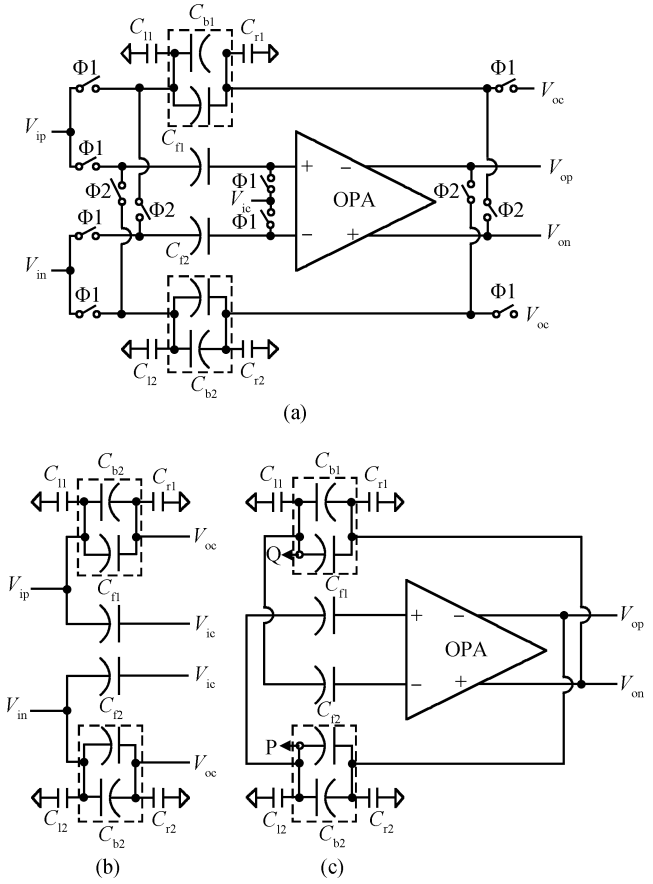

Fig. 3. (a) Proposed MBT amplifier circuit. (b) Configuration in phase $\Phi 1$. (c) Configuration in phase $\Phi 2$.

make the difference between C_{lx} and C_{rx} smaller, C_{bx} could be made up with two identical capacitors connected reversely in parallel.

Ignoring the parasitic capacitor, during phase $\Phi 1$ shown in Fig. 3(b), the voltage sampled by C_{f1}, C_{b1}, C_{f2}, and C_{b2} are V_{ip}–V_{ic}, V_{ip}–V_{oc}, V_{in}–V_{ic}, and V_{in}–V_{oc}. As shown in Fig. 3(c), during phase $\Phi 2$, the common mode voltage of the OPA output is V_{oc} and the differential output voltage $V_{od} = V_{op} - V_{on} = (V_{oc} - V_{in}) + (V_{ip} - V_{ic}) + (V_{ic} - V_{in}) + (V_{ip} - V_{oc}) = 2(V_{ip} - V_{in}) = 2V_{id}$. Because the common mode voltage of the OPA output is V_{oc}, the common mode voltage of the OPA input is still V_{ic}. The input voltage of OPA does not change in the process and it has nothing to do with the sample signal, so the sample signal can reach full swing.

3.2. Parasitic and mismatch influence on basic circuit

Considering the effects of nonidealities, capacitor mismatch is ε such as $C_{b1} = C(1 + \varepsilon_{b1})$ and parasitic factor is α such as $C_{l1} = \alpha C$. In phase $\Phi 1$, capacitors C_{fx} and C_{bx} sample the differential input signal $V_{id} = V_{ip} - V_{in}$. In phase $\Phi 2$, the charge equations at nodes P, and Q are defined as
node P:

$$-\frac{1}{2}V_{id}(C_{b2} + C_{l2}) = \left(\frac{1}{2}V_{id} - V_{op}\right)C_{b2} + \frac{1}{2}V_{id}C_{l2}, \quad (2)$$

node Q:

$$\frac{1}{2}V_{id}(C_{b1} + C_{l1}) = \left(-\frac{1}{2}V_{id} - V_{on}\right)C_{b1} - \frac{1}{2}V_{id}C_{l1}. \quad (3)$$

The differential output signal is defined as $V_{od} = V_{op} - V_{on}$. Assuming capacitors C_{b1} and C_{b2} are equal, the output of the amplification phase result from Eqs. (2) and (3) is

$$V_{od} = 2V_{id}\left(1 + \frac{C_{l1} + C_{l2}}{C_{b1} + C_{b2}}\right). \quad (4)$$

Because $C_{lx} = \alpha C_{bx}$, the gain error is nearly equal to parasitic factor α. Simulation results are shown in Fig. 4.

3.3. Complete version of the proposed MBT amplifier circuit

In order to reduce the gain error, the charge-complement structure shown in Fig. 5 is introduced. As shown in Fig. 6, there are three circuit phases. In the sample phase, only switches $\Phi 1$ are closed. In the charge-complement phase, only switches $\Phi 2$ are closed. In the amplification phase, only switches $\Phi 3$ are closed.

The sample phase is the same as phase $\Phi 1$ in the basic circuit. In the charge-complement phase, the charge equations

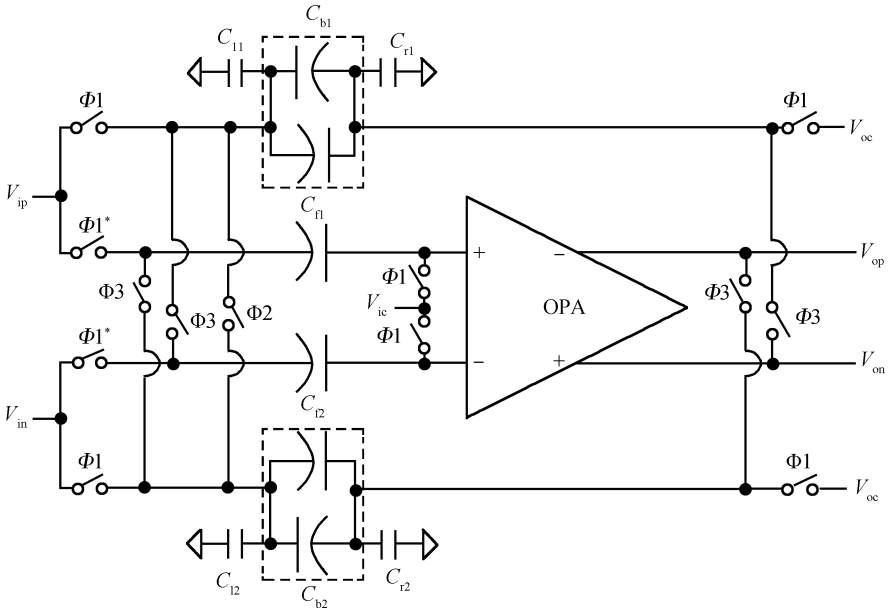

Fig. 5. Complete version of the proposed MBT amplifier circuit.

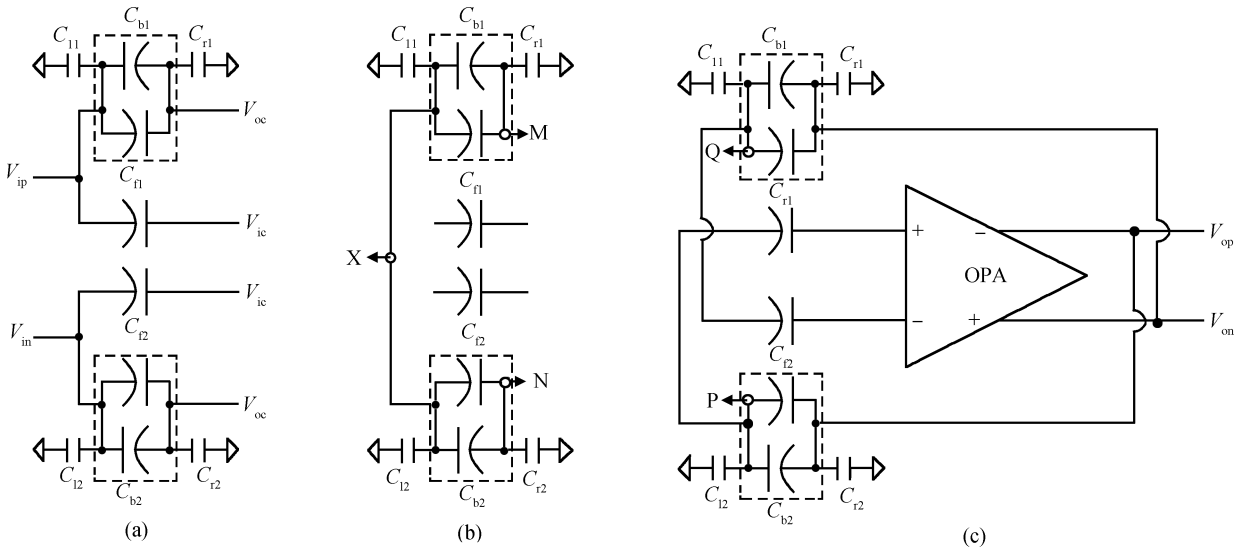

Fig. 6. (a) Sample phase. (b) Charge-complement phase. (c) Amplification phase.

at nodes M, N, and X are defined as
node M:

$$-\frac{1}{2}V_{\mathrm{id}}C_{\mathrm{b1}} = V_{\mathrm{M}}C_{\mathrm{r1}} + V_{\mathrm{M}}C_{\mathrm{b1}}, \tag{5}$$

node N:

$$\frac{1}{2}V_{\mathrm{id}}C_{\mathrm{b2}} = V_{\mathrm{N}}C_{\mathrm{r2}} + V_{\mathrm{N}}C_{\mathrm{b2}} \tag{6}$$

The voltage of node X is 0. In the amplification phase, the charge equations at nodes P, and Q are defined as
node P:

$$-V_{\mathrm{N}}C_{\mathrm{b2}} = \frac{1}{2}V_{\mathrm{id}}C_{\mathrm{l2}} + \left(\frac{1}{2}V_{\mathrm{id}} - V_{\mathrm{op}}\right)C_{\mathrm{b2}}, \tag{7}$$

node Q:

$$-V_{\mathrm{M}}C_{\mathrm{b1}} = -\frac{1}{2}V_{\mathrm{id}}C_{\mathrm{l1}} + \left(-\frac{1}{2}V_{\mathrm{id}} - V_{\mathrm{on}}\right)C_{\mathrm{b1}}. \tag{8}$$

According to Eqs. (7) and (8), the output of the amplification phase is

$$V_{\mathrm{od}} = \frac{1}{2}V_{\mathrm{id}}\left(4 + \frac{C_{\mathrm{l1}}}{C_{\mathrm{b1}}} - \frac{C_{\mathrm{r1}}}{C_{\mathrm{b1}} + C_{\mathrm{r1}}} + \frac{C_{\mathrm{l2}}}{C_{\mathrm{b2}}} - \frac{C_{\mathrm{r2}}}{C_{\mathrm{b2}} + C_{\mathrm{r2}}}\right). \tag{9}$$

If we use ε and α to express all capacitors, Equation (9) can be expressed as

$$V_{\mathrm{od}} = \frac{1}{2}V_{\mathrm{id}}\left(4 + \frac{\alpha_{\mathrm{l1}}}{1+\varepsilon_{\mathrm{b1}}} - \frac{\alpha_{\mathrm{r1}}}{1+\varepsilon_{\mathrm{b1}}+\alpha_{\mathrm{r1}}} + \frac{\alpha_{\mathrm{l2}}}{1+\varepsilon_{\mathrm{b2}}} - \frac{\alpha_{\mathrm{r2}}}{1+\varepsilon_{\mathrm{b2}}+\alpha_{\mathrm{r2}}}\right). \tag{10}$$

Obviously, if α is 0, the gain is 2. The capacitor mismatch ε of C_{fx} has no influence on the gain, so C_{bx} need not to be equal with C_{fx}.

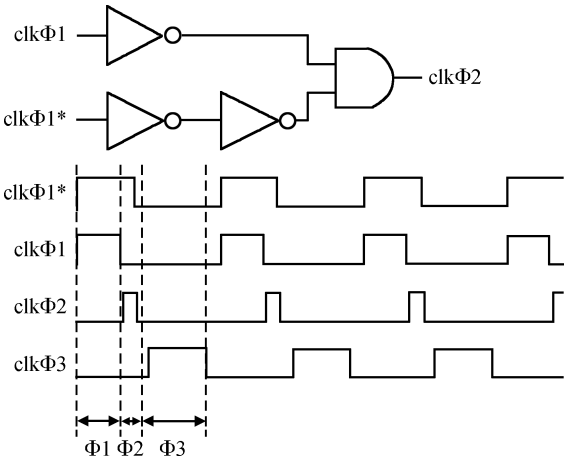

Fig. 7. Timing design of proposed MBT amplifier circuit.

3.4. Timing design

Advanced turning-off clock technology is usually used to alleviate the problem of channel charge injection[11]. Because the parasitic capacitor is very small, only little charge need to move in charge-complement phase and the time of this phase can be very short. Therefore the clock of the charge-complement phase can be produced by using a normal clock clkΦ1* and an advanced turning-off clock clkΦ1, as shown in Fig. 7. Although three phases are used in the circuit, the whole process can be completed in one clock cycle. It is also necessary that clkΦ2 and clkΦ3 should not be turned on at the same time.

Only switches Φ1* are controlled by clkΦ1*. Other switches closed in phase Φ1 are controlled by clkΦ1.

3.5. Feedback factor and amplifier settling

For the conventional circuit in Fig. 1, we have feedback factor $\beta = C_{ax}/(C_{ax} + C_{bx}) = 1/2$. For the proposed circuit in Fig. 5, obviously $\beta = 1$. The output settling to N-bit accuracy in the time period T leads to the following requirement for gain bandwidth[12]:

$$\mathrm{GBW} > \frac{N \ln 2 C_{\mathrm{L,tot}}}{2\pi T \beta C_{\mathrm{L}}}. \tag{11}$$

C_{L} is an open-loop load capacitor and $C_{\mathrm{L,tot}}$ is a closed-loop effective load capacitor. According to Eq. (11), the proposed circuit has a higher GBW. Usually we consider the phase margin of open-loop amplifier at the unity gain frequency. So the phase margin of the proposed circuit can also give a good indication of the settling time.

3.6. Thermal noise

The sampled-and-held *kT/C* noise from the sampling switches in the sample phase and the charge-complement phase and the broadband noise contribution from the amplifier in the amplification phase should be taken into account. The analysis of broadband noise is not important here, because circuits with same amplifier have the same output-referred mean squared noise.

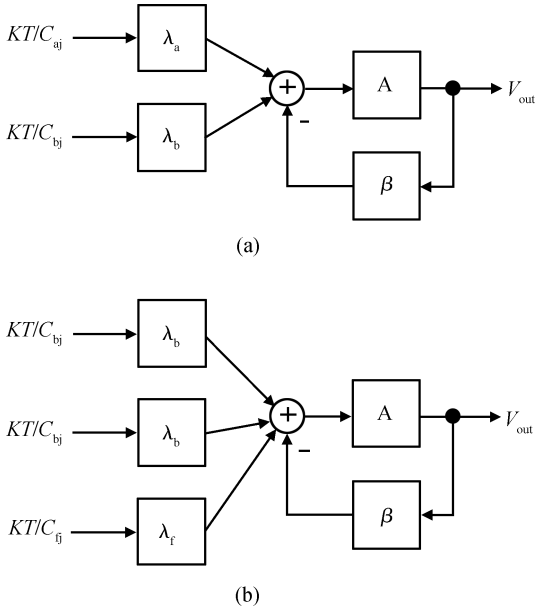

Fig. 8. Simplified block diagram for kT/C noise analysis. (a) Conventional circuit. (b) Proposed circuit.

For *kT/C* noise analysis, we can use the simple model shown in Figs. 8(a) and 8(b). The *KT/C* noise is contributed by C_{x} to the input of amplifier is $(kT/C_x)\lambda_x^2$. In the conventional circuit, $\lambda_{\mathrm{a}} = C_{\mathrm{ax}}/(C_{\mathrm{ax}}+C_{\mathrm{bx}}) = 1/2$ and $\lambda_{\mathrm{b}} = C_{\mathrm{bx}}/(C_{\mathrm{ax}}+C_{\mathrm{bx}}) = 1/2$. The equation of *kT/C* noise according to the block diagram in Fig. 8(a) is[13]

$$\overline{v^2_{\mathrm{noise}(kT/C)}} = 2\left(\frac{kT}{C_{\mathrm{ax}}}\frac{\lambda_{\mathrm{a}}^2}{\beta^2} + \frac{kT}{C_{\mathrm{bx}}}\frac{\lambda_{\mathrm{b}}^2}{\beta^2}\right) = \frac{4kT}{C}. \tag{12}$$

In the proposed circuit, $\lambda_{\mathrm{f}} = 1$ and $\lambda_{\mathrm{b}} = 1$. Assuming $C_{\mathrm{fx}} = C_{\mathrm{bx}}$, the equation of *kT/C* noise is

$$\overline{v^2_{\mathrm{noise}(kT/C)}} = 2\left(\frac{kT}{C_{\mathrm{fx}}}\frac{\lambda_{\mathrm{f}}^2}{\beta^2} + 2\times\frac{kT}{C_{\mathrm{bx}}}\frac{\lambda_{\mathrm{b}}^2}{\beta^2}\right) = \frac{6kT}{C}. \tag{13}$$

From Eqs. (12) and (13), we can find that the *kT/C* noise is 3/2 higher in the proposed circuit. If the *kT/C* noise is fatal, we can use larger capacitors to reduce the noise.

4. Simulations of proposed MBT amplifier circuit

We realized the circuit in a 0.18 μm CMOS technology, which is the same as the one used to realize the conventional circuit and simulate the circuit with Spectre. Normal CMOS switches and a folded cascade OPA with gain of 69 dB are used in these simulations. Actual models are used in all simulations. The unit capacitor C is 1 pF.

4.1. Simulations of nonidealities

Typical values in deep submicrometer CMOS technologies (e.g., 0.18 μm) with MIM capacitors are $\sigma(\varepsilon) = 0.2\%$ and $\alpha = 0.25\%$, where σ is standard deviation[9]. Figure 9 shows the simulation results of gain error (GE) versus capacitor mismatch ε when α is 0.25%. Figure 10 shows the simulation results of

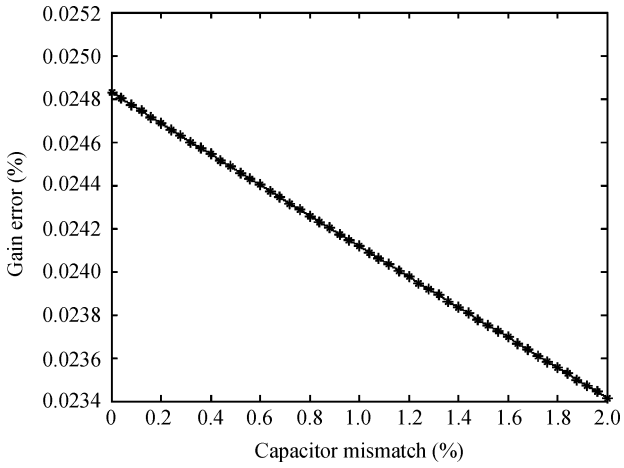

Fig. 9. Gain error versus capacitor mismatch of the proposed circuit when parasitic factor α is 0.25%.

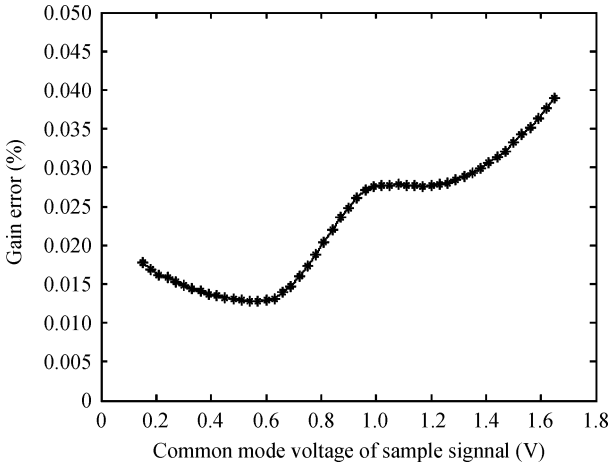

Fig. 11. Gain error versus capacitor mismatch of the reality circuit when parasitic factor α is 0.25%.

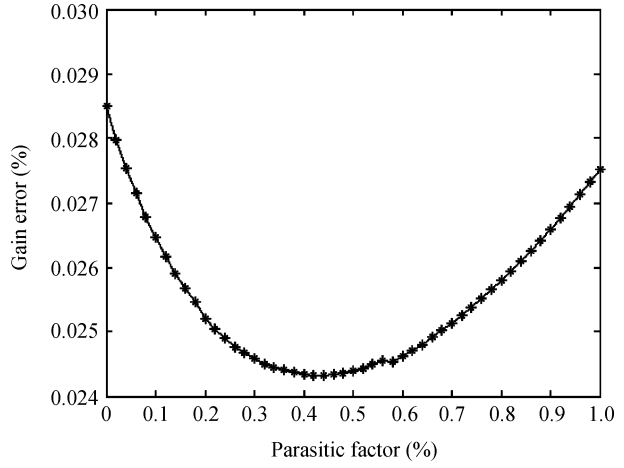

Fig. 10. Gain error versus parasitic factor α of the proposed circuit when capacitor mismatch ε is 0.

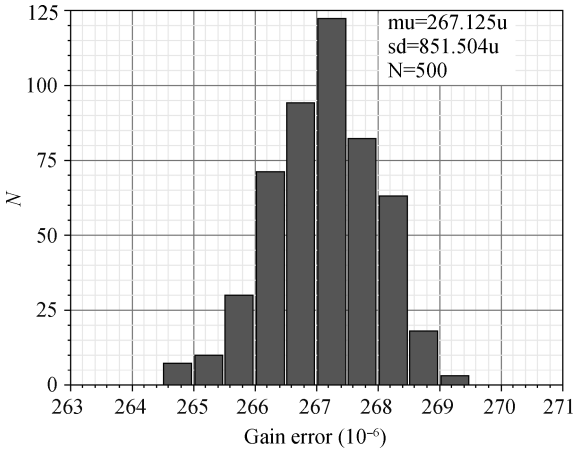

Fig. 12. Standard deviation of the GE of the proposed MBTA circuit versus the normal distributed MIM capacitance process and mismatch.

GE versus parasitic factor α when ε is 0. The difference of gain error between $\varepsilon = 0$ and $\varepsilon = 0.2\%$ in the conventional circuit and the proposed circuit are about 0.08% and 0.00015%. Compared with Ref. [9], the difference of gain error between $\varepsilon = 0$ and $\varepsilon = 0.2\%$ in Ref. [9] is 0.002%.

Different common mode voltages of the sample signal lead to a change of the characteristic of CMOS switches, especially switches connected to the sample signal terminal. The simulation results of gain error versus the common mode voltage of the sample signal are shown in Fig. 11. The difference between the minimum and maximum GE is less than 0.03%.

4.2. Monte Carlo and corners simulations

We have analyzed the situation when MIM capacitors are used in proposed circuit. Figure 12 displays the simulated standard deviation of the GE (Monte Carlo simulations for 500 cases) of the proposed MBTA circuit versus the normal distributed MIM capacitance process and mismatch. The range of GE is from 0.02645% to 0.02695%. The results of Monte Carlo simulation verify that the proposed circuit is insensitive to capacitor mismatches. Corners simulation results are shown in Tables 1–3. In all corners, the proposed circuit can satisfy the requirement of accuracy.

4.3. Output spectrum

A 1024-bin fast Fourier transform of the simulated differential output is shown in Fig. 13. The input signal is a 120 kHz sinusoidal differential signal with amplitude of 0.3 V and the sampling frequency is 4 MS/s. In the simulation, the sample capacitors are 1 pF and parasitic factor α is 0.25%. Simulation results exhibit that when $\varepsilon = 0$, the THD is better than –73.18 dB; and when $\varepsilon = 0.2\%$, the THD is better than –73.17 dB. In both simulations, the THD is mainly dominated by the second harmonic.

5. Conclusion

A switched-capacitor MBT amplifier with reduced capacitors mismatches sensitivity and full swing sample signal common-mode voltage is proposed here. Only one amplifier is used to achieve the gain of two in only one clock cycle. Compared with a conventional MBT amplifier circuit, the difference of gain error between $\varepsilon = 0$ and $\varepsilon = 0.2\%$ in the

Table 1. Corner simulation results for parasitic factor.

Corner	Parasitic factor (%)	Gain error (%)
tt	0	0.028501
	0.2	0.025202
	0.5	0.02439
ff	0	0.032499
	0.2	0.029751
	0.5	0.028688
ss	0	0.01475
	0.2	0.011167
	0.5	0.008895
fs	0	0.027275
	0.2	0.024629
	0.5	0.023968
sf	0	0.027258
	0.2	0.02411
	0.5	0.023331

Table 2. Corner simulation results for capacitor mismatch.

Corner	Capacitor mismatch (%)	Gain error (%)
tt	0	0.024832
	0.2	0.024686
	0.4	0.024543
ff	0	0.029371
	0.2	0.02922
	0.4	0.02907
ss	0	0.010617
	0.2	0.010461
	0.4	0.010305
fs	0	0.024306
	0.2	0.024164
	0.4	0.024022
sf	0	0.023756
	0.2	0.023612
	0.4	0.023469

Table 3. Corner simulation results for common mode voltage of sample signal (Vscm).

Corner	V_{scm} (V)	Gain error (%)
tt	0.15	0.017783
	0.9	0.024829
	1.65	0.038913
ff	0.15	0.035594
	0.9	0.029371
	1.65	0.0386
ss	0.15	0.016063
	0.9	0.010617
	1.65	0.040257
fs	0.15	0.019706
	0.9	0.024306
	1.65	0.039803
sf	0.15	0.017085
	0.9	0.023756
	1.65	0.037651

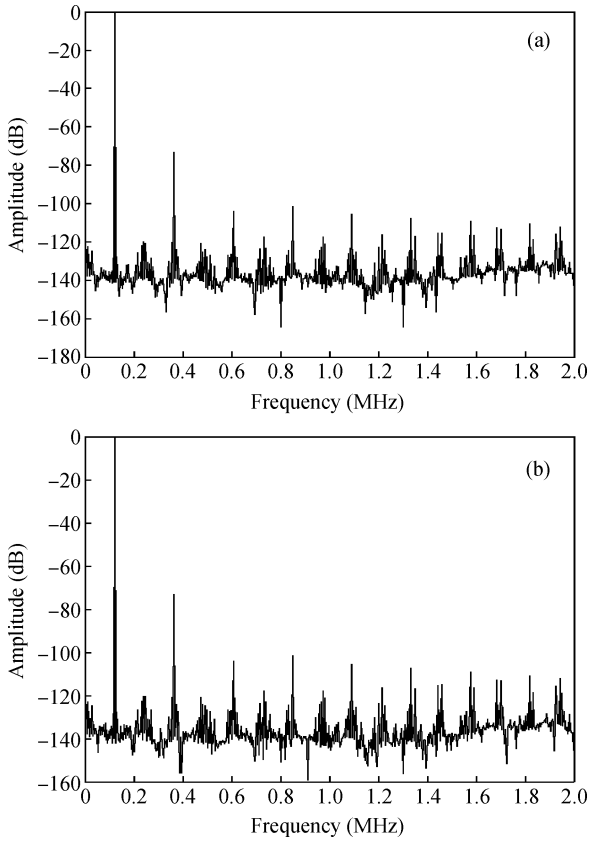

Fig. 13. Simulated FFT spectrum of the output signal of the proposed MBTA circuit operating at 4 MHz when a 120 kHz input signal is applied. (a) $\varepsilon = 0$, $\alpha = 0.25\%$. (b) $\varepsilon = 0.2\%$, $\alpha = 0.25\%$.

conventional circuit and proposed circuit are about 0.08% and 0.00015%.

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