A digital prediction algorithm for a single-phase boost PFC*

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Abstract: A novel digital control algorithm for digital control power factor correction is presented, which is called the prediction algorithm and has a feature of a higher PF (power factor) with lower total harmonic distortion, and a faster dynamic response with the change of the input voltage or load current. For a certain system, based on the current system state parameters, the prediction algorithm can estimate the track of the output voltage and the inductor current at the next switching cycle and get a set of optimized control sequences to perfectly track the trajectory of input voltage. The proposed prediction algorithm is verified at different conditions, and computer simulation and experimental results under multi-situations confirm the effectiveness of the prediction algorithm. Under the circumstances that the input voltage is in the range of 90–265 V and the load current in the range of 20%–100%, the PF value is larger than 0.998. The startup and the recovery times respectively are about 0.1 s and 0.02 s without overshoot. The experimental results also verify the validity of the proposed method.

Key words: PFC; digital control; prediction; transient performance

DOI: 10.1088/1674-4926/33/12/125007 **EEACC:** 2570

1. Introduction

The switching power supply is widely used in electrical systems, industry, transport, and electrical appliances, which, however, leads to the decrease of input power factor and the increase of harmonic pollution on the power grid. For the reason that switching power supply has become the primary source of harmonic pollution, it is inevitable that power factor correction is applied. In the design process of power factor correction (PFC) converters, in addition to considering the system's stability, higher power factor (PF) with lower total harmonic distortion (THD) is more important in the control loop design.

In analog implementations of PFC converters, numerous control methods have been explored to improve system performance. The early passive PFC (PPFC), which uses an LC filter, has been abandoned because of its larger size and poor PF modulation. Now the active PFC (APFC) is widely adopted, which works at high frequency for small inductance and capacitance, and the PF value can be as high as 0.999. Dual-loop control technology is usually used to enhance the dynamic performance in a continuous current mode APFC, such as average/peak current control[1−5], hysteretic control[6, 7], etc. In addition, some non-linear control strategies are proposed to simplify the control strategy, such as the sliding mode variable structure control and deadbeat control. A novel control method—single-cycle control[8−10]—was proposed in the early 1990s by Smedley, which eliminated the need for input voltage sensing and the multiplier in current loop compensation in order to simplify the design complexity. The control strategies above have been confirmed as being effective for PFC systems and have been implemented in some typical products, such as ML4812 and UC3854 using dual-loop control, and IR1150 using single-cycle control.

However, the increased requirements in integration and cost cause some limitations in analog implementation strategies due to its poor anti-aging, anti-jamming, and relatively weak adaptability. Especially, once the circuit parameters changes, the control loop needs to be redesigned and complex control methods are also difficult or costly to be implemented. The employment of digital technology can overcome these problems, as it is more suitable for accomplishing the required control loop complex data processing and flexible algorithms required for enhancing performance. For example, the first digital control PFC chip, CS1500, uses a piecewise digital algorithm to provide the higher efficiency at full load, especially under a light load. Sampling data show that the efficiency of CS1500 is up to 93% at 10% load, which is far more superior to the maximum value 88% at the same load condition in the analog PFC. The number of external components is reduced by 30% or more, simplifying system design. In addition, the digital implementation with the help of EDA tools can greatly shorten the design cycle, which analog design cannot be comparable with.

However, directly realizing the analog scheme using digital technology will cause many problems. For instance, the basic multiplier, needed in the implementation of dual loop control strategies, will inevitably introduce a delay affecting the control effect, and at the core of the analog single-cycle PFC is a high-speed integrator which is more complicated to be implemented with a digital algorithm.

In this paper, a real-time predictive method based on a boost circuit structure is put forward in a digital controller. This method calculates the orbits of inductor current and out-

* Project supported by the Natural Science Foundation of Jiangsu Province, China (Nos. BK2010167, BK2011059), the Program for New Century Excellent Talents in University, China (No. NCET-10-0331), and the Qing Lan Project.

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Received 11 April 2012, revised manuscript received 24 June 2012

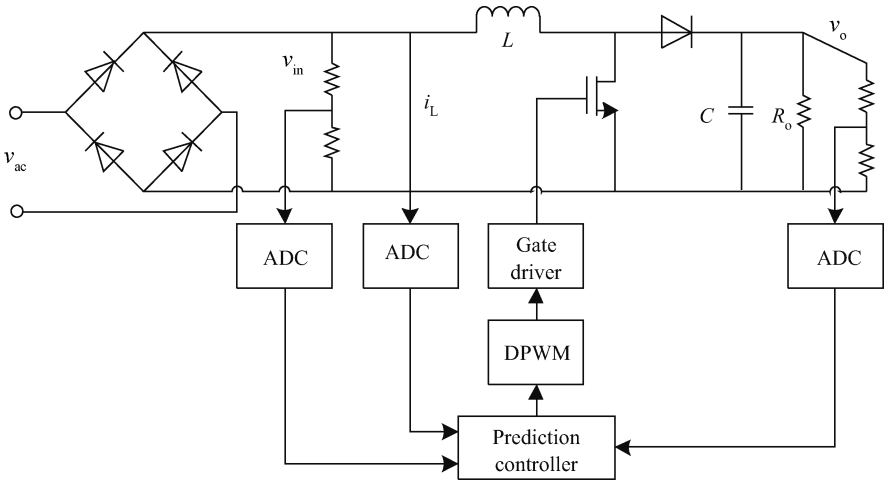


Fig. 1. The structure of a digital controlled boost converter with the proposed control method.

put voltage before the beginning of the next switching period based on the sampling input voltage, inductor current, output voltage, and the duty ratio in the current period, which enables the input current to track the input voltage better. The theory of the real-time prediction method and the treatment process are introduced in this paper. The simulation and experiment results in dynamic and steady states are shown and analyzed.

2. The idea of prediction method

In general, a digital control loop consists of analog-digital conversion (ADC), an algorithm controller, and a digital pulse width modulator (DPWM). Figure 1 shows the basic structure of a boost PFC converter with the prediction method of the digital control algorithm as an example.

For a given system, duty ratio is the unique controlled variable for system operation. Regardless of whether the power system is in a steady-state or a dynamic-state, the relationship of voltage and current abides by the same rules. According to the different state of the MOSFET, boost converters have two topologies. Because the inductor current cannot change instantaneously, the relationship is described by

$$\frac{\mathrm{d}i_{\mathrm{L}}}{\mathrm{d}t}=\frac{v_{\mathrm{L}}}{L}=\begin{cases}\dfrac{v_{\mathrm{in}}-v_{\mathrm{o}}}{L}, & \text{MOSFET is off,}\\ \dfrac{v_{\mathrm{in}}}{L}, & \text{MOSFET is on.}\end{cases} \tag{1}$$

If all the circuit parameters are determined, including constant switching frequency, inductor (L), and output capacitor (C), it is not difficult to estimate the output voltage and the inductor current of the next cycle according to Eq. (1). Detailed formulas and steps are as follows:

Step 1: the acquisition of the initial values, which includes: (1) some drivers' parameters such as load resistance (R_{o}), inductance (L), and capacitance (C). (2) the duty ratio at current cycle $d[k]$ and the samples of input voltage $v_{\mathrm{in}}(t)$, output voltage $v_{\mathrm{o}}(t)$, inductance current $i_{\mathrm{L}}(t)$ at current cycle, which are transformed into digital signals $v_{\mathrm{in}}[k]$, $v_{\mathrm{o}}[k]$, $i_{\mathrm{L}}[k]$.

Step 2: The estimation of $v_{\mathrm{o}}[k+1]$ and $i_{\mathrm{L}}[k+1]$ at the next cycle by using the following formulas.

$$\begin{cases} i_{\mathrm{L}}[k+1]=i_{\mathrm{L}}[k]+\dfrac{v_{\mathrm{in}}[k]}{L}dT_{\mathrm{s}}+\dfrac{v_{\mathrm{in}}[k]-v_{\mathrm{o}}[k]}{L}(1-d)T_{\mathrm{s}},\\ v_{\mathrm{o}}[k+1]=v_{\mathrm{o}}[k]+\dfrac{v_{\mathrm{o}}[k]}{RC}dT_{\mathrm{s}}+\dfrac{i_{\mathrm{av}}[k]-v_{\mathrm{o}}[k]/R}{L}\\ \qquad\qquad\times(1-d)T_{\mathrm{s}}, \end{cases} \tag{2}$$

where the average current $I_{\mathrm{av}}[k]$ can be calculated by

$$i_{\mathrm{av}}[k]=\frac{i_{\mathrm{L}}[k]+2\dfrac{v_{\mathrm{in}}[k]}{L}dT_{\mathrm{s}}+i_{\mathrm{L}}[k+1]}{4}. \tag{3}$$

When we estimate $i_{\mathrm{L}}[k+1]$ and $v_{\mathrm{o}}[k+1]$ of the next cycle, the curve trend can be estimated before it takes place. For an ideal steady-state PFC, the trend of i_{L} should track the sinusoidal waveforms of input voltage v_{in} and the output voltage v_{o} should be stable near the reference value. So in the process of a duty cycle acquisition, we can examine whether the curves of $v_{\mathrm{o}}[k]$, $i_{\mathrm{L}}[k]$ are in line with the expectations of the ideal system by simulation and computation, and thus further indicate the correctness and effectiveness of the duty cycle.

3. The specific implementation of the prediction algorithm

An assessment for a power system usually consists of two aspects, namely dynamic performance and steady performance[13−16]. The process of adjusting controlled parameters close to the expectation during the startup of a system or the response for the change of the load current/input voltage belongs to the dynamic state. Shorter response time and overshoot are expected in this process. When the output variable is near the expectation, the system enters into the steady state. The concerns of steady-state performance indexes vary from one system to another. In a converter system, ripple voltages are the most important indexes. While for a PFC system, the PF value is the most important. Therefore, for a PFC system, an optimal control should meet both fast transient response and high PF value in different cases. Two different control algo-

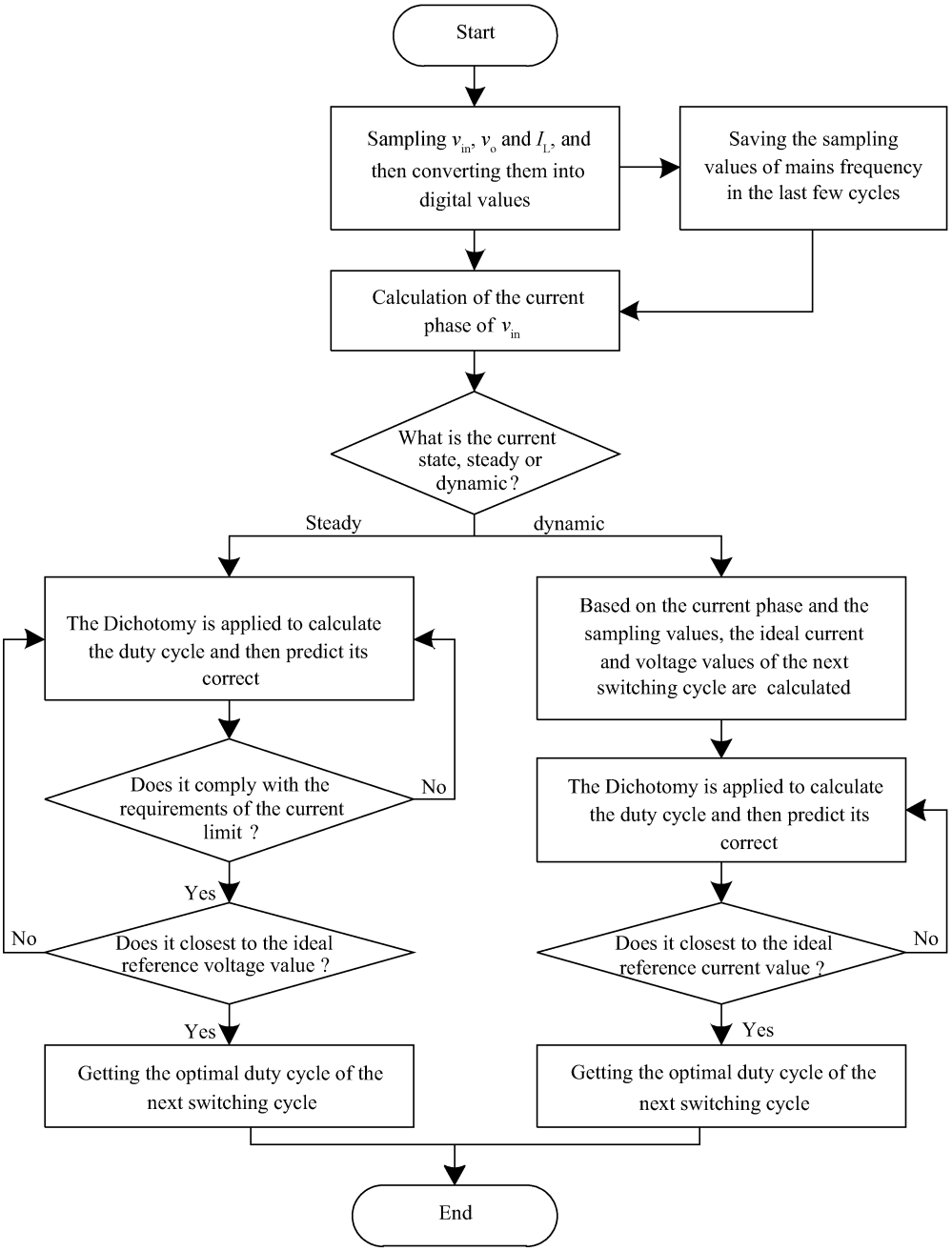


Fig. 2. Flow chart of the proposed prediction algorithm using a PFC.

rithms should be designed separately in the dynamic state and the steady state.

For a boost PFC system, the dynamic algorithm aims at making output voltage $v_o(t)$ achieve the expected value as fast as possible at different cases. The input voltage after the rectifier bridge is a half-sinusoidal waveform, and $v_o(t)$ varies quickly near the input voltage's peak point where the larger duty ratio provided by the dynamic algorithm is needed to increase inductor current and improve transient response.

The steady algorithm has two characteristics. One is to keep output voltage $v_o(t)$ around the expectation, the other is to let inductor current $i_L(t)$ track input voltage $v_{in}(t)$ synchronously to obtain a better PF value. According to the phase and amplitude of $v_{in}(t)$, the most accurate value of $i_L[k+1]$ that tracks $v_{in}[k+1]$ at the next cycle can be estimated easily by the proposed prediction method, and the duty ratio $d[k+1]$ should be obtained. Note that the influence of delay time is ignored here[11, 12].

The process of the control algorithm operates as follows:

Step 1: acquiring some initial values as shown in step 1 of Section 2. All of these values are indispensable in the control algorithm. Components' parameters will affect the dynamic or steady performance of system. It is prerequisite to evaluate the performance of various algorithms in the determined parameters. Updating the sampling at the beginning of every switching cycle can avoid the accumulation of prediction error.

Step 2: because the changes of $v_{in}(t)$ are cyclical, the current phase of $v_{in}(t)$ can be ensured based on the previous samples. However, at the startup process of the input port access to

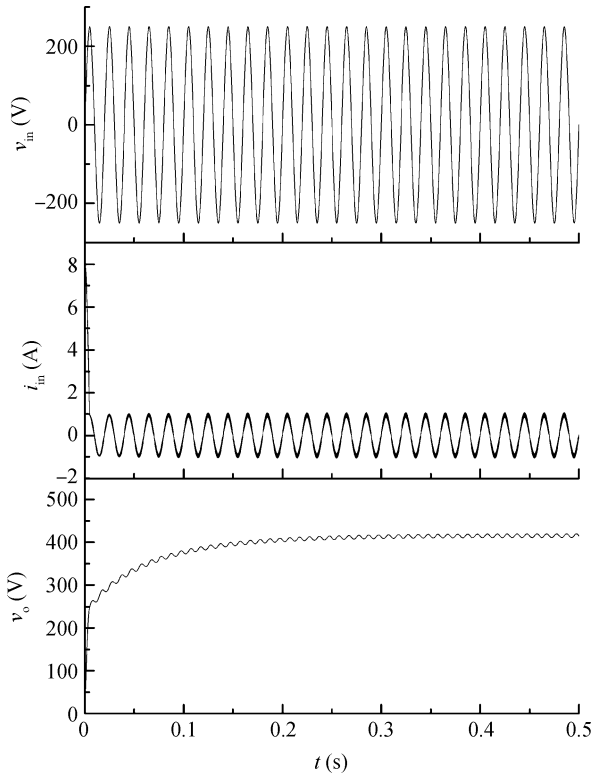


Fig. 3. Waveforms of v_o and i_{in} when $v_{in} = 250$ V (maximum value).

commercial power, at least half power cycle is needed to detect phases.

Step 3: comparing the sample of $v_o[k]$ with the expected reference value to determine the system's current state, steady state or dynamic state.

Step 4: if in the dynamic state, the proposed prediction algorithm can be used in a rapid regulator. According to the values of $i_L[k+1]$ and $v_o[k+1]$, on the premise that $i_L[k+1]$ is not overshot, the optimal duty ratio for dynamic response can be achieved when $v_o[k+1]$ is closed to the expectation. In other words, in cases where the inductor current does not exceed the limit, make the output voltage of the next cycle closer to the reference. If the duty cycle meets the above conditions, it will speed up response time.

Step 5: if in the steady state, the first step is to calculate the input current value that can perfectly track the input voltage curve. Then the duty cycle can be calculated by using the proposed prediction algorithm. Ideal $i_L[k+1]$ can be calculated according to the power frequency phase of input voltage, to satisfy PFC. After that, different values of $i_L[k+1]$ under different duty ratios can be predicted by using the dichotomizing search. The optimal duty cycle for the PFC is obtained when the value of $i_L[k+1]$ is close to the ideal one. The PF value is improved in real-time sinusoidal tracking, and optimized THD and reduced phase difference between input voltage and input current are realized.

The above control algorithm runs once per cycle to calculate the optimal duty ratio of this cycle and then controls the DPWM to adjust the converter system. The flow chart of the above steps can be found in Fig. 2.

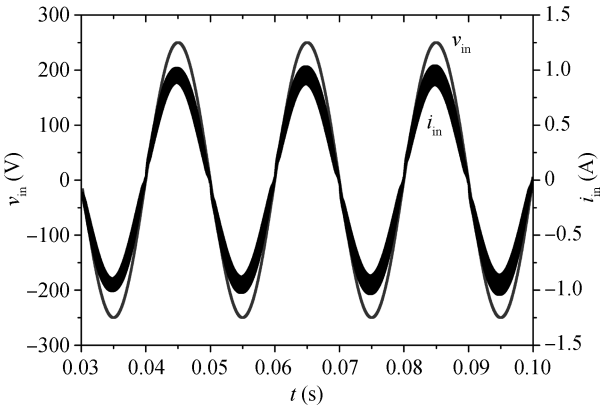


Fig. 4. Waveforms of input voltage v_{in} and input current i_{in}.

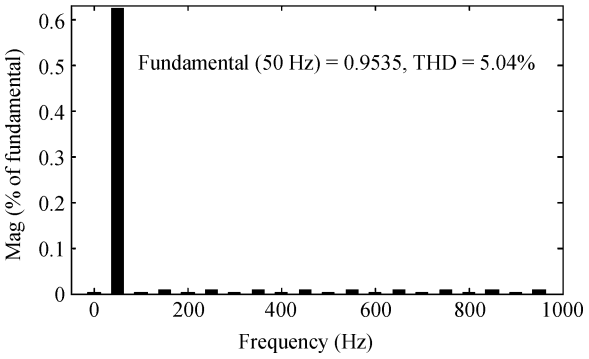


Fig. 5. Spectrum of input current i_{in}.

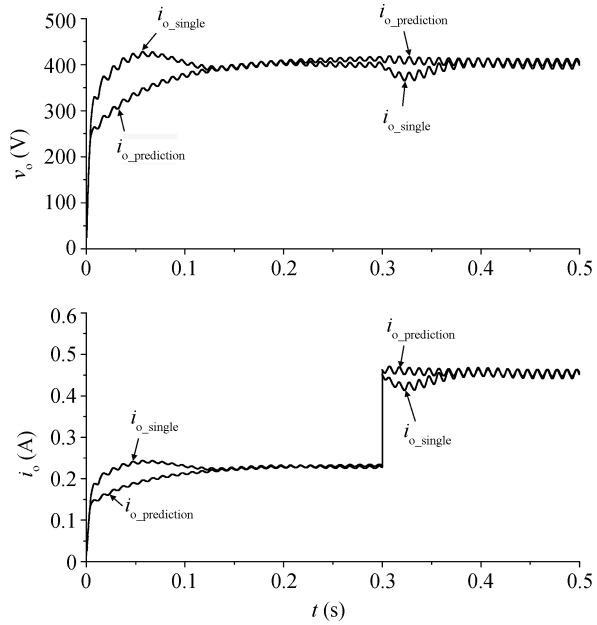


Fig. 6. Waveforms of output voltage v_{out} with the load change.

4. Computer and experiments results

The effectiveness of proposed algorithm has been verified by MATLAB-Simulink. The parameters of the boost PFC converter are listed as follows: $v_{in} = 90$–265 V, $v_o = 400$ V, $L = 4.7$ mH, $C = 100$ μF, $P_{out,max} = 300$ W. The switching

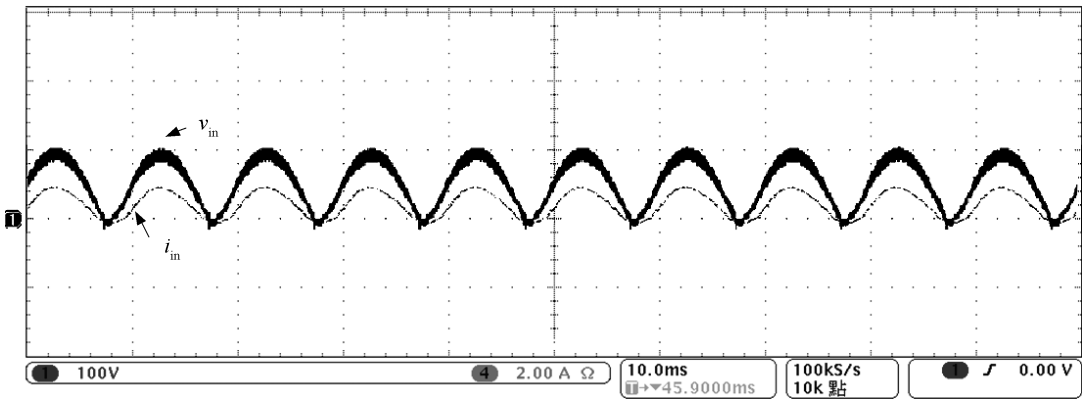
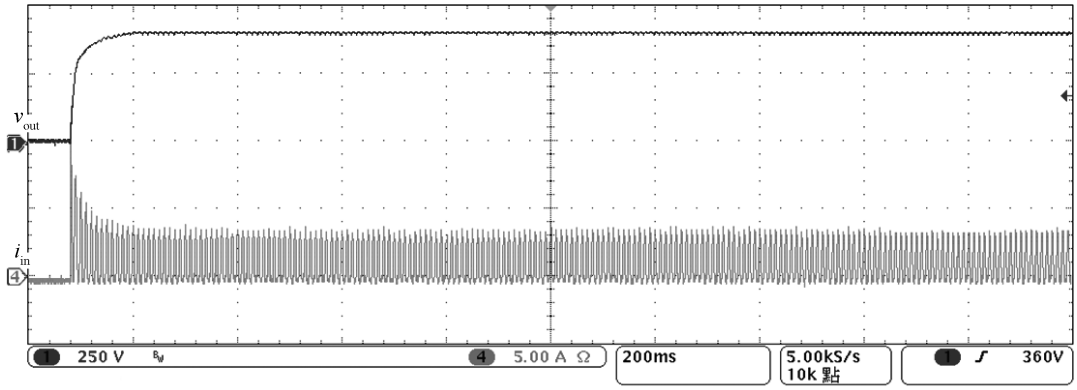
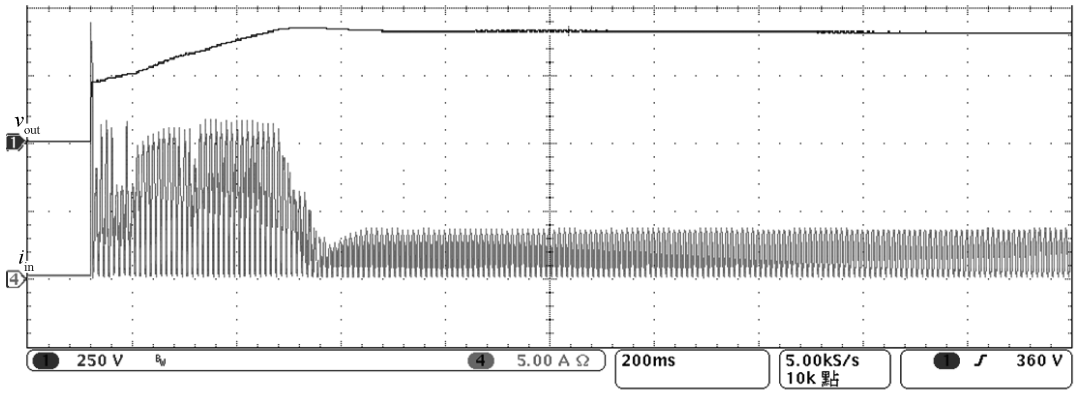


Fig. 7. Waveforms of input voltage v_{in} and input current i_{in} after the rectifier bridge.



(a) Test waveforms with the prediction algorithm



(b) Test waveforms with the single-cycle algorithm

Fig. 8. Waveforms of v_o and i_{in} in the startup process.

frequency and sampling frequency are both 100 kHz.

Figure 3 shows the waves of the input voltage $v_{in}(t)$, input current $i_{in}(t)$, and output voltage $v_o(t)$ from top to bottom when the maximum input voltage is 250 V at the rated load. The simulation results show that $i_{in}(t)$ tracks $v_{in}(t)$ in real-time, and that the proposed prediction algorithm has a good power factor correction effect.

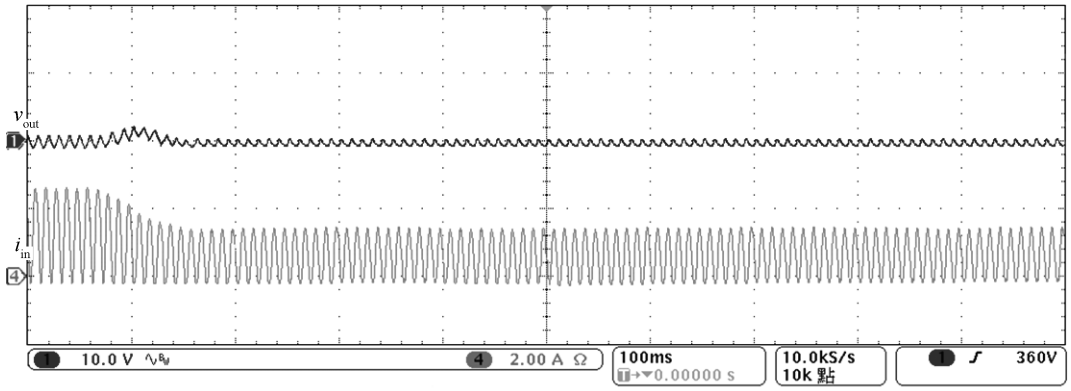
Figure 4 exhibits the comparison between the modulated input current and the input voltage. Figure 5 exhibits the input current spectrum. From the two figures, we can see that the phase is in conformance with input voltage and input current, and almost has no cross-over distortion, so there are fewer high harmonics, and PF is up to 0.998.

Figure 6 gives the situation of the output voltage following the load current change with single-cycle control and the proposed control method. When the load changes from light to high, with the prediction algorithm controller the output voltage remains stable except that the ripple becomes larger, while with the single-cycle controller the undershoot of the output voltage is about 12%.

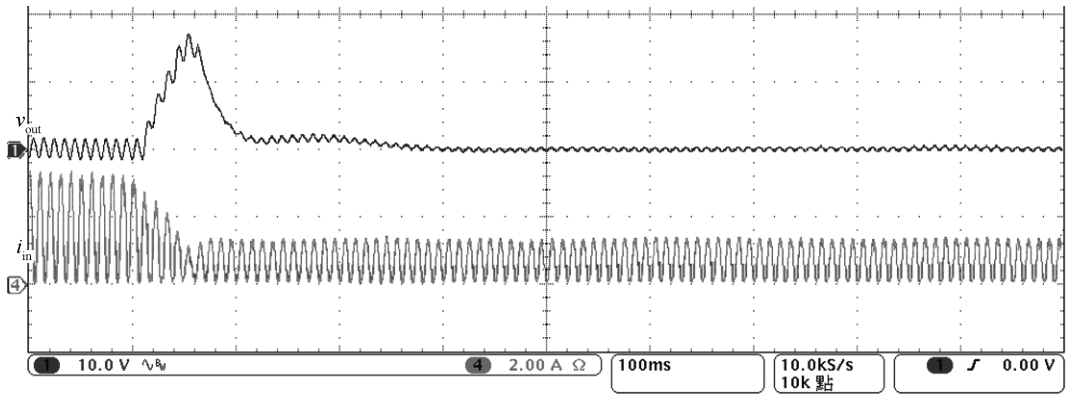
Table 1 summarizes the simulation results of a boost PFC with the proposed prediction algorithm in various kinds. It is observed from above simulation and Table 1 that proposed prediction algorithm can achieve excellent performance in any conditions. Whatever the index is, over/undershoot, startup time or recovery time, all of them produce more superior results

Table 1. Parameters of a boost PFC with the proposed prediction algorithm.

v_{in} (V) (maximum value)	Steady parameter			Dynamic parameter (50% $i_o \rightarrow$ 100% i_o)			
	ΔV_o (V)	PF	THD (%)	Start up (s)	Recover (s)	Overshoot	Deviation (V)
150	7	$\approx$ 0.998	5.90	0.11	0.025	$\approx$ 0	5
250	8	$\approx$ 0.998	5.04	0.15	0.02	$\approx$ 0	7
300	10	$\approx$ 0.998	5.92	0.076	0.018	$\approx$ 0	7



(a) Test waveforms with the prediction algorithm



(b) Test waveforms with the single-cycle algorithm

Fig. 9. Output voltage response with the load change from 0.8 A to 0.4 A.

than other control methods. However, it is noteworthy that using the prediction algorithm to estimate the track of the output voltage and the inductor current at the next switching cycle is based on the current system state parameters, so this algorithm depends on the system parameters and the calculation increases significantly with the increase of calculation accuracy. When synthesized with an FPGA, the number of standard cells of the proposed controller is five times larger than that of the single-cycle controller.

A test system with the same condition as the simulation is built to verify the prediction algorithm with the help of an FPGA. Figure 7 is a comparison between the input current and the input voltage, and the reading of the voltmeter shows the PF value is 0.96 due to some cross-over distortion. Figure 8 shows the test waveforms. Please note that a difference probe is used to test the output voltage with 500× attenuation. The accuracy of the sampling resistor and sampling circuit speed may affect the compensation, resulting in crossover distortion.

Figures 8 and 9 illustrate the startup process and the output voltage response following the load current change with two control algorithms, respectively. The startup time with the proposed algorithm is about 10 power frequency cycles, about 30 power frequency cycles faster than single-cycle control method. And the setting time with the load current change is approximately 80 ms (about 4 power frequency cycles), and the overshoot is about 6% under the proposed algorithm control, better than the single-cycle controller. According to Fig. 9(a), the efficiency is about 96% in heavy load and then becomes 90% when the load becomes a half of the original.

Several papers whose design specifications are identical or similar to this article are picked out and comparisons of their static and dynamic performances are listed in Table 2. The efficiency, setting time, and the overshoot voltage in the proposed PFC are competitive, but power factor is a little bit worse. Moreover, note that the calculation of the proposed algorithm will be greatly increased with the improvement in prediction accuracy, and at the same time hardware resources will be occupied more significantly and the efficiency will be reduced.

5. Conclusion

The development trends of PFC are requiring advanced

Table 2. PFC parameters in different papers.

Parameter	This work	Ref. [18]	Ref. [19]	Ref. [20]	Ref. [21]
Operating conditions	$V_{in} = 220V_{ac}$ $P_{out} = 300$ W $V_{out} = 400$ V $f_{sw} = 100$ kHz	$V_{in} = 220V_{ac}$ $P_{out} = 300$ W $V_{out} = 400$ V $f_{sw} = 100$ kHz	$V_{in} = 110V_{ac}$ $P_{out} = 225$ W $V_{out} = 48$ V $f_{sw} = 100$ kHz	$V_{in} = 220V_{ac}$ $P_{out} = 300$ W $V_{out} = 380$ V $f_{sw} = 100$ kHz	$V_{in} = 100V_{ac}$ $P_{out} = 300$ W $V_{out} = 392$ V $f_{sw} = 50$ kHz
Power factor	0.96	0.995	0.98	0.999	/
Efficiency (%)	95.87	/	96	/	95.1
Settling time (ms)	80	20	150	200	100
Overshoot/Undershoot (%)	6	4	4.6	5.3	5
Load change (%)	$50 \rightarrow 100$	$100 \rightarrow 50$	$30 \rightarrow 100$	$100 \rightarrow 67$	$20 \rightarrow 70$

control strategies, reducing product costs, EMI, THD, and device switching stress, and improving system efficiency. This paper presents a new digital algorithm, named the prediction algorithm, which, operating in CCM, can effectively improve the system dynamics and static performance. The amount of algorithm calculation is relatively great but the simulation results show that by using this algorithm, the power factor and efficiency are higher. The experimental results include some unsatisfactory PF values, which may be due to inappropriate implementation. So the next research will be to further improve these performances.

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