Design and implementation of an ultra-low power passive UHF RFID tag*

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Abstract: This paper presents a fully integrated passive UHF RFID tag chip complying with the ISO18000-6B protocol. The tag chip includes an RF/analog front-end, a baseband processor, and a 512-bit EEPROM memory. To improve power conversion efficiency, a Schottky barrier diode based rectifier is adopted. A novel voltage reference using the peaking current source is discussed in detail, which can meet the low-power, low-voltage requirement while retaining circuit simplicity. Most of the analog blocks are designed to work under sub-1 V to reduce power consumption, and several practical methods are used to further reduce the power consumption of the baseband processor. The whole tag chip is implemented in a TSMC 0.18 μm CMOS process with a die size of 800×800 μm^2. Measurement results show that the total power consumption of the tag chip is only 7.4 μW with a sensitivity of –12 dBm.

Key words: UHF RFID tag; voltage reference; demodulator; low power
DOI: 10.1088/1674-4926/33/11/115011 **EEACC:** 2570

1. Introduction

Passive radio frequency identification (RFID) tags operating in the UHF band are showing a wide range of prospective applications for their advantages of low cost, long operating distance, high data rate, and small antenna size[1]. The commercial applications of passive UHF RFID tags are diverse, including intelligent transportation systems, asset tracking, supply-chain management, logistics, and many other areas[2–5].

A passive tag operates without using a battery, and it gathers power from the incident RF power generated by an RFID reader. Because the operating range of the UHF RFID system is highly dependent on the power consumption of the tag[6], it is crucial to design ultra-low power circuits for passive tags to guarantee longer communication distances.

In this paper, an ultra-low power passive UHF RFID tag complying with the ISO18000-6B protocol is designed and implemented. Based on the traditional Dickson rectifier structure, we use a Schottky barrier diode instead of a diode-connected MOSFET to improve the power conversion efficiency of the rectifier. A novel voltage reference circuit using the peaking current source is designed to generate a stable voltage reference. In order to reduce the overall power, low power techniques such as power management, clock gating, and component reuse are applied to the baseband processor design. The tag chip is fabricated in TSMC 0.18 μm CMOS process with a die size of 800×800 μm^2.

2. Chip architecture

Figure 1 shows the block diagram of the proposed RFID tag, which includes a RF/analog front-end, a baseband processor, and an EEPROM memory. The RF/analog front-end performs all analog processing for DC power, receive signal detection/demodulation, and transmit modulation. The baseband processor decodes incoming data, responds to commands from the reader, reads and writes to the EEPROM memory.

The RF/analog front-end has several internal sub-blocks. The rectifier converts the RF energy from the reader into DC power to supply the whole system. A voltage limiter is used to avoid high voltage damage when the received power is high. A voltage reference and a voltage regulator generate a stable supply voltage. The system clock is generated by a current controlled ring oscillator. A power-on reset (POR) circuit resets the baseband processor when the supply voltage reaches a reliable, regulated level. In the forward link (reader to tag), the reader-to-tag data are demodulated from the envelope of the carrier. In the return link (tag to reader), the tag sends data back to the reader by load modulation. An energy storage capacitor Cs is employed to supply the chip in case of an energy gap.

3. Building blocks

3.1. Rectifier

In a passive RFID tag, the supply power is harvested from the input RF energy through the rectifier. The higher the power conversion efficiency of the rectifier, the more power the tag gains. A conventional rectifier circuit is based on a Dickson charge pump[7]. The voltage drop across the diode (about 0.7 V) is the main power loss factor. Substituting diodes with diode-connected MOS transistors can reduce power loss, but the voltage drop of diode-connected MOS transistors (about 0.5 V) is still too high.

In this paper, we use a Schottky barrier diode, which has a voltage drop of 0.3 V, to further reduce power loss. The rectifier circuit is shown in Fig. 2. The DC output voltage of the rectifier

* Project supported by the Shenzhen Key Laboratory Development Project, China (No. CXB201104210007A).
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Received 12 April 2012, revised manuscript received 14 June 2012

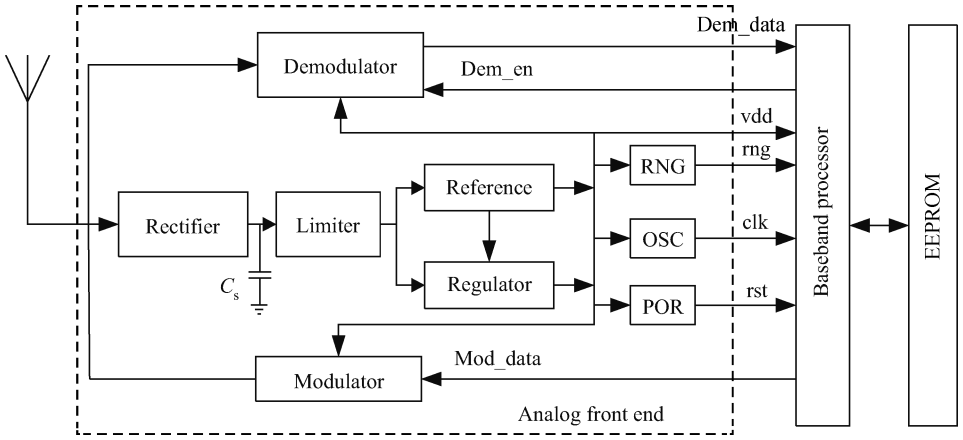

Fig. 1. Block diagram of the proposed RFID tag.

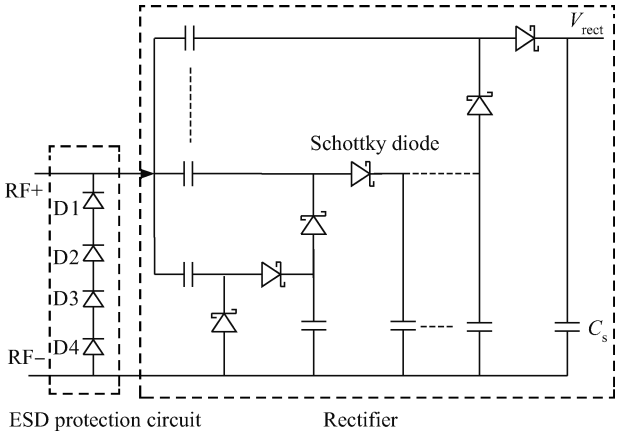

Fig. 2. Schematic of the proposed rectifier.

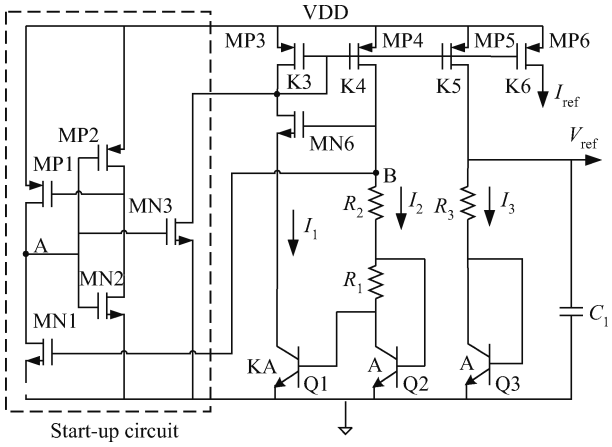

Fig. 3. Schematic of the proposed voltage reference.

can be approximately expressed as[8]

$$V_{\rm rect} = 2N(V_{\rm rf} - V_{\rm d}), \tag{1}$$

where N is the number of stages, $V_{\rm rf}$ is the amplitude of the input RF voltage, and $V_{\rm d}$ is the voltage drop on a Schottky barrier diode. From Eq. (1), it is clear that a larger N induces a higher output voltage. However, simulation results show that the conversion efficiency decreases when more stages are used. So we must choose an appropriate N to achieve the optimal value of the efficiency and output voltage. In our design, the stage number N is chosen to be 5.

3.2. Voltage reference

Due to the variable distance between the reader and the tag, the energy received from the electromagnetic field also varies, leading to a large variation of the output voltage of the rectifier (1.1–3 V in our system). Hence, a reference circuit is used to generate a stable voltage reference and it must be able to tolerate this large variation. A conventional band-gap reference circuit[9], which usually generates 1.25 V voltage reference, is not suitable for low-voltage design. Several sub-1 V voltage reference circuits are reported in Refs. [10, 11], but they do not fit the RFID tag because of their large power consumption.

The peaking current source[12, 13] has been recognized as a useful low-current reference. This work exploits the peaking current source to realize a low-power voltage reference. The proposed voltage reference circuit is depicted in Fig. 3. This circuit can meet the low-power, low-voltage requirement while retaining circuit simplicity.

Elements Q1, Q2 and R_1 constitute the peaking current source, while the elements MP3 and MP4, connected in a current mirror, serve to realize the function of self-biasing. The MP3, MP4 mirror is designed to make the collector current of Q1 and Q2 operate in the peaking relation, then the voltage across R_1 is proportional to the absolute temperature (PTAT). Thus, the resistor ratio R_3/R_1 can be used to compensate the variation of the base–emitter voltage of Q3 with respect to the temperature. A steady reference voltage output, $V_{\rm ref}$, is therefore obtained. The detailed analysis is as follows.

Ignoring base current, the collector currents of Q1 and Q2 can be given by

$$I_1 = I_{\rm S1} \exp \frac{V_{\rm BE1}}{V_{\rm T}}, \tag{2}$$

$$I_2 = I_{\rm S2} \exp \frac{V_{\rm BE2}}{V_{\rm T}}, \tag{3}$$

where $I_{\rm S1}$ and $I_{\rm S2}$ are the reverse saturation currents of Q1 and Q2, respectively, $V_{\rm T}$ is the thermal voltage, $V_{\rm BE1}$ and $V_{\rm BE2}$ are the base–emitter voltages of Q1 and Q2, respectively.

The relation between the two collector currents is, therefore,

$$I_1 = I_2 \frac{I_{S1}}{I_{S2}} \exp \frac{V_{BE1} - V_{BE2}}{V_T} = I_2 K \exp \frac{V_{BE1} - V_{BE2}}{V_T}, \quad (4)$$

where K is the emitter area ratio between Q1 and Q2.

The difference between the two base–emitter voltages of Q1 and Q2 can be expressed as

$$V_{BE1} - V_{BE2} = -I_2 R_1. \quad (5)$$

Substituting Eq. (5) into Eq. (4), we obtain

$$I_1 = I_2 K \exp\left(-\frac{I_2 R_1}{V_T}\right). \quad (6)$$

The peaking current source is designed such that I_1 is at its peaking value. It can be achieved by zeroing the derivative of I_1 with respect to I_2 using Eq. (6), yielding the following design condition

$$I_2 R_1 = V_T. \quad (7)$$

If the condition is satisfied, then the collector currents of Q1 and Q2 are related by

$$I_1 = I_2 K e^{-1}. \quad (8)$$

Hence, the self-biasing mirror constituted by MP3 and MP4 is designed to make I_1 and I_2 satisfy the relation in Eq. (8). And then the peaking condition (7) is maintained. In our design, we choose $K = 2$, then setting $K_3 = K_4 \times 2 \times e^{-1}$ will satisfy the peaking condition (K_3, K_4 are the width to length ratios of MP3 and MP4, respectively).

If setting $K_4 = K_5$, we will get

$$I_2 = I_3. \quad (9)$$

So the output reference voltage can be written as

$$V_{ref} = V_{BE3} + I_3 R_3 = V_{BE3} + \frac{R_3}{R_1} V_T. \quad (10)$$

V_{BE3} has a negative temperature coefficient while V_T has a positive one. So by carefully designing the value of R_3 and R_1, V_{ref} can be independent of temperature. Figure 4(a) shows simulation results of V_{ref} as a function of temperature. The temperature coefficient of the voltage reference is 125 ppm/℃ when temperature ranges from –20 to 60 ℃.

In the reference circuit, MN6 is applied to keep the collector voltage of Q2 stable under a large variation of the supply voltage, which will reduce the impact of the Early effect. According to Ref. [14], considering the Early effect, the collector current of Q1 is given by

$$I_1 = I_{S1}\left(1 + \frac{V_{CE1}}{V_A}\right) \exp \frac{V_{BE1}}{V_T}, \quad (11)$$

where V_{CE} is the collector–emitter voltage, and V_A is the Early voltage.

If MN6 is not used, the collector voltage of Q1 will follow the variation of the supply voltage (1.1 to 3 V in our design), which can induce a large variation of V_{CE1}. According to Eq. (11), I_1 varies a lot with the supply voltage, which will cause a large variation of V_{ref}. So to minimum this variation of V_{ref}, MN6 is adopted. The gate voltage of MN6 is relatively stable, which will make the collector voltage of Q1 stable. Thus, V_{ref} varies little with the supply voltage. Figure 4(b) shows the simulation results of V_{ref} as a function of supply voltage, line regulation is 1.7%/V when the supply voltage ranges from 1.1 to 3 V.

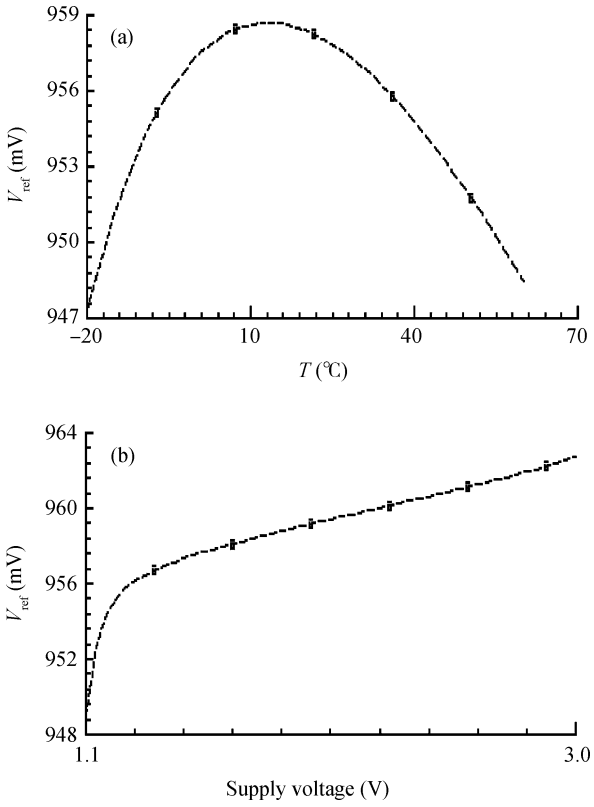

Fig. 4. V_{ref} as functions of (a) temperature and (b) supply voltage.

MN1, MN2, MN3, MP1, and MP2 form a start-up circuit without static power consumption. When the circuit is powered on, node "A" firstly becomes high to turn on MN3, which will inject pulse current through MP3 to set the circuit to the right operating point. Then node "B" turns high, which will turn on MN1. Thus, node "A" becomes low and MN3 is shut down. Simulation results show that the start-up time is less than 200 μs and current consumption of the voltage reference circuit is only 150 nA.

3.3. ASK demodulator

The proposed ASK demodulator is composed of an envelope detector, a low-pass filter, an average detector, and a comparator, as Figure 5 shows. The envelope detector is composed by a two-stage rectifier, paralleled with a resistance. The low-pass filter is used to filter out the high frequency component. In order to realize proper filter function, the RC product must satisfy the condition as Eq. (12)[15],

$$\frac{1}{f_{RF}} \ll RC \ll \frac{1}{f_{data}}, \quad (12)$$

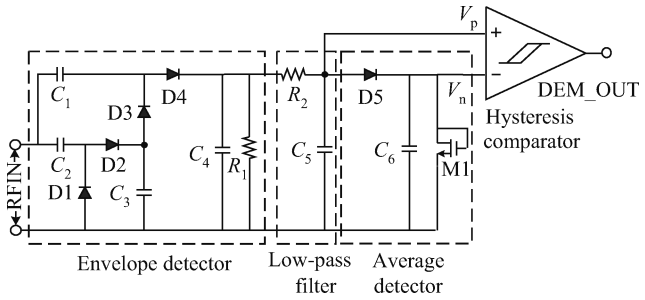

Fig. 5. ASK demodulator circuit.

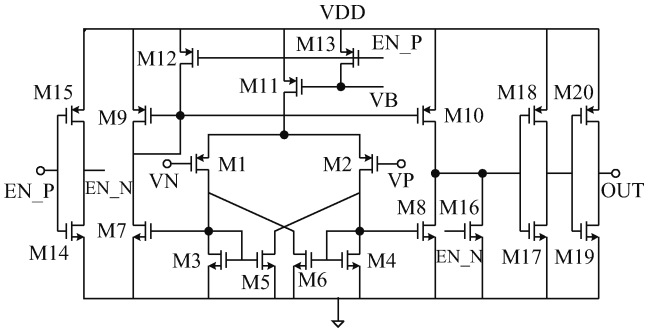

Fig. 6. Hysteresis comparator circuit.

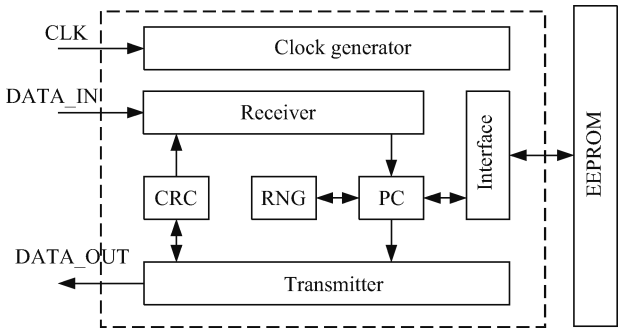

Fig. 7. Block diagram of the baseband processor.

where f_{RF} is the frequency of the carrier wave and f_{data} represents the digital data rate. The average detector slows down the fast change of V_p[16]. Finally the comparator compares V_p with V_n and sends the demodulated signal to the baseband processor.

The hysteresis comparator circuit is presented in Fig. 6. The comparator needs hysteresis to reduce the BER (bit error rate)[17]. We add an enable switch to power down the comparator when it is not used. The enable signal is generated by the baseband processor.

3.4. Baseband processor

Figure 7 illustrates the block diagram of the baseband processor. It consists of seven modules: clock generator (CG), receiver, protocol controller (PC), transmitter, random number generator (RNG), CRC, and interface. The receiver is responsible for receiving, decoding and holding incoming data. The PC mainly processes the ISO 18000-6B standard and executes actions such as reading from or writing to the EEPROM. Data exchange between the EEPROM and the PC is based on the interface module. Combined with analog circuits, a RNG module is used to generate a one-bit true random number for collision arbitration. The CRC calculates CRC-16 for forward and return links to check the data's integrality. Data transmitted to the reader is encoded to FM0 format and transmitted by the transmitter.

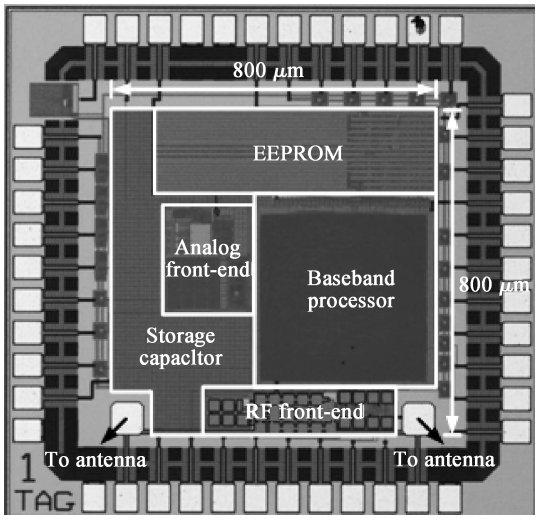

Fig. 8. Microphotograph of the tag chip.

In this paper, several low-power strategies are implemented. The clock generator module is designed to control enabling signals of other modules at system level to reduce the total power. In addition, a strategy of clock gating is used at RTL level, which enables or disables the clock of a register in a module. To further reduce power consumption and chip area, strategies like component reuse, lowering the supply voltage, and lowering the system clock frequency are adopted[18].

4. Experiment results

The whole tag is implemented in a TSMC 0.18 μm CMOS process. As shown in Fig. 8, the tag chip includes an RF/analog front-end, a baseband processor, and a 512-bit EEPROM memory. In addition, a 600 pF capacitor for power storage is integrated. The chip size is 800 μm × 800 μm. A folded dipole antenna is designed for the tag chip, as Figure 9 shows. Measurement results show that, with a 100k resistor load, the power conversion efficiency of the rectifier reaches 34.2%. Figure 10 is the measured results of the ASK demodulator, the minimum input RF signal that can be demodulated is 100 mV and the maximum input data rate is 160 kb/s. Figure 11 shows the measured results of forward link and return link communication. In the forward link, the reader sends a "WRITE" command to the tag and writes data into the EEPROM memory. Then in the return link the tag responses back to the reader, which indicates a correct writing operation. Measurement results show that at a 0.96 V supply voltage, the RF/analog front end consumes 2.25 μA current while the baseband processor consumes 2.45 μA, and the current consumption of the EEPRROM memory is about 3 μA when in reading state. The total power consumption of the tag chip is 7.4 μW with a sensitivity of –12 dBm. Comparisons of this circuit's performance with some of the latest work are listed in Table 1.

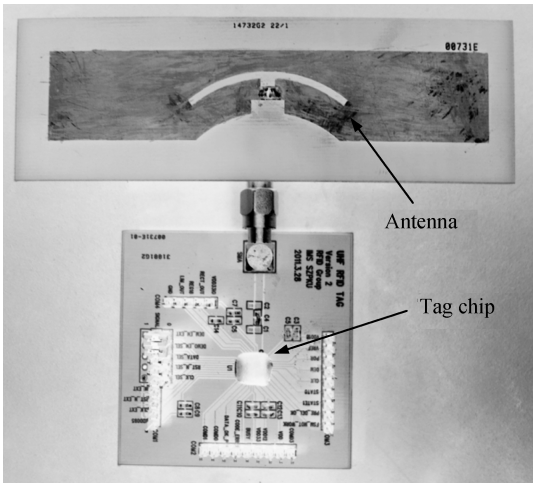

Fig. 9. Testing board of the tag chip.

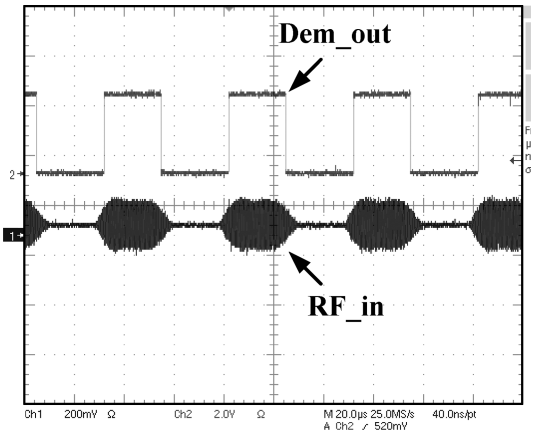

Fig. 10. Measured results of the ASK demodulator.

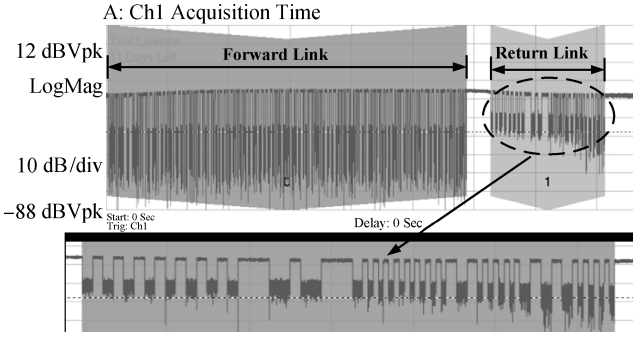

Fig. 11. Measured results of forward link and return link communication.

5. Conclusion

This paper presents a fully integrated passive UHF RFID tag chip complying with the ISO18000-6B protocol. The tag chip includes an RF/analog front-end, a baseband processor, and a 512-bit EEPROM memory. To improve power conversion efficiency, a Schottky barrier diode based rectifier is adopted. The design of a novel voltage reference circuit using the peaking current source, an ASK demodulator and a low-power baseband processor are discussed in detail. Measurement results show that the total power consumption of the tag chip is only 7.4 μW with a sensitivity of –12 dBm.

Table 1. Result comparison.

Features	This work	Ref. [19]	Ref. [20]
Process	0.18 μm	0.18 μm	0.18 μm
Standard	ISO/IEC 18000-6B	EPC Gen-2	ISO/IEC 18000-6C
Supply voltage (V)	0.96	1	1
Power consumption (μW)	7.4	15	14
Sensitivity (dBm)	–12	–11	–9.5
Chip area (μm^2)	800 × 800	1300 × 700	880 × 880

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