A RF receiver frontend for SC-UWB in a 0.18-μm CMOS process*

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Abstract: A radio frequency (RF) receiver frontend for single-carrier ultra-wideband (SC-UWB) is presented. The front end employs direct-conversion architecture, and consists of a differential low noise amplifier (LNA), a quadrature mixer, and two intermediate frequency (IF) amplifiers. The proposed LNA employs source inductively degenerated topology. First, the expression of input impedance matching bandwidth in terms of gate–source capacitance, resonant frequency and target S_{11} is given. Then, a noise figure optimization strategy under gain and power constraints is proposed, with consideration of the integrated gate inductor, the bond-wire inductance, and its variation. The LNA utilizes two stages with different resonant frequencies to acquire flat gain over the 7.1–8.1 GHz frequency band, and has two gain modes to obtain a higher receiver dynamic range. The mixer uses a double balanced Gilbert structure. The front end is fabricated in a TSMC 0.18-μm RF CMOS process and occupies an area of 1.43 mm^2. In high and low gain modes, the measured maximum conversion gain are 42 dB and 22 dB, input 1 dB compression points are -40 dBm and -20 dBm, and S_{11} is better than –18 dB and –14.5 dB. The 3 dB IF bandwidth is more than 500 MHz. The double sideband noise figure is 4.7 dB in high gain mode. The total power consumption is 65 mW from a 1.8 V supply.

Key words: radio frequency receiver front end; CMOS; low noise amplifier; inductively degenerated; single-carrier ultra-wideband

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1. Introduction

Ultra-wideband (UWB) is a high-speed short-range wireless technology applied to high-definition video data transfer, wireless USB, etc.[1]. According to the Federal Communications Commission (FCC), a signal with a fractional bandwidth greater than 20% or which occupies more than 500 MHz of spectrum can be defined as a UWB signal. The licensed frequency bands for UWB over the world generally range from 3.1 to 10.6 GHz. There exist two industrial standards for UWB technology, which are multiband orthogonal frequency division multiplexing (MB-OFDM) and direct sequence spread spectrum (DS-SS). In application, MB-OFDM system is more robust with respect to multipath effects and interferences due to its multiple band operation characteristic, while DS-SS system has advantages of lower peak-to-average power ratio (PAPR), insensitivity to carrier offset, and lower system complexity and performance specifications[2]. In China, both of the two systems are under research. A group from Tsinghua University proposed a single-carrier UWB (SC-UWB) communication system based on DS-SS scheme, which is one of the candidates of China Wireless Personal Area Network (C-WPAN) standards. In the SC-UWB system, carrier frequency is fixed to 7.656 GHz with an operation bandwidth of 528 MHz (from 7.392 to 7.920 GHz), and the intermediate frequency (IF) bandwidth is 264 MHz. The dynamic range of the receiver is from –80 dBm to –20 dBm.

This paper presents a radio frequency (RF) receiver front end for SC-UWB standard. The front end employs direct-conversion architecture, and consists of a low noise amplifier (LNA), a quadrature mixer, and two IF amplifiers, as shown in Fig. 1.

2. Circuit design

2.1. Low noise amplifier

The main challenges faced in designing a CMOS UWB LNA are wideband input impedance matching, flat gain over the frequency bands, and low noise figure at high frequency. Many different topologies for UWB LNA have been reported, such as feedback[3–5], common-gate capacitor-cross coupling[6], LC ladder[7], load tuning[8], and noise cancel-

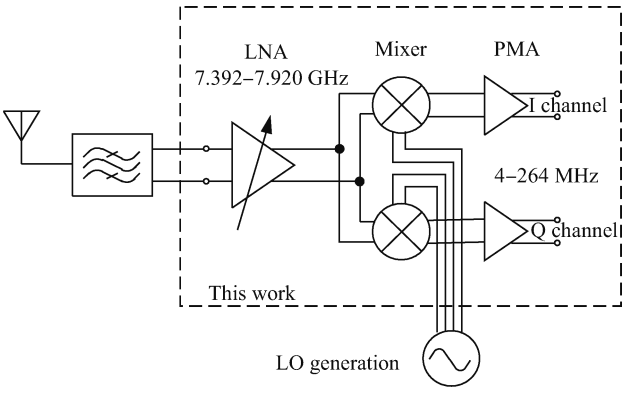

Fig. 1. Block diagram of the proposed RF receiver front end architecture.

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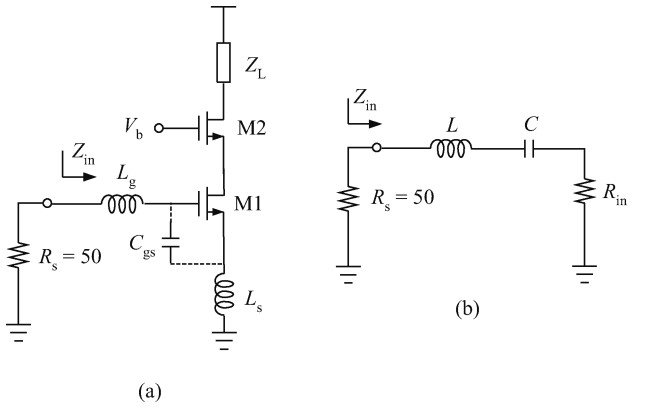

Fig. 2. (a) Topology of a single-end inductively degenerated cascode LNA. (b) Equivalent circuit of the input impedance matching network.

ing[9]. However, since the SC-UWB receiver operates over a relatively narrower frequency band of 7.392–7.920 GHz, the conventional source inductively degenerated LNA is the first choice, which exhibits a better noise figure (NF) and gain performance with lower power consumption.

2.1.1. Input impedance matching analysis

Source inductively degenerated topology has been widely used in the design of LNAs, because the source inductor provides a 50 Ω equivalent resistance for input impedance matching without introducing extra noise. However, because of the narrow-band characteristic of traditional wireless applications, explicit analysis about how much bandwidth it can provide has never been reported. Considering that the RF bandwidth of SC-UWB is 528 MHz, and could be wider if sufficient margin is left, the bandwidth capability of this structure needs to be explored first.

Figure 2(a) shows the topology of a single-end source inductively degenerated cascode LNA. It consists of a source resistance R_s of 50 Ω, gate inductor L_g, source inductor L_s, transistors M1 and M2, gate–source capacitance C_{gs}, and load impedance Z_L. Figure 2(b) shows the simplified equivalent input impedance matching network.

The equivalent input impedance can be expressed as

$$\begin{aligned} Z_{in} &= s(L_g + L_s) + \frac{1}{sC_{gs}} + \frac{g_m}{C_{gs}} L_s \\ &= sL + \frac{1}{sC} + R_{in}, \end{aligned} \tag{1}$$

where g_m is the transconductance of M1,

$$L = L_g + L_s, \quad C = C_{gs}, \quad R_{in} = \frac{g_m}{C_{gs}} L_s.$$

Then Equation (1) can be rewritten as

$$Z_{in} = jX\left(\frac{f}{f_0} - \frac{f_0}{f}\right) + R_{in}, \tag{2}$$

where f is the operation frequency, f_0 is the resonant frequency of the network, and

$$X = \sqrt{\frac{L}{C}}, \quad f_0 = \frac{1}{2\pi\sqrt{LC}}.$$

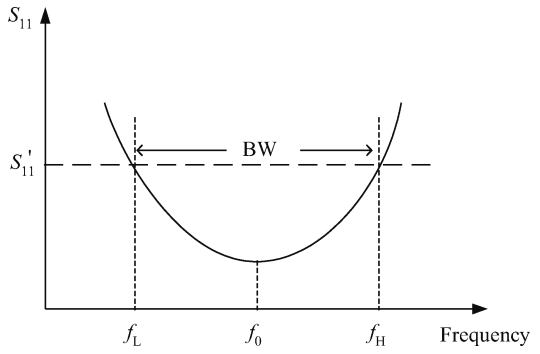

Fig. 3. Diagram of the input impedance matching bandwidth for a certain reflection coefficient, S'_{11}, and resonant frequency.

The input reflection coefficient S_{11} can be expressed as

$$\begin{aligned} S_{11} &= \left|\frac{Z_{in} - R_s}{Z_{in} + R_s}\right| \\ &= \frac{X\left(\dfrac{f}{f_0} - \dfrac{f_0}{f}\right)^2 + (R_{in} - R_s)^2}{X\left(\dfrac{f}{f_0} - \dfrac{f_0}{f}\right)^2 + (R_{in} + R_s)^2}. \end{aligned} \tag{3}$$

Suppose that the S_{11} needs to be lower than a certain value of S'_{11} between frequencies of f_L and f_H, as shown in Fig. 3, which can be expressed as

$$S_{11} \leqslant S'_{11}. \tag{4}$$

By solving Eqs. (3) and (4), it can be found

$$\begin{cases} f_L = \dfrac{-Z_0 + \sqrt{Z_0^2 + 4X^2}}{2X} f_0, \\ f_H = \dfrac{Z_0 + \sqrt{Z_0^2 + 4X^2}}{2X} f_0, \end{cases} \tag{5}$$

where

$$Z_0 = \sqrt{\frac{(R_{in} + R_s)^2 S'^2_{11} - (R_{in} - R_s)^2}{1 - S'^2_{11}}}. \tag{6}$$

The bandwidth can be expressed as

$$\mathrm{BW} = f_H - f_L = \frac{Z_0}{X} f_0. \tag{7}$$

When R_{in} is close to R_s, Equation (7) can be further written as

$$\begin{aligned} \mathrm{BW} &\approx 200\pi C f_0^2 \frac{S'_{11}}{\sqrt{1 - S'^2_{11}}} \\ &\approx 200\pi C f_0^2 S'_{11}. \end{aligned} \tag{8}$$

According to Eq. (8), the bandwidth is determined by total gate–source capacitance C, resonant frequency f_0, and target

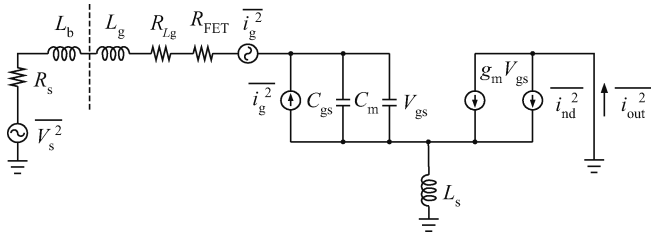

Fig. 4. Small signal model of an inductively degenerated LNA.

value of the input reflection coefficient S'_{11}. For a fixed f_0 and S'_{11}, a minimum C can be determined by BW. When the Miller effect of M1 is taken into account, C will be 30%–100% larger than C_{gs}[10]. If C_{gs} is assumed to be 60 fF and Miller-effect capacitance is estimated as 70% of C_{gs}, the total C will be 110 fF. When f_0 is 7.656 GHz, and S'_{11} is required to be –10 dB (0.316) or –15 dB (0.178), it can be calculated that the available bandwidths are 1.350 GHz and 733 MHz, respectively, which can cover the 528 MHz bandwidth.

2.1.2. Noise figure optimization

In an inductively degenerated LNA, loss of the on-chip spiral inductor can degrade the noise figure by as much as 0.5–1 dB. Thus the gate inductors are often placed off-chip. If the noise contribution of the gate inductor can be reduced, an LNA with integrated gate inductors is more attractive. Reference [11] gives a noise figure optimization method for an inductively degenerated LNA with an integrated gate inductor and bond wire inductance. It demonstrates the possibility and effectiveness of noise figure optimization under gain and power constraints. However, this method was based on numerical simulation, and is barely applicable to practical design. Reference [12] simplified the equations in Ref. [11], but they are still not clear enough. Both references focus more on theoretical analysis rather than physical explanation. So a new noise figure optimization strategy is presented here.

A typical small signal model of an inductively degenerated LNA is shown in Fig. 4. $\overline{V_s^2}$ is the thermal noise voltage of source resistance R_s; $\overline{V_g^2}$ is the thermal noise voltage generated by R_{L_g} and R_{FET}, which are parasitic resistances of gate inductor L_g and the gate polysilicon. $\overline{i_g^2}$, $\overline{i_{nd}^2}$ and $\overline{i_{out}^2}$ represent gate induced noise current, channel thermal noise current, and the total output noise current. L_b is a high-quality bond wire inductor. C_m is the equivalent capacitance due to the Miller effect, which is proportional to C_{gs}. Parasitic resistance of source inductor L_s is ignored because of its little effect on the noise figure optimization.

Since the derivation of basic noise figure expression has been detailed in precious literatures[10–12], here we just start with the primary expression in Ref. [11], except that Miller effect capacitance is added in. The noise figure can be expressed as

$$F = \frac{R}{R_S}\left[1 + \frac{\gamma}{\alpha}\frac{\omega_0^2 R(C_{gs}+C_m)^2}{g_m}\chi\right], \tag{9}$$

where

$$R = R_s + R_{L_g} + R_{FET}, \tag{10}$$

$$R_{L_g} = \frac{\omega_0 L_g}{Q_L}, \tag{11}$$

$$R_{FET} = \frac{R_\square W}{12n^2 L}, \tag{12}$$

$$\omega_0 = \frac{1}{\sqrt{L_t(C_{gs}+C_m)}}, \tag{13}$$

$$L_t = L_g + L_b + L_s, \tag{14}$$

$$C_{gs} = W\left(\frac{2}{3}LC_{ox} + C_{ov}\right), \tag{15}$$

$$C_m = (\phi - 1)C_{gs}, \tag{16}$$

$$\chi = A(1+Q_s^2) + 1 - 2|c|\sqrt{A} = AQ_s^2 + B, \tag{17}$$

$$A = \frac{\delta\alpha^2}{5\gamma}, \tag{18}$$

$$B = A + 1 - 2|c|\sqrt{A}, \tag{19}$$

$$Q_s = \frac{1}{\omega_0 R(C_{gs}+C_m)} = \frac{1}{\phi\omega_0 RC_{gs}}, \tag{20}$$

$$\alpha = \frac{1+\frac{1}{2}\rho}{(1+\rho)^2}, \tag{21}$$

$$\rho = \frac{V_{od}}{LE_{sat}}. \tag{22}$$

In the above equations, Q_L is the quality factor of the gate inductor, W and L are gate width and channel length, $R_\square$ is the sheet resistance of the gate polysilicon, n is the number of gate fingers, C_{ox} is the gate oxide capacitor, C_{ov} is the unit width gate–source overlap capacitance, ϕ is related to the Miller effect of M1, δ and γ are constant process parameters, c is the gate-and-drain noise correlation coefficient, V_{od} is the gate overdrive voltage, and E_{sat} is the saturation velocity.

When the input impedance is matched to R_s at ω_0,

$$\begin{aligned} R_s &= R_{L_g} + R_{FET} + \frac{g_m}{\phi C_{gs}}L_s \\ &= R_{L_g} + R_{FET} + \frac{\mu_{eff}\alpha}{\phi\left(\frac{2}{3}L^2 + \frac{C_{ov}}{C_{ox}}L\right)}V_{od}L_s. \end{aligned} \tag{23}$$

Based on the second-order electrical model for a CMOS transistor[13], the drain current and transconductance can be expressed as

$$I = WC_{ox}v_{sat}\frac{V_{od}^2}{V_{od}+LE_{sat}}, \tag{24}$$

$$g_m = \mu_{eff}C_{ox}\frac{W}{L}V_{od}\alpha, \tag{25}$$

where v_{sat} is the saturate velocity and $\mu_{eff} = \frac{2v_{sat}}{E_{sat}}$.

The effective transconductance of the LNA can be expressed as

$$G_{\rm m}=\frac{g_{\rm m}}{2\phi\omega_0 R_{\rm s}C_{\rm gs}}=\frac{\mu_{\rm eff}C_{\rm ox}}{2\phi\omega_0 R_{\rm s}\left(\frac{2}{3}LC_{\rm ox}+C_{\rm ov}\right)}V_{\rm od}\alpha, \quad (26)$$

When the load impedance of LNA is fixed, $G_{\rm m}$ is proportional to the voltage gain of the LNA.

Until now, relationships among all of the parameters have been presented by Eqs. (9)–(26).

Equation (9) can be further written as

$$F=\frac{R}{R_{\rm S}}+A\frac{\gamma}{\alpha}\frac{1}{g_{\rm m}R_{\rm s}}+B\frac{\gamma}{\alpha}\frac{\phi^2\omega_0^2R^2C_{\rm gs}^2}{g_{\rm m}R_{\rm s}}. \quad (27)$$

It can be found that R, $g_{\rm m}$ and $C_{\rm gs}$ are all determined by only two independent parameters of $V_{\rm od}$ and W, so the noise figure can be defined as

$$F=F(V_{\rm od},W), \quad (28)$$

under the power and gain constraints of

$$I=I(V_{\rm od},W), \quad (29)$$

$$G_{\rm m}=G_{\rm m}(V_{\rm od}). \quad (30)$$

The noise figure optimization process is actually finding certain values of $V_{\rm od}$ and W for a minimum F. Under the gain constraint, $G_{\rm m}$ and $V_{\rm od}$ are fixed according to Eq. (26), an optimum gate width W can be obtained for minimum F with a certain current consumption. While under a power constraint, Equations. (29) and (30) have to be solved to find the optimum value. However, the expressions are of high order and difficult to simplify.

In a 0.18 μm CMOS process, the typical values of the parameters are as follows: $\delta=\frac{4}{3}$, $\gamma=\frac{2}{3}$, $c=j0.395$; $E_{\rm sat}=4.7\times10^6$ V/m, $v_{\rm sat}=8.43\times10^4$ m/s, $R_{\square}=10\,\Omega$, $L=0.16$ μm (effective channel length)[11]. When $V_{\rm od}=200$ mV, it can be obtained by Eq. (14) that $\rho=0.024$ and $\alpha=0.965$. $Q_{\rm L}$ and ϕ can be estimated as 10 and 1.7, respectively. Generally the range of $g_{\rm m}$ is between 20–50 mS, $L_{\rm g}$ between 1–5 nH, and $R_{L_{\rm g}}$ between 4.8–24 Ω at 7.6 GHz. Thus it can be well assumed $g_{\rm m0}=30$ mS, $C_{\rm gs0}=60$ fF and $R_{L_{\rm g0}}=10\,\Omega$, as initial reference values. When the number of gate fingers is large enough (more than 20), $R_{\rm FET}$ could be much smaller than 1 Ω, and can be neglected compared with $R_{L_{\rm g}}$ in the optimization.

When the input impedance matching is realized, substituting typical value of each parameter in Eq. (27), it can be written as:

$$F=1+0.17\frac{1}{\frac{g_{\rm m}}{g_{\rm m0}}}+0.2\frac{R_{L_{\rm g}}}{R_{L_{\rm g0}}}+0.1\frac{\left(\frac{C_{\rm gs}}{C_{\rm gs0}}\right)^2}{\frac{g_{\rm m}}{g_{\rm m0}}}. \quad (31)$$

Larger bondwire inductance $L_{\rm b}$ allows smaller $L_{\rm g}$ and $R_{L_{\rm g}}$, thus reducing the noise figure. Generally, the value of $L_{\rm b}$ is between 0.5–2 nH in a chip package, with a variation of 10%. This variation leads to an offset of f_0 and affects input impedance matching performance.

The resonant frequency can be expressed as:

$$f_0=\frac{1}{2\pi\sqrt{L_{\rm t}(C_{\rm gs}+C_{\rm m})}}. \quad (32)$$

When the variation of $L_{\rm b}$ is $\Delta L_{\rm b}$, the offset of f_0 is

$$\begin{aligned}\Delta f_0&=\frac{1}{2\pi\sqrt{C_{\rm gs}+C_{\rm m}}}\left(\frac{1}{\sqrt{L_{\rm t}}}-\frac{1}{\sqrt{L_{\rm t}+\Delta L_{\rm b}}}\right)\\&=f_0\left(1-\frac{1}{\sqrt{1+\frac{\Delta L_{\rm b}}{L_{\rm t}}}}\right).\end{aligned} \quad (33)$$

When $\Delta L_{\rm b}\ll L_{\rm t}$, Equation (33) can be simplified as

$$\Delta f_0=f_0\frac{\Delta L_{\rm b}}{2L_{\rm t}}. \quad (34)$$

It can be derived that

$$L_{\rm b}=2\frac{\Delta f_0}{f_0}\frac{L_{\rm b}}{\Delta L_{\rm b}}L_{\rm t}. \quad (35)$$

For instance, if $\frac{\Delta f_0}{f_0}$ is limited to 2%, which is about 150 MHz at $f_0=7.6$ GHz, $\frac{\Delta L_{\rm b}}{L_{\rm b}}=10\%$, and $L_{\rm t}=4$ nH, then $L_{\rm b}$ should be no more than 1.6 nH.

Based on all of the above analysis, the gain-power consumption co-optimization procedure is proposed as follows.

Step (1): finding an initial value of $V_{\rm od}$ according to Eq. (26) to achieve the required gain ($G_{\rm m}$).

Step (2): the minimum gate width W can be obtained by the S_{11} bandwidth constraint according to Eqs. (8), (15) and (16), meanwhile $g_{\rm m}$ can be obtained by Eq. (25).

Step (3): $L_{\rm s}$, $L_{\rm g}$ and $L_{\rm b}$ are determined by Eqs. (13)–(16), and (23). Now, an initial F with minimum power consumption is obtained under a constant gain constraint.

Step (4): then, by increasing gate width, W, the value of $C_{\rm gs}$ and $g_{\rm m}$ becomes larger with a constant value of $\frac{g_{\rm m}}{C_{\rm gs}}$. The increase of $g_{\rm m}$ in the second term of Eq. (31) will improve the noise figure, while the noise contributed by $C_{\rm gs}$ in the last term increases. Moreover, according to Eqs. (13)–(16) and (23), $L_{\rm g}$ should be reduced to keep the resonant frequency constant, so $R_{L\rm g}$ becomes smaller and provides less noise; $L_{\rm s}$ should be increased a little to compensate the resistance reduction of $L_{\rm g}$.

In the above steps, there are two cases to discuss.

Case 1: with the increasing of W, $C_{\rm gs}$ in the fourth term of Eq. (31) begins to take effect, thus the noise figure will decrease to a minimum value point and then start to increase. Therefore, the $W_{\rm opt}$ can be obtained.

Case 2: with the increase of W, it is also probable that the required maximum current $I_{\rm max}$ has been reached before $W_{\rm opt}$ turns up, where the W corresponding to the $I_{\rm max}$ gives a minimum F under gain and power constraints.

Besides, the minimum noise figure is mainly determined by the value of $V_{\rm od}$. Each $V_{\rm od}$ corresponds to an optimized minimum noise figure. Hence if a lower noise figure is required, a higher $V_{\rm od}$ is needed.

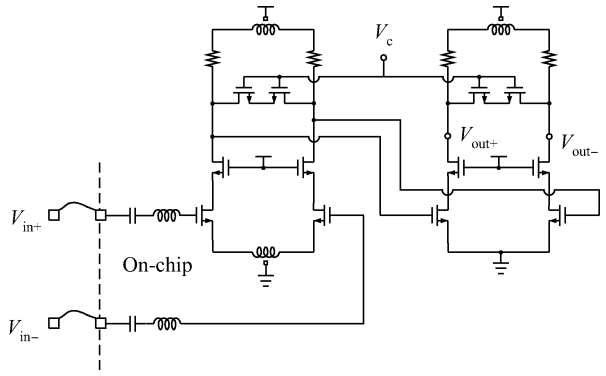

Fig. 5. Schematic of the proposed LNA.

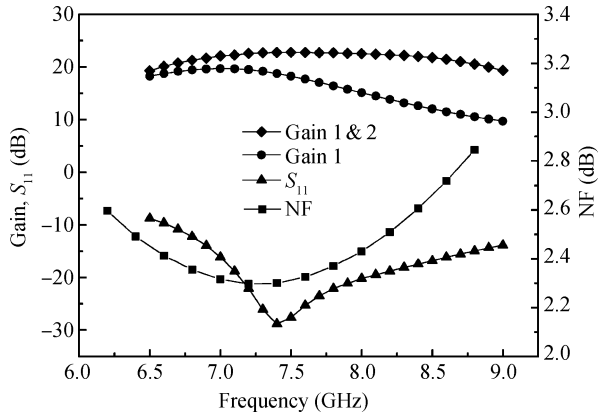

Fig. 6. Simulated gain, S_{11} and NF of the LNA. "Gain 1" and "Gain 1 & 2" represent the gain of the first stage and the total gain, respectively.

2.1.3. LNA circuit design

The proposed differential LNA shown in Fig. 5 is designed based on the new optimization strategy. The SC-UWB frequency band from 7.392 to 7.920 GHz is expanded to 7.1–8.1 GHz in the design for some margin. The parameter values of the input stage are optimized as follows:

$V_{od} = 260$ mV, $W = 80$ μm, $g_m = 33$ mS, $I = 5.9$ mA (single end), $C_{gs} = 70$ fF, $L_g = 1.3$ nH, $L_b = 1.2$ nH, $L_s = 1$ nH.

A second stage is used to provide higher and flat gain over the operation band, which consumes a DC current of 4.8 mA. The gain is variable by changing load impedances of the two stages to improve the receiver dynamic range. The simulated performance of LNA is shown in Fig. 6.

2.2. Mixer and IF amplifier

The quadrature down-conversion mixer is based on double balanced Gilbert topology, as shown in Fig. 7. The IF bandwidth is 264 MHz. Noise figure, gain and linearity performance are optimized by choosing an optimum bias current and gate size for the switch transistors[13]. The load resistance is 280 Ω, which provides a relatively small gain and allows a larger IF bandwidth. The mixer achieves a conversion gain of 2 dB and consumes a DC current of 6 mA.

Two post mixer amplifiers in the I/Q path are designed to

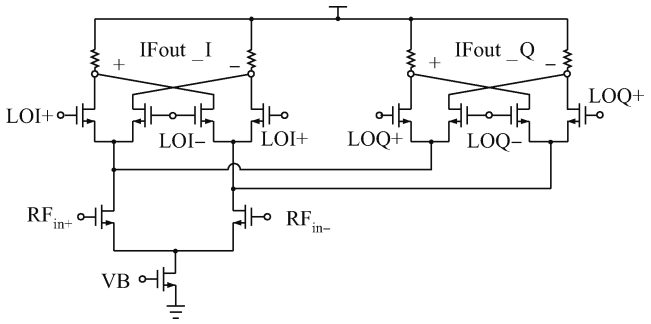

Fig. 7. Schematic of an active double-balanced quadrature Gilbert mixer.

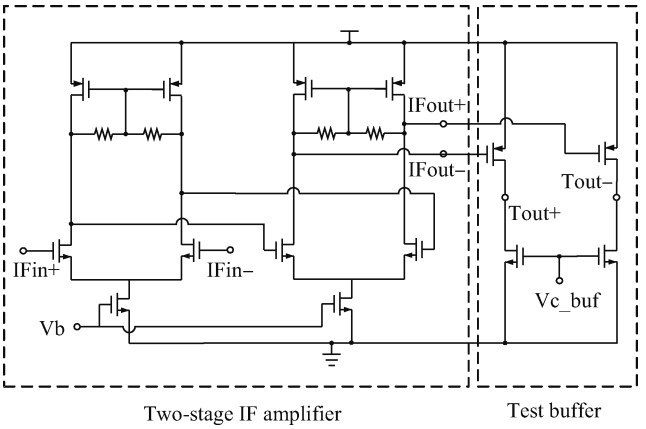

Fig. 8. Schematic of a post-mixer amplifier.

provide more gain for the receiver. It also sets the DC bias voltage of 900 mV for the succeeding low pass filter (LPF). As the IF bandwidth is much wider, the amplifier employs a two-stage structure, which is able to achieve a larger gain-bandwidth-product. The bias and gain of each stage are optimized to achieve best IIP3. A test buffer is also designed which can be shut down by the control voltage of "Vc_buf". The amplifier provides 20 dB gain with a DC current of 11.2 mA. The schematic of a baseband amplifier is shown in Fig. 8.

3. Implementation and measurement results

The RF receiver front end was fabricated in a TSMC 0.18-μm RF CMOS process. The chip area is 1.43 mm^2 including all bonding pads. The micrograph of the front-end chip and testing printed circuit board (PCB) are shown in Fig. 9. A passive balun on the PCB is designed for measurements, which exhibits an insertion loss of 1.1 dB. The LO signal is generated by an integrated frequency synthesizer. The test equipment includes an Agilent S-parameter network analyzer 8720ES, a spectrum analyzer E4440A, an RF signal generator E4438C, a noise figure analyzer N8975A, and an N4002A noise source.

Figure 10 shows measured conversion gains versus frequency in high gain mode. The peak conversion gains are 42 dB and 22 dB in high and low gain modes, and the 3 dB IF bandwidth is more than 500 MHz. The test buffer of the PMA introduces a loss of 5 dB by simulation, which is calculated in during the conversion gain measurement.

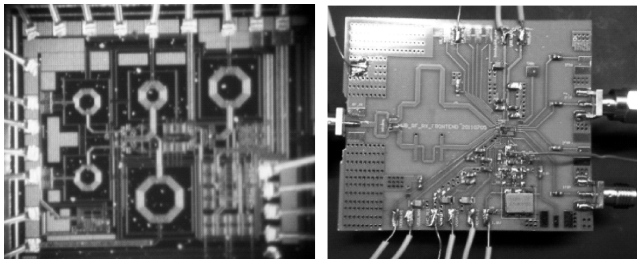

Fig. 9. Micrograph of the front end and the testing PCB.

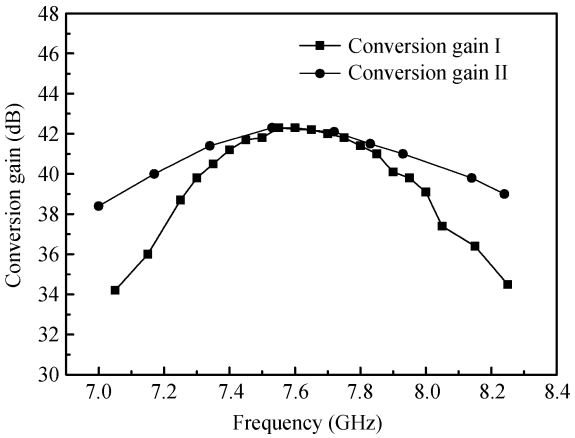

Fig. 10. Measured conversion gain of the receiver front end in high gain mode. "Gain I" is measured by sweeping RF frequency with a fixed LO frequency at 7.656 GHz; "Gain II" is measured by sweeping RF and LO frequency simultaneously with a fixed intermediate frequency of 50 MHz.

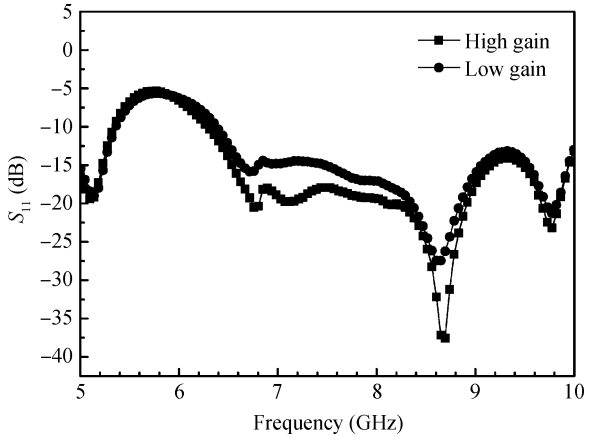

Fig. 11. Measured S_{11} for the LNA.

The measured S_{11} in high and low gain modes are better than –18 dB and –14.5 dB, respectively, as shown in Fig. 11. The measured double sideband (DSB) noise figure in high gain mode is about 4.7 dB after compensation of the balun loss, as shown in Fig. 12. The measured input 1 dB compression points in high and low gain modes are −40 and –20 dBm, as shown in Fig. 13. The input third-order intercept points (IIP3) of the front end are measured by two-tone test, which are –28 dBm and −6.7 dBm in high and low gain modes. The total power consumption is 65 mW under a 1.8 V supply. Table 1 summarizes all the measured performances of the RF receiver front end in contrast with other published literatures.

Table 1. The front-end performance summary.

Parameter	This work	Ref. [14]	Ref. [8]
RF band (GHz)	7.1–8.1	3–5	7.3–7.9
Gain (dB)	42/22	25.5	20
DSB NF (dB)*	4.7	5	5
S_{11} (dB)	–18/–14.5	–13	/
P_{1dB} (dBm)	–40/–20	/	/
IIP3 (dBm)	–28/–6.7	–4.3	–5.6
Power (mW)	65	18	45
Supply voltage (V)	1.8	1.8	2.3
Area (mm^2)	1.43	1.31	0.35
Technology (CMOS)	0.18 μ m	0.18 μ m	0.18 μ m

* High gain mode.

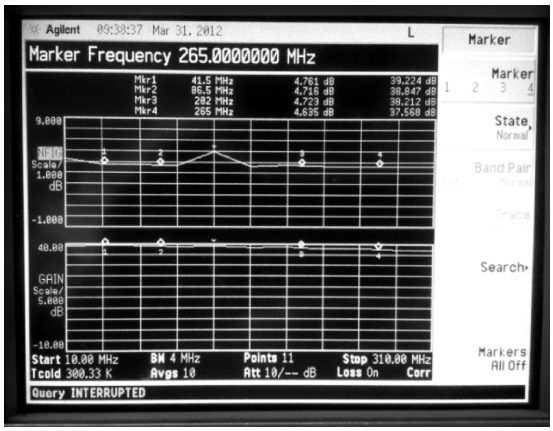

Fig. 12. Measured DSB noise figure of the front end with LO frequency at 7.656 GHz.

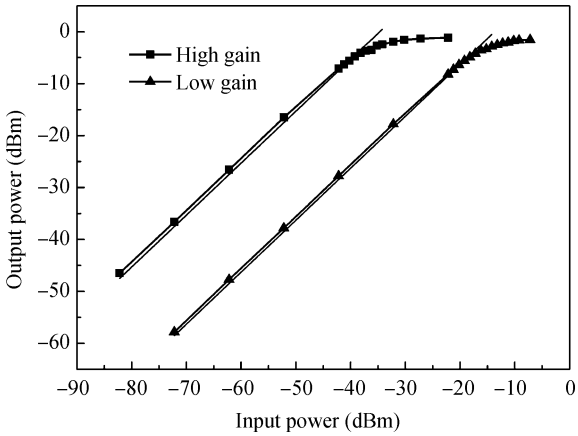

Fig. 13. Measured input 1 dB compression point in high and low gain modes with LO frequency at 7.656 GHz and intermediate frequency of 50 MHz.

4. Conclusion

In this paper, an RF receiver front end for SC-UWB is presented. The front end employs direct-conversion architecture, and consists of an LNA, a quadrature mixer, and two IF amplifiers. The proposed LNA employs source inductively de-

generated topology. An explicit expression of input impedance matching bandwidth in terms of gate–source capacitance, resonant frequency and target S_{11} is given. Then, a noise figure optimization strategy under gain and power constraints is proposed, with consideration of integrated gate inductor, bondwire inductance and its variation. The LNA utilizes two amplifying stages with different resonant frequencies to acquire gain flatness over 7.1–8.1 GHz frequency band, and has two gain modes to obtain a higher dynamic range. The mixer uses a double balanced Gilbert structure. The front end is fabricated in TSMC 0.18-μm RF CMOS process and occupies an area of 1.43 mm^2. The measured maximum conversion gains are 42 dB and 22 dB in high and low gain modes; the input 1 dB compression points are −40 dBm and –20 dBm, and S_{11} is better than –18 dB and –14.5 dB, respectively. The 3 dB IF bandwidth is more than 500 MHz. The double sideband noise figure is 4.7 dB in high gain mode. The total power consumption is 65 mW from a 1.8 V supply.

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