Design of a dual-channel multi-mode GNSS receiver with a ΣΔ fractional-*N* synthesizer

Long Qiang(龙强)[1,†], Zhuang Yiqi(庄奕琪)[1], Yin Yue(阴玥)[1], Li Le(李乐)[2], Wang Jin(王晋)[2], Li Zhenrong(李振荣)[1], Liu Qiankun(刘乾坤)[2], and Wang Lei(王磊)[2]

[1]National Key Laboratory of Wide Band-Gap Semiconductor Technology, School of Microelectronics, Xi'dian University, Xi'an 710071, China
[2]China Key System, CETC, Wuxi 214072, China

Abstract: A 72 mW highly integrated dual-channel multimode GNSS (global navigation satellite system) receiver with a ΣΔ fractional-*N* synthesizer which covers GPS L1 and the Compass B1/B2/B3 band is presented. This chip was fabricated in a TSMC CMOS 0.18 μm process and packaged in a 48-pin 3 × 3 mm^2 land grid array chip scale package. This work achieves NF $\leqslant$ 5.3 dB without an external LNA, channel gain = 105 dB for channel one (Compass B2 and B3 band), and channel gain = 110 dB for channel two (GPS L1 and Compass B1 band). Image rejection (IMRR) = 36 dB, phase noise is –115.9 dBc @ 1 MHz and –108.9 dBc @ 1 MHz offset from the carrier for the two channels separately. At the low power consumption, multibands of GNSS are compatible in one chip, which is easy for consumers to use, when two different navigation signals are received simultaneously.

Key words: compass; G_m–C filter; ΣΔ fractional-*N* synthesizer; LNA; GNSS
DOI: 10.1088/1674-4926/33/11/115005 **EEACC:** 2570

1. Introduction

A global navigation satellite system (GNSS) is an important spatial information infrastructure and Russia, Europe, and China are developing their own satellite navigation systems. In future, there is bound to more than one navigation standard in parallel[1,2]. At present, many works have studied GPS solutions[3–5], and some research concentrates on the integration of Bluetooth, WCDMA, and Galileo, which support no more than four modes. This work demonstrates a nine-mode GNSS receiver, which covers GPS and Compass bands. In different environments, nine modes of this chip can work at one mode or two modes simultaneously. When two channels work simultaneously, the maximum power consumption is 72 mW.

Satellites are often obscured due to signal impairments, so the more satellites (from different systems) there are the better. From a user's point of view this means a faster time to first fix and better tracking under hard conditions (urban canyons, indoor etc). Based on this requirement, dual-channel multimode navigation chips will become the new darling of the market for the current market situation. This paper presents a dual-channel multimode GNSS receiver with a ΣΔ fractional-*N* synthesizer, which improves the compatibility of the GNSS receiver and is easy for customers to use.

This ΣΔ fractional-*N* synthesizer has better phase noise, faster switching speed, wider coverage, and has fine resolution frequency steps, which is unachievable in integer-*N* synthesizers. Also, a multi-stage noise shaping (MASH) 1-1-1ΣΔ modulator with dither technology is adopted, which flattens the spurs of the synthesizer. In order to achieve multimode compatibility, a programmed RFA (radio frequency amplifier) is optimized, which covers different GPS and Compass bands, and has a large dynamic range. For the purpose of low current dissipation, a novel quadrature I/Q mixer is adopted, so the power consumption of the mixer is cut down by 50%. The other blocks such as: the G_m–C filter, the AGC and, the ADC are also presented in this paper. In this dual-channel multimode GNSS receiver, the interference between these two channels and different blocks are a serious problem, this work makes careful frequency plans and a layer of NT_N in the layout is adopted for good isolation.

2. GNSS receiver architecture

A block diagram of the dual-channel multimode GNSS receiver with a ΣΔ fractional-*N* synthesizer[6,7] is shown in Fig. 1.

This receiver has two channels: one channel works at 1.57542 GHz (GPS L1 band) and 1.561098 GHz (Compass B1 band); the other channel works at 1.20714 GHz (Compass B2 band) and 1.26852 GHz (Compass B3 band). It can work at nine modes, which greatly improves the receiver's compatibility and lowers the current dissipation, the work mode is shown in Table 1.

The GPS signal code is a direct-sequence spread spectrum (DSSS) and binary phase-shift keying (BPSK) modulation is adopted. The thermal noise power (KTB) is –114 dBm/MHz and associated signal-to-noise ratio (SNR) at the antenna is –19 dB, so the minimum received signal at the antenna port is about –133 dBm for L1 band. So for the 4 MHz bandwidth of the GPS signal, which lies at the middle of the 20 MHz GPS channel[8–10], the noise floor is –108 dBm. Considering the system requirements, a low-IF architecture with image rejection has been selected in channel two, which relaxes the constraints on the external RF filter and reduces the noise figure

† Corresponding author. Email: Plike8846@163.com
Received 15 April 2012, revised manuscript received 3 June 2012

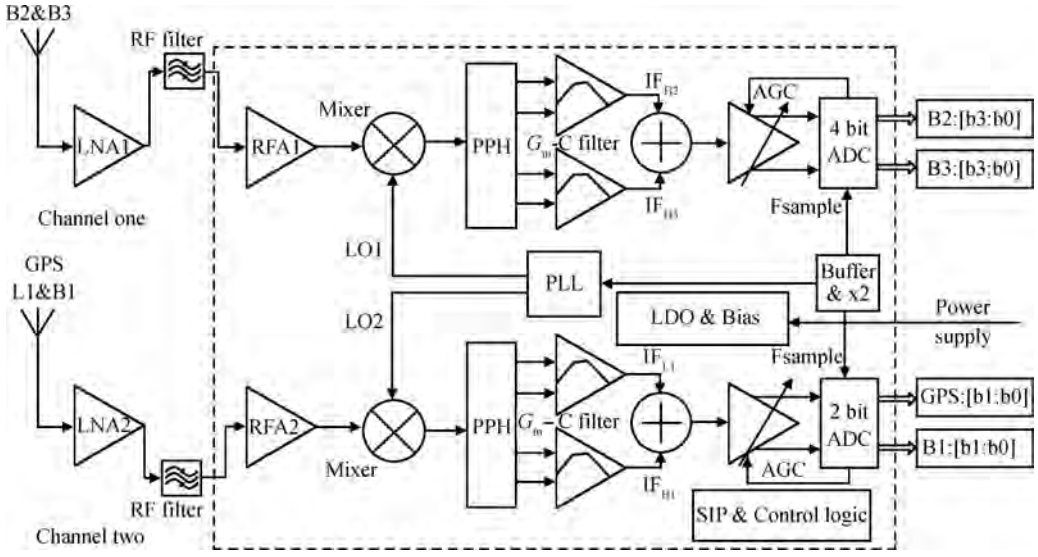

Fig. 1. Block diagram of the dual-channel multimode GNSS receiver.

Table 1. Work mode.

Mode number	Work band				Note
	L1	B1	B2	B3	
1	▲				
2		▲			
3			▲		
4				▲	
5	▲		▲		
6	▲			▲	
7		▲	▲		
8		▲		▲	
Standby mode					PLL work only

(NF) of the receiver. In channel two, a programmed RF amplifier (RFA), an I/Q down-conversion mixer, a low pass filter, a automatic gain control (AGC), a 2-bit ADC, and a ΣΔ fractional-N synthesizer with LC-VCO are integrated. The IF frequency is selected as $4f_0$ (where $f_0 = 1.023$ MHz) for image rejection relaxing, the analog-to-digital converter (ADC) sampling frequency ($16f_0$) and main system clock ($48f_0$) for the digital baseband processor are carefully selected[2].

In channel one, the IF filter and ADC are substituted by a G_m–C filter and a 4-bit ADC, a high IF (46 MHz) is selected, which improve the image rejection ratio and the sensitivity of the receiver. A 62 MHz ring oscillator is also integrated in the chip, which provides the sample clock for the ADC. The reference clocks of the ΣΔ fractional-N synthesizer and 62 MHz ring oscillator are selectable from 10 to 50 MHz.

3. Circuit implementation

3.1. RFA and mixer

To achieve a wide dynamic range and guarantee high sensitivity of the receiver, the LNA and mixer must have a low noise figure and high linearity. The circuit-level description of the RFA and mixer are shown in Fig. 2.

The gain and resonant frequency of the RFA are programmed, which employs a common-source common-gate (CS/CG) structure with a source degeneration inductor[11]. The degeneration inductor is substituted by a bond-wire which saves chip area. The transistor M1 and the degeneration inductor generate real term impedance equal to

$$Z_{\text{in}} = \frac{g_{\text{m}}}{C_{\text{gs}}} L_{\text{s}}, \tag{1}$$

which complicates the task of noise matching and impedance matching. The cascade structure reduces the Miller effect, improves the reverse isolation, and increases stability.

Two dominant noise sources in the MOS device are channel current thermal noise and induced gate thermal noise, which are given by Eqs. (2) and (3) separately.

$$\frac{\overline{i_{\text{d}}^2}}{f} = 4kT\gamma g_{\text{d0}}, \tag{2}$$

$$\frac{\overline{i_{\text{g}}^2}}{f} = 4kT\delta g_{\text{g}}, \tag{3}$$

where g_{d0} is the device zero-bias drain conductance, and γ and δ are coefficients describing the magnitude of the noise power[12]. Transistor M1 is the dominant noise source and M3 contributes noise power as well, in this design we merge the drains of M1 and the sources M3 together, the width of M1 and M3 are equal.

A 3-bit LC-tank with a capacitor bank[2] as the RFA load maximizes the gain of the RFA at the bands of L1, B1, B2, and B3 separately, this achieves the compatibility of different GNSS modes. At the node of E, the current of M1 is bypassed to ground by transistor M2, and the RFA achieves 0 dB gain, which enlarges the dynamic range of the receiver.

An I/Q active pseudo-differential Gilbert mixer is AC coupled to the RFA[13, 14]. It converts RF signal to IF signal. In conventional receiver design, two Gilbert mixers are often used, so the area and current dissipation of the mixer is large. These two mixers perform quadrature mixing, they have the same RF input and LO input, but this will cause amplitude and phase mismatch in the I and Q channels, which degrades the

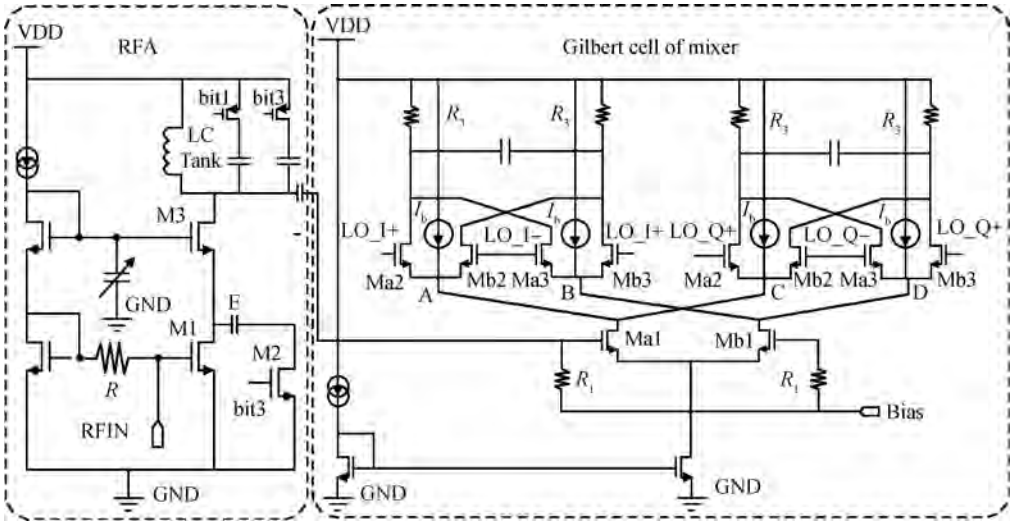

Fig. 2. Schematic of the proposed RFA and mixer.

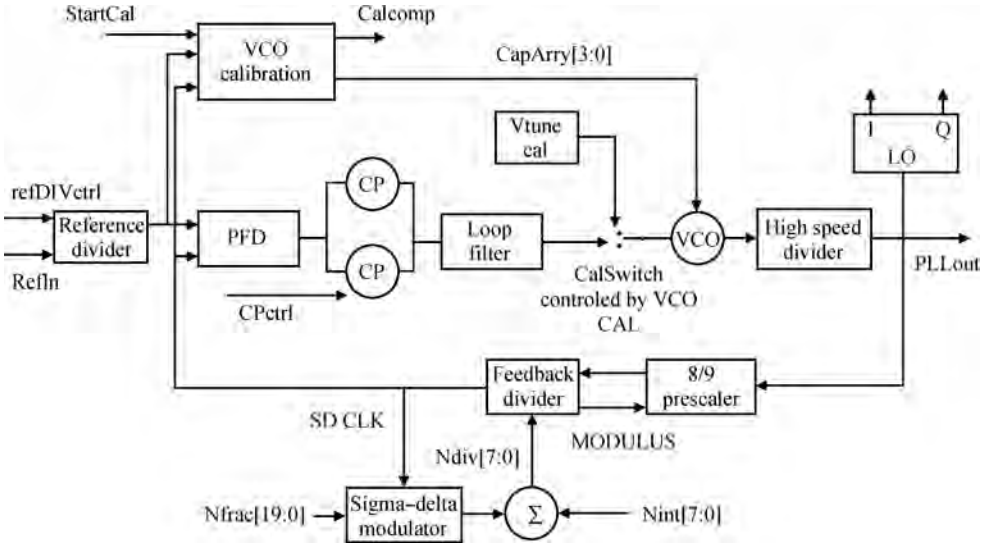

Fig. 3. Structure of the ΣΔ fractional-N synthesizer.

SNR of the receiver. In this work we merged two mixers together, which saved current dissipation and mixer area. The schematic of the mixer is shown in Fig. 2. The I/Q path of the mixer has a common G_m stage; the switching pair are driven by a pair of quadrature LO signals with a 50% duty-cycle. At the A, B, C and D nodes, a current source draws current from the G_m stage[2], for high gain, this structure minimizes the current flow to the load to maximize R_L, and we can maximize the bias current for RF devices to minimize the noise contribution of the G_m stage.

Given the same power consumption, this mixer has advantages of high conversion gain, low noise figure, low power dissipation, and the same linearity compared to a conventional Gilbert mixer. At the end of the mixer, a poly phase (PPH) follows, the structure of the PPH is shown in Ref. [5]. By careful design, the RFA block and mixer draws 4 mA current from the power supply and achieves a 4 dB noise figure and 30 dB conversion gain.

3.2. ΣΔ fractional-N synthesizer

In this paper, two ΣΔ fractional-N synthesizers are integrated in the receiver. The synthesizer generates a quadrature local oscillator (LO) for a quadrature Gilbert mixer. The structure of the ΣΔ fractional-N synthesizer is shown in Fig. 3.

For an integer-N synthesizer, the frequency step size is limited by the crystal oscillator frequency. Only integer multiples of the crystal frequency can be generated. A fractional-N synthesizer will always provide a better phase noise performance since a lower value of N can be used as compared to an integer-N synthesizer. It combines a high reference frequency with fine-resolution frequency steps, which is unachievable in integer-N synthesizers. Its major shortcoming is the generation of fractional spurs. The tradeoff is that the fractional-N synthesizer is more complex and there are fractional reference spurs to deal with instead of just the integer reference spurs. But for low phase noise and high switching speed, fractional-

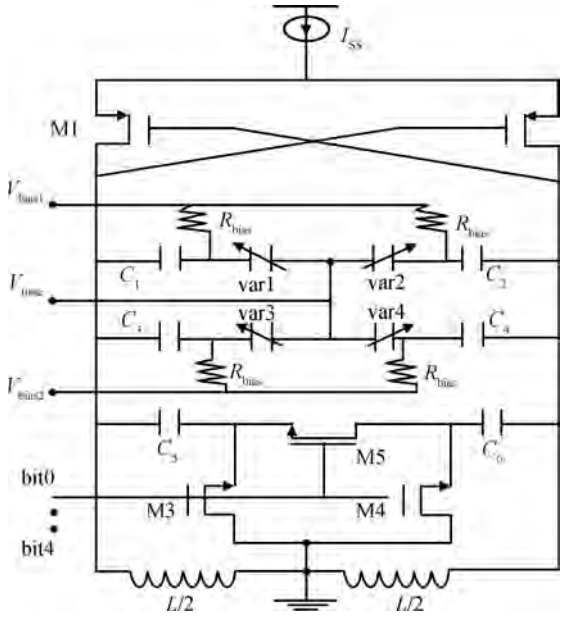

Fig. 4. Structure of a VCO with a dual-varactor stage.

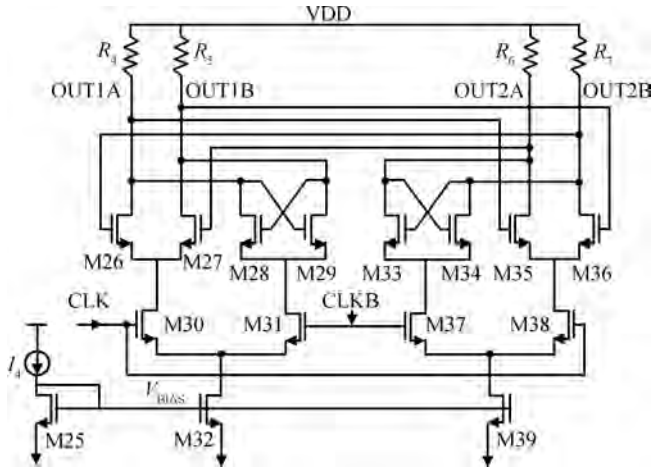

Fig. 5. Structure of the high frequency divider by 2.

N synthesizers are the way to go.

This work includes a phase frequency detector (PFD), a charge pump (CP), a voltage-controlled oscillator (VCO), a loop filter (LF), a high speed divider, an 8/9 prescaler, and a reference divider[6, 7]. The VCO and the divider are two important blocks in the synthesizer, the structure of the VCO and the divider-by-two are shown in Figs. 4 and 5.

In this design, a VCO with dual stages of accumulation mode varactors is presented. It combine digital and analog tuning in the VCO core with some sub-bands, which widen the cover range[15], and provide superior phase noise (PN) and tuning linearity. Thus, the VCO can cover GPS L1, Compass B1, B2 and B3 bands. The continuous tuning is implemented by MOS varactors and the discrete sub-band is chosen by a capacitive switch bank with several coarse tuning bits, which are generated in the PLL (phase locked loop) calibration procedure.

To satisfy the high speed and low consumption requirements, the 1/2 frequency divider employs a source-coupled logic (SCL) structure[16], as shown in Fig. 5. This fully differential frequency divider consists of two identical latches which cross-couple each other. Each latch consists of two sense devices (M30 and M31 in the master and M37 and M38 in the slave), an NMOS cross-coupled pair (M28 and M29 in the master and M33 and M34 in the slave) for the latch, two loading resistors (R_4 and R_5 in the master and R_6 and R_7 in the slave), and two NMOS driven transistors (M26 and M27 in the master and M35 and M36 in the slave). When CLK goes high, the cross-coupled pair of the slave D-flip–flop holds the OUT2A and OUT2B outputs; when CLK goes low, the cross-coupled pair of master flip–flop holds the OUT1A and OUT1B outputs.

In this $\Sigma\Delta$ fractional-N synthesizer, a multi-stage noise shaping (MASH) 1-1-1$\Sigma\Delta$ modulator with dither technology was adopted to smooth the spurs, the 3rd-order sigma–delta modulator is cascaded by three 1st-order sigma–delta modulators. The input to the modulator is a 20-bit fractional signal and an 8-bit integer signal. The MASH modulator produces an 8bit output to control the multi-modulus divider. With this structure, the spurs are flattened and modulated noise at high frequency is filtered by the synthesizer LF (loop filter)[4, 16].

3.3. IF filter

Two different IF filters are integrated in this dual-channel multimode GNSS receiver. In channel two, for the GPS L1 band and the Compass B1 band, a 6th-order Chebyshev RC-active filter is adopted. At low frequency, it provides high linearity and a large dynamic range. The bandwidth of this filter is from 2 to 7 MHz with an active gain of 13 to 16 dB. The current dissipation is 700 μA[4, 10].

In channel one for Compass B2 and B3 bands, an 8th-order tunable G_m–C band-pass filter is adopted, the structure of this filter is shown in Fig. 6. This 8th-order filter is constructed by four-stage cascaded biquad sections[17, 18]. To minimize the differences of parameter shifts between biquad stages, each section has different f_0, Q value, and bandwidth.

The structure of the G_m–C biquad band-pass filter is shown in Fig. 6. G_{m1} transfers the voltage to current, G_{m3}, G_{m4} and C_2 compose a symmetrical floating gyrator inductor, the negative output of G_{m2} was connected back to its positive input, which represents a resistor. A g_m-based resistor and a symmetrical floating gyrator inductor are shown in Fig. 7. The tuning control bits control the capacitor bank of C_1 and C_2 to adjust the Q and f_0 of the G_m–C biquad band-pass filter[19, 20].

This proposed 8th-order tunable G_m–C band-pass filter achieves a 46 MHz band-pass filter for the Compass B2 and B3 bands, the –3 dB bandwidth is 21 MHz, gain is 10 dB, and current dissipation is 3 mA.

3.4. AGC and ADC

The automatic gain control (AGC)[21] has a wide dynamic range from –2 to 52 dB with a gain step of 1.7 dB for GPS L1 and Compass B1 bands, furthermore the AGC has a dynamic range from 6 to 58 dB with 32 steps for channel one. These two AGCs are cascaded with five amplifiers stages; each stage has a high gain and a low gain, which achieves a wide dynamic range for the receiver.

The ADC is the interface between an analog signal and a digital signal, it contains sample, hold, equalization and encode

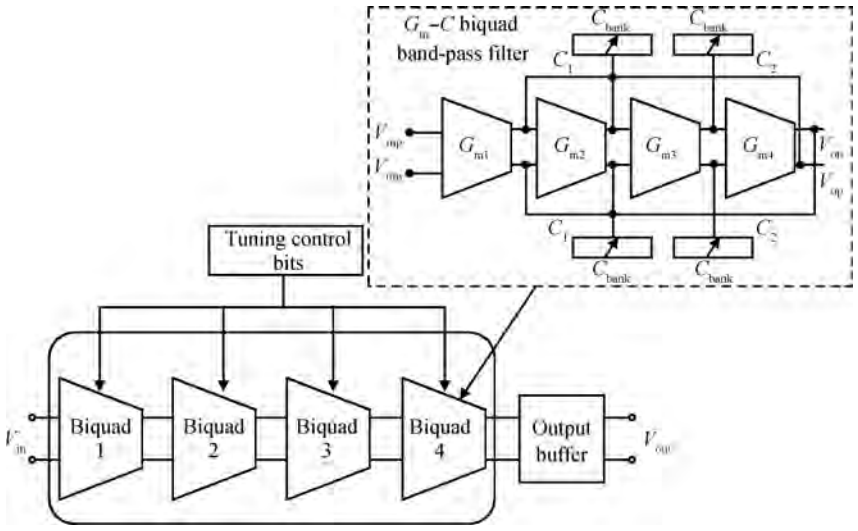

Fig. 6. 8th-order tunable G_m–C band-pass filter.

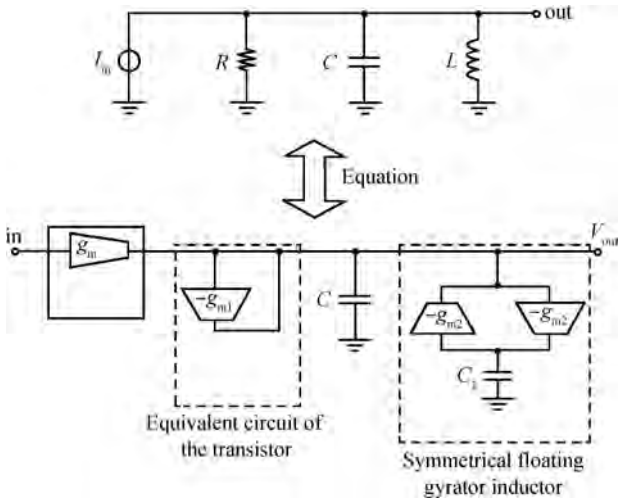

Fig. 7. The G_m–C biquad band-pass filter model.

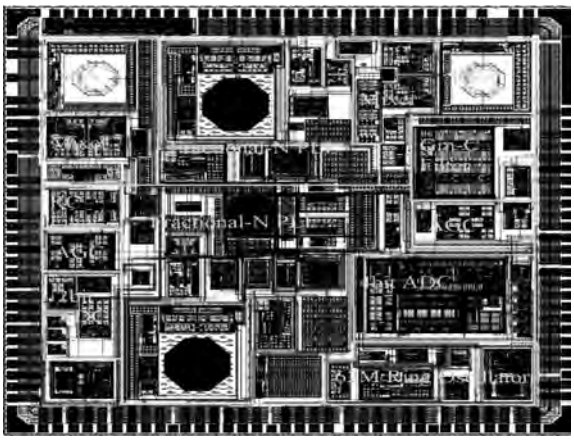

Fig. 8. Layout of the dual-channel multi-mode GNSS receiver.

blocks. In this work, a 4-bit flash ADC is adopted for Compass B2 and B3 bands, but for the GPS L1 and Compass B1 bands, a 2-bit ADC is used. In channel two for GPS L1 and Compass B1 bands, the ADC provides a 2-bit output code as sign (Sig) and magnitude (Mag) bits[4, 22]. In channel one for Compass B2 and B3 bands, the AGC amplifier output drives a 4-bit A/D converter[23] whose input signal is 2 MHz. The sample frequency is 62 MHz, which is provided by a ring oscillator.

4. Experimental results

This work was fabricated in a TSMC 0.18 μm CMOS process, the layout of this chip is shown in Fig. 8. The chip occupies an area of 3×3 mm^2 and draws 40 mA current from the power supply when the two channel work simultaneously.

The chip is measured by using an Agilent MXA signal analyzer N9020A and a PSG vector signal generator E8267D. The experimental results are shown in Table 2.

The NF is measured by using the gain method, the NF can be expressed in Eq. (4).

$$\mathrm{NF} = 174 + \mathrm{PWD} + G - \mathrm{INL}. \tag{4}$$

The power spectrum density (PWD), the gain of the channel (G), and the insert loss (INL) is minused from the noise floor (–174 dBm).

The noise figures are 3.6 dB, 5.3 dB, 5.1 dB, 4.9 dB separately for GPS L1, Compass B1, B2 and B3 bands without an extra external LNA. The measured phase noise performance is shown in Figs. 9 and 10. The phase noise is –115.9 dBc and –108.9 dBc at 1 MHz offset from the carrier frequency.

The signal spectrums of the AGC output for channels one and two are shown in Figs. 11 and 12. The IF bandwidth of this receiver for channel one is 21 MHz at 46 M IF and 4 MHz at 4 M IF for channel two. The bandwidth satisfies the dual-channel multimode GNSS receiver requirement.

After careful frequency planning and layout design, the interferences in this chip are largely reduced, with an external LNA, the noise figure and phase noise are lower than some presented works. When GPS and Compass signals are received simultaneously, there is no interference, 9 GPS satellites and 6 Compass satellites are visible.

In Table 3, the proposed GNSS receiver is compared

Table 2. Experiment results of the receiver.

Parameter	Unit	Channel 2		Channel 1	
		B1	L1	B2	B3
RF frequency	MHz	1561.098	1575.42	1207	1268
LO frequency	MHz	1557.006	1571.328	1161	1222
IF	MHz	4.092	4.092	46	46
Channel gain	dB	103	100	105	105
IF BW	MHz	4	4	21	21
NF	dB	5.3	3.6	5.1	4.9
PN @ 100 Hz	dBc	–72.63	–72.63	–70.9	–70.9
PN @1 kHz	dBc	–75.82	–75.82	–83.53	–83.53
PN @ 10 kHz	dBc	–80.26	–80.26	–83.96	–83.96
PN @ 100 kHz	dBc	–80	–80	–84.19	–84.19
PN @ 1 MHz	dBc	–115.9	–115.9	–108.9	–108.9
Current	mA	40	40	40	40

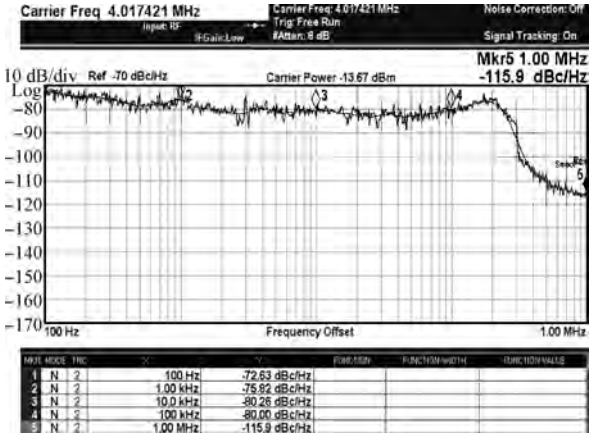

Fig. 9. Measured GPS L1 and BD B1 band phase noise of the VCO. The phase noise at 1 kHz, 10 kHz, 100 kHz, and 1 MHz frequency offsets are –75.82, –80.26, –80, –115.9 dBc/Hz, respectively.

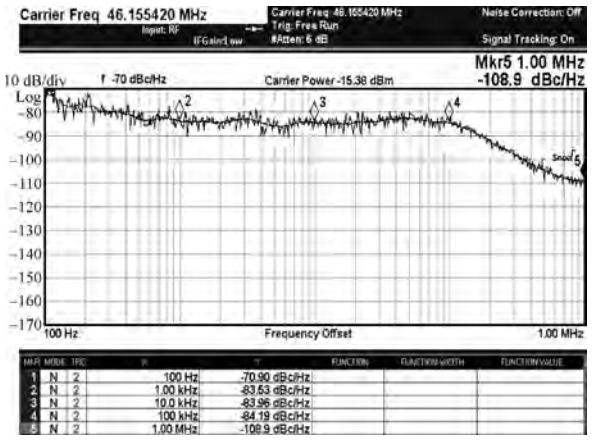

Fig. 10. Measured BD B2 and B3 band phase noise of the VCO. The phase noise at 1 kHz, 10 kHz, 100 kHz and 1 MHz frequency offsets are –83.53, –83.96, –84.19, –108.9 dBc/Hz, respectively.

with some multi-band and multi-mode receivers. It can be seen that this work occupies less die area and has less power consumption.

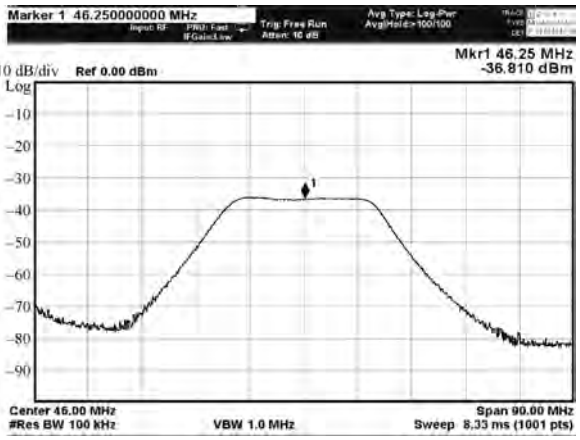

Fig. 11. Signal spectrum of the AGC output for Compass B2 and B3 band.

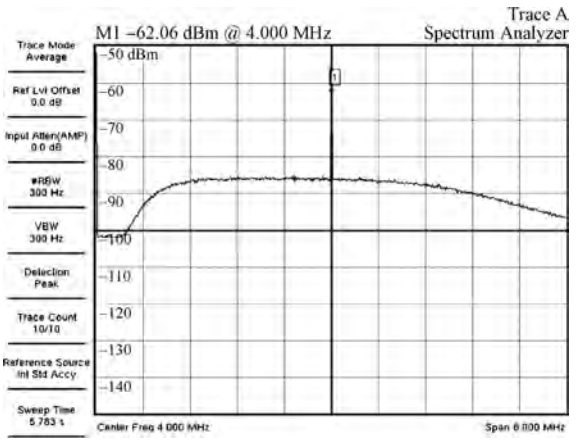

Fig. 12. Signal spectrum of the AGC output for GPS L1 and Compass B1 band.

5. Conclusion

A low power and low noise figure highly integrated dual-channel multimode GNSS receiver is presented in this paper. A $\Sigma\Delta$ fractional-N synthesizer and a programmed RFA are integrated in the chip, which can support nine modes for different GNSS applications. This architecture improves the compati-

Table 3. Compared results with other work.

Parameter	Ref. [24]	Ref. [25]	Ref. [26]	Ref. [27]	This work
Process	0.18 μm CMOS	0.13 μm CMOS	0.18 μm CMOS	0.13 μm CMOS	0.18 μm CMOS
Supply voltage (V)	1.8	1.2	1.8	1.2	1.8
NF (dB)	4.1/4.5/5.1	4.3/4.5	2.4	2.3/2.2	$\leqslant$ 5.3
Gain (dB)	26/33/21.4	112/115	117	110	105/110
Compatible bands (MHz)	GPS/WCDMA/ Bluetooth	GPSL1/ GPSL2	GPSL1/L5/ Galileo E1/E5A	GPSL1/L5/ Galileo L1F/E5a	GPSL1/ CompassB1/B2/B3
Mode number	3	2	4	4	9
IF frequency (MHz)	2/2/2	4.092/4.092	3.25/3.42	N/A	4/46
Synthesizer structure	Integer	Integer	Integer	Integer	$\Sigma\Delta$ fractional-N
IF bandwidth (MHz)	N/A	2/2	9	4.53/24	5/21
Active area (mm^2)	2.4×2.4	N/A	N/A	3×3.8	3×3
Power consumption (mW)	2.5–3.5	12	54	26	72

bility of GNSS applications and is easy for consumers to use. This work largely minimizes the size of the chip and lowers the current dissipation, which satisfies the requirements of different GNSS applications. In the temperature range of –55 to 125 ℃ it has superior PVT (process, voltage and temperature) tolerance.

References

[1] Li Di, Yang Yintang, Wang Jiang'an, et al. Design of a low power GPS receiver in 0.18 μm CMOS technology with a $\Sigma\Delta$ fractional-N synthesizer. J Zhejiang Univ-Sci C (Comput & Electron), 2010, 11(6): 444

[2] Li Bing, Zhuang Yiqi, Long Qiang, et al. Design of a 0.18 μm CMOS multi-band compatible low power GNSS receiver RF frontend. Journal of Semiconductors, 2011, 32(3): 035007

[3] Vancorenland P, Coppejans P, De Cock W, et al. Optimization of a fully integrated low power CMOS GPS receiver. IEEE/ACM International Conference on Computer Aided Design, ICCAD 2002: 305

[4] Moon H, Heo S C, Yu H, et al. A 27 mW 2.2 dB NF GPS receiver using a capacitive cross-coupled structure in 65 nm CMOS. IEEE Custom Integrated Circuits Conference (CICC), 2010: 1

[5] Ikeuchi O, Saito N, Nauta B. Quadrature sampling mixer topology for SAW-less GPS receivers in 0.18 μm CMOS. IEEE Symposium on VLSI Circuits (VLSIC), 2010: 177

[6] Li Z B, Ni W H, Ma J, et al. A dual-band CMOS transceiver for 3G TD-SCDMA. Digest of Technical Papers, IEEE International Solid-State Circuits Conference, 2007: 344

[7] Aktas A, Ismail M. CMOS PLLs and VCOs for 4G wireless. Boston: Kluwer Academic, 2004, Chap. 5

[8] Ko J, Kim J, Cho S, et al. A 19-mW 2.6-mm^2 L1/L2 dual-band CMOS GPS receiver. IEEE J Solid-State Circuits, 2005, 40(7): 1414

[9] Kim J, Cho S, Ko J. L1/L2 dual-band CMOS GPS receiver. Proceeding of the 30th European Solid-State Circuits Conference, 2004: 87

[10] Montagna G, Gramegna G, Bietti I, et al. A 35-mW 3.6-mm^2 fully integrated 0.18-μm CMOS GPS radio. IEEE J Solid-State Circuits, 2003, 38(7): 1163

[11] Shahani A R, Shaeffer D K, Lee T H. A 12 mW wide dynamic range CMOS front-end for a portable GPS receiver. Digest of Technical Papers, 43rd IEEE International Solid-State Circuits Conference, 1997: 368, 487

[12] Shaeffer D K, Lee T H. A 1.5-V, 1.5-GHz CMOS low noise amplifier. IEEE J Solid-State Circuits, 1997, 32: 745

[13] Blaakmeer S C, Klumperink E A M, Leenaerts D M W. The BLIXER, a wideband balun-LNA-I/Q-mixer topology. IEEE J Solid-State Circuits, 2008, 43(12): 2706

[14] Zito D, Pepe D, Neri B. Low-power RF transceiver for IEEE 802.15.4 (ZigBee) standard applications. 13th IEEE International Conference on Electronics, Circuits and Systems, 2006: 1312

[15] Broussev S S, Lehtonen T A, Tchamov N T. A wide-band low phase-noise LC-VCO with programmable $K_{\rm vco}$. IEEE Microw Wireless Compon Lett, 2007, 17(4): 274

[16] De Muer B, Steyaert M. CMOS fractional-N synthesizers: design for high spectral purity and monolithic integration. Norwell: Kluwer Academic Publishers, 2003: 53

[17] Yamazaki H, Oishi K, Gotoh K. An accurate center frequency tuning scheme for 450-kHz CMOS $G_{\rm m}$–C bandpass filters. IEEE J Solid-State Circuits, 1999, 34(12): 1691

[18] Yoo C, Jung K, Lee J W, et al. A 15 MHz, 2.6 mW, sixth-order bandpass $G_{\rm m}$–C filter in CMOS. Proceedings of the 40th Midwest Symposium on Circuits and Systems, 1997, 1: 306

[19] Weng J H, Yang C Y. An active $G_{\rm m}$–C filter using a linear transconductance. IEEE Conference on Electron Devices and Solid-State Circuits, 2007: 909

[20] Farhad M M, Mirzakuchaki S. A second-order $G_{\rm m}$–C continuous time filter in mobile radio receiver architecture. 2nd International Conference on Education Technology and Computer (ICETC), 2010: 170

[21] Aloi D N, Alsliety M, Akos D M, et al. A methodology for the evaluation of a GPS receiver performance in telematics applications. IEEE Trans Instrumentation and Measurement, 2007, 56(1): 11

[22] Cloutier M, Varelas T, Cojocaru C, et al. A 4-dB NF GPS receiver front-end with AGC and 2-b A/D. Proceedings of the IEEE Custom Integrated Circuits, 1999: 205

[23] Lee H Y, Wang I H, Liu S I. A 7-bit 400 MS/s sub-ranging flash ADC IN 0.18 μm CMOS. IEEE International SOC Conference, 2007: 11

[24] Chung T C, Chen C W, Chen O T C, et al. A multi-band RF frontend receiver for Bluetooth, WCDMA, and GPS applications. IEEE International Symposium on Micro-NanoMechatronics and Human Science, 2003: 1175

[25] Abdelrahim T A, Elesseily T, Abdou A S, et al. A 12-mW fully integrated low-IF dual-band GPS receiver on 0.13 μm CMOS. IEEE International Symposium on Circuits and Systems, 2007: 3034

[26] Detratti M, Lopez E, Perez E. Dual-band RF receiver chipset for Galileo/GPS applications. IEEE/ION Position, Location and Navigation Symposium, 2008: 851

[27] Moon Y, Cha S, Kim G. A 26 mW dual-mode RF receiver for GPS/Galileo with L1/L1F and L5/E5a bands. International SoC Design Conference, 2008: 421