A 31.7-GHz high linearity millimeter-wave CMOS LNA using an ultra-wideband input matching technique*

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Abstract: A CMOS low-noise amplifier (LNA) operating at 31.7 GHz with a low input return loss (S_{11}) and high linearity is proposed. The wideband input matching was achieved by employing a simple LC compounded network to generate more than one S_{11} dip below –10 dB level. The principle of the matching circuit is analyzed and the critical factors with significant effect on the input impedance ($Z_{\rm in}$) are determined. The relationship between the input impedance and the load configuration is explored in depth, which is seldom concentrated upon previously. In addition, the noise of the input stage is modeled using a cascading matrix instead of conventional noise theory. In this way $Z_{\rm in}$ and the noise figure can be calculated using one uniform formula. The linearity analysis is also performed in this paper. Finally, an LNA was designed for demonstration purposes. The measurement results show that the proposed LNA achieves a maximum power gain of 9.7 dB and an input return loss of < -10 dB from 29 GHz to an elevated frequency limited by the measuring range. The measured input-referred compression point and the third order inter-modulation point are –7.8 and 5.8 dBm, respectively. The LNA is fabricated in a 90-nm RF CMOS process and occupies an area of 755×670 μm^2 including pads. The whole circuit dissipates a DC power of 24 mW from one 1.3-V supply.

Key words: CMOS; low noise amplifier; input matching; millimeter-wave

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1. Introduction

With the development of wireless communication, millimeter-wave technology has achieved significant progress because of its compensation to the spectrum blockage in low frequency ranges and satisfaction of the increasing requirements for higher data-rate transmission. Traditionally, monolithic millimeter-wave integrated circuits (MMICs) have been fabricated using III–V compound semiconductor technologies due to their higher electron mobility and lower substrate loss than previous CMOS technologies[1−3]. However, the CMOS process is particularly attractive for its low costs, low power, and ability of integration with base-band ICs. Practically, the improved modern CMOS technology has been demonstrated to be feasible to render the millimeter-wave circuitry[4−6].

The low noise amplifier (LNA), which plays an important role in a wireless receiver frontend, is widely expected to deliver sufficient power gain for an incoming signal while suppressing the potential noise for a desirable signal-to-noise ratio at an output. It is one of the most crucial evaluation criteria determining whether a CMOS process is suitable for millimeter-wave applications. Additionally, implementation of an LNA involves a wide range of circuit design and analyzing theories, including linear (such as noise analysis) and nonlinear (such as linearity) aspects. These theories intensively reflect the quintessence in RF CMOS circuit design.

In this paper, a 3-stage common source LNA with ultra-wideband input matching is proposed to provide insight into the 30-GHz range millimeter-wave integrated circuit design. The wideband input matching characteristic of the LNA was achieved by a compounded LC network, which will be discussed in detail. Additionally, the designed LNA exhibits a good linearity which will be also analyzed.

2. Design considerations

2.1. Input matching schemes

As far as maximum power transmission is concerned, a constructive input matching network is needed in front of the LNA. Moreover, the input transistor should be characterized primarily because of its dominant role in matching realization. In addition, to obtain a positive real part of input impedance ($\mathrm{Re}[Z_{\rm in}]$), we also deal with the problem of how to realize wideband input matching. To conquer this challenge, some previously published papers, such as Refs. [7–9], have provided their respective perspectives. They all realized wideband input matching in the frequency band lower than 30 GHz. The achievement of Ref. [7] is attributed to a negative feedback resistor $R_{\rm FB}$ and a π-like input network, which consists of a shunt capacitor $C_{\rm in}$, a series gate inductor $L_{\rm g}$, and a parasitic capacitor $C_{\rm gs}$. Besides $R_{\rm FB}$ and $L_{\rm g}$, Reference [8] introduced the prevalent source degenerated technique and took an LC load

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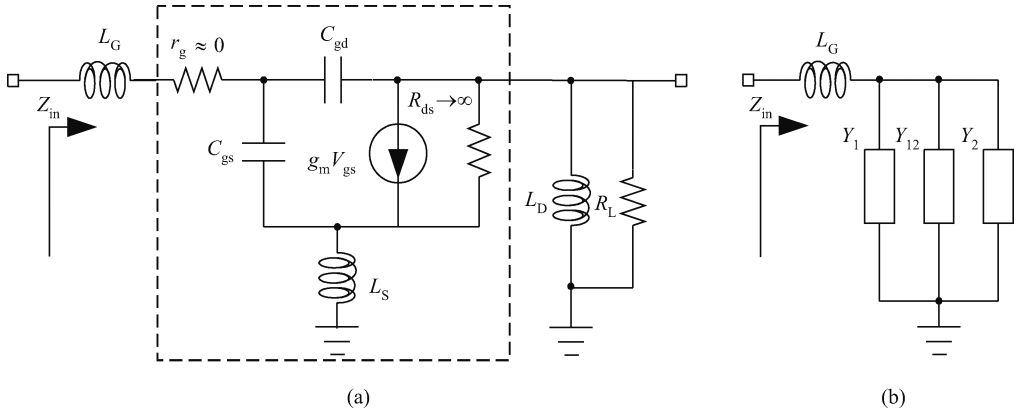

Fig. 1. (a) Small signal input matching circuit. (b) Equivalent circuit of (a).

in consideration. The whole network was regarded as an RLC branch. Both References [7, 8] neglect the transistor's parasitic capacitor between gate and drain (C_{gd}) which have to be considered at relatively high frequencies. Its fundamental effect on S_{11} will be illustrated in the following section. Different from Refs. [7, 8], wideband input matching was achieved in Ref. [9] but incorporating the C_{gd}. However, the authors of Ref. [9] derived the resonance frequencies with the assumption $L_{S1} = L_{G1}$. Anyone with experience in electromagnetic simulation can draw a conclusion from their layout that the assumption is unreasonable. Additionally, the load impedance of the first source-degenerative stage seems to be small over the frequencies in which they were interested. However, in the elevate band the load configuration must be dealt with. Figure 1 shows the input matching circuit incorporating a source degenerated inductor L_s and a gate-series inductor L_g in this work. R_L is considered as the real part of the following stages. Since r_g is small and R_{ds} is enough large, they all can be ignored for analysis simplification.

The ABCD matrix, well known for its cascading characteristic, can be employed to provide the uniform method for input matching and noise analyzing. As far as a 2-port network surrounded by the dash line box shown in Fig. 1(a) is concerned, its ABCD matrix can be derived as:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \dfrac{1+sL_S\left(g_m+sC_{gs}\right)}{1-\dfrac{g_m}{sC_{gd}}+sL_S\left(g_m+sC_{gs}\right)} & \dfrac{1+sL_S\left(g_m+sC_{gs}\right)}{sC_{gd}\left[1+sL_S\left(g_m+sC_{gs}\right)\right]-g_m} \\ \dfrac{g_m+sC_{gs}}{1-\dfrac{g_m}{sC_{gd}}+sL_S\left(g_m+sC_{gs}\right)} & \dfrac{sC_{gs}+sC_{gd}\left[1+sL_S\left(g_m+sC_{gs}\right)\right]}{sC_{gd}\left[1+sL_S\left(g_m+sC_{gs}\right)\right]-g_m} \end{bmatrix}. \tag{1}$$

The ABCD matrix of the load impedance right in Fig. 1(a) is given by:

$$\begin{bmatrix} A_{load} & B_{load} \\ C_{load} & D_{load} \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ \dfrac{1}{sL_D||R_L} & 1 \end{bmatrix}. \tag{2}$$

New input impedance Z_{in} is related to Eqs. (1) and (2), combining Eqs. (1) and (2) results in:

$$Z_{in} = sL_G + \left[\frac{1}{\dfrac{1}{sC_{gs}}+\omega_T L_S + sL_S} + \frac{\omega_T L_D/\left(R_L+sL_D\right)}{\left(\dfrac{1}{sC_{gs}}+\omega_T L_S+sL_S\right)\left(\dfrac{1}{sC_{gd}}+sL_D||R_L\right)} + \frac{1}{\dfrac{1}{sC_{gd}}+sL_D||R_L} \right]^{-1}, \tag{3}$$

where $\omega_T = g_m/C_{gs}$, represents the characteristic frequency. It is noteworthy from Eq. (3) that Z_{in} can be factorized into 4 parts, so Figure 1(a) is equivalent to Fig. 1(b). The conductance of Y_1, Y_{12}, and Y_2 are the left, middle, and right components in the denominator of Eq. (3). Significantly, the effect of the load and C_{gd} can be derived from Eq. (3) and its guidance to wideband input matching will be generalized below.

$$\begin{aligned} S_{11}^1 &= \frac{1-R_S/Y_1}{1+R_S/Y_1} = \frac{\dfrac{1}{sC_{gs}}+s\left(L_G+L_S\right)+\omega_T L_S - R_S}{\dfrac{1}{sC_{gs}}+s\left(L_G+L_S\right)+\omega_T L_S + R_S} \\ &= \frac{s^2+\omega_{01}^2}{s^2+2\dfrac{\omega_{01}}{Q_{01}}+\omega_{01}^2}, \end{aligned} \tag{4}$$

in which

$$\omega_{01} = \frac{1}{\sqrt{\left(L_G+L_S\right)C_{gs}}}, \quad Q_{01} = \frac{\omega_{01}\left(L_G+L_S\right)}{R_S}. \tag{5}$$

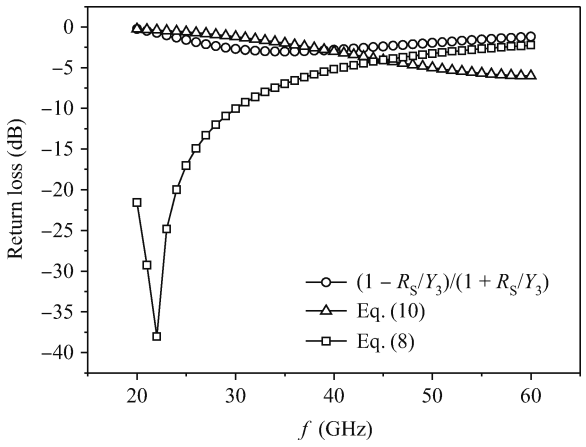

Fig. 2. Calculated return loss in dB by Eqs. (4) and (6) and $(1 - R_S/Y_3)/(1 + R_S/Y_3)$ versus frequency.

Similarly,

$$S_{11}^2 = \frac{1 - R_S/Y_2}{1 + R_S/Y_2} = \frac{\dfrac{1}{sC_{gs}} + s\left(L_G + \dfrac{Q_P^2}{1+Q_P^2}L_D\right) + \dfrac{R_L}{1+Q_P^2} - R_S}{\dfrac{1}{sC_{gs}} + s\left(L_G + \dfrac{Q_P^2}{1+Q_P^2}L_D\right) + \dfrac{R_L}{1+Q_P^2} + R_S} = \frac{s^2 + \omega_{02}^2}{s^2 + 2\dfrac{\omega_{02}}{Q_{02}}\omega_{02}^2}, \tag{6}$$

in which,

$$Q_P = \frac{\omega L_D}{R_L}, \quad \omega_{02} = \frac{1}{\sqrt{\left(L_G + \dfrac{Q_P^2}{1+Q_P^2}L_D\right)C_{gd}}},$$

$$Q_{01} = \frac{\omega_{02}\left(L_G + \dfrac{Q_P^2}{1+Q_P^2}L_D\right)}{R_S}. \tag{7}$$

If the branch of Y_1 and Y_2 are configured to resonate at lower corner frequency ω_{01} and upper corner frequency ω_{02}, the branch of Y_{12} must resonate at the geometric mean frequency of ω_{01} and ω_{02}. Both Equations (4) and (6) assume that R_S is cancelled; this may not happen in practice, however, the assumption will not affect the validity of the discussion. It is proved by Fig. 2.

Now we can use the generalization above to evaluate the effect of C_{gd} and R_L on the input matching mentioned above. Figure 3 depicts the relationship between $|S_{11}|$ in dB ($20\log_{10}[|(Z_{in}-R_s)/(Z_{in} + R_S)|]$) and C_{gd} and R_L by a 3-D plot. There obviously exists a deep notch in S_{11} when C_{gd} is among 40–60 fF.

Actually, the value of C_{gd} is closely related to the optimization of the input transistor. In addition, for the purpose of compensating the gain degeneration caused by the employment of

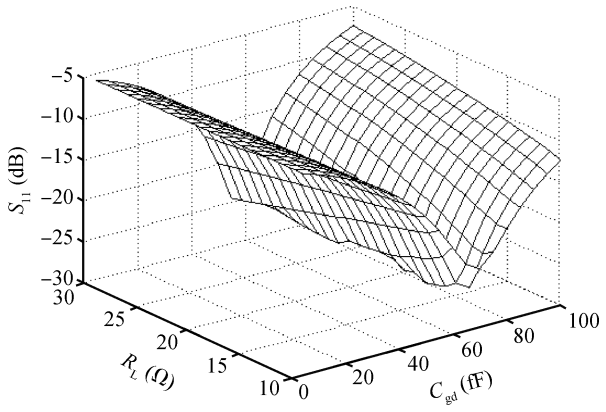

Fig. 3. Calculated S_{11} in dB with respect to the variance of R_L and C_{gd}.

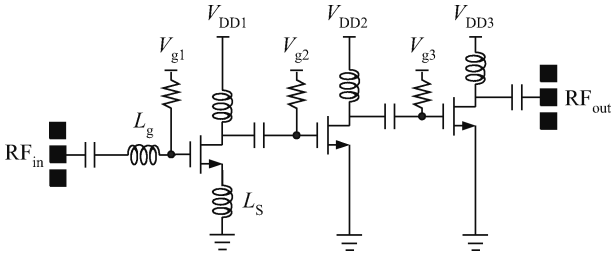

Fig. 4. Schematic of the proposed 3-stage common source LNA.

L_S, a multi-stage topology is needed to provide sufficient gain. Therefore, the input resistance of the render stages should cater for the span of R_L. Finally, a simplest case is considered in this work that a source degenerated structure is employed as the first stage for wideband input matching, a common-source structure is introduced as the second stage for gain compensation and another common-source topology is used to realize further amplification and output matching. The circuit is schematized in Fig. 4.

Figure 5 shows the simulated and calculated S_{11} versus frequency when all of the factors aforementioned are taken in consideration. Because of the simplification in calculation they only have similar tendency in the lower and upper frequency bands, but the two results correspond well in the range in which we are interested.

2.2. Noise factor derivation

The noise figure (NF) of a multi-stage LNA was proved to be decided by the first stage transistor. The dominant noise in CMOS devices is referred to as the channel noise and the gate-induced noise due to non-quasi-static effect[11]. In this work, a source-degenerative topology is employed as the input stage. Therefore, the noise equivalent circuit of the source-degenerative transistor will be modeled. The upper diagram in Fig. 6 shows the noise composition of the source-degenerative topology. Taking advantage of the ABCD matrix derived previously, the output channel noise can be converted at the input, as shown in the lower diagram in Fig. 6. According to the definition, the noise factor can be given by

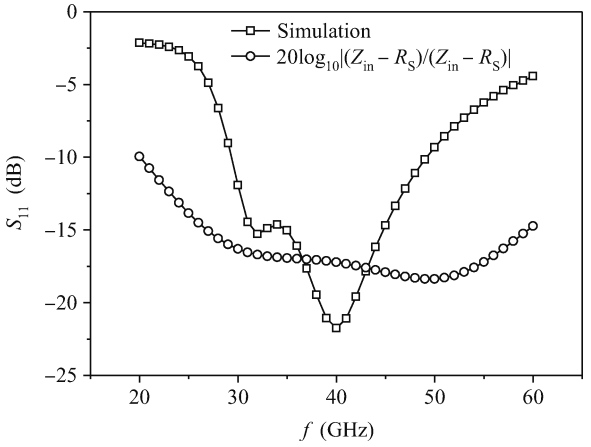

Fig. 5. Comparison of simulated and calculated S_{11}.

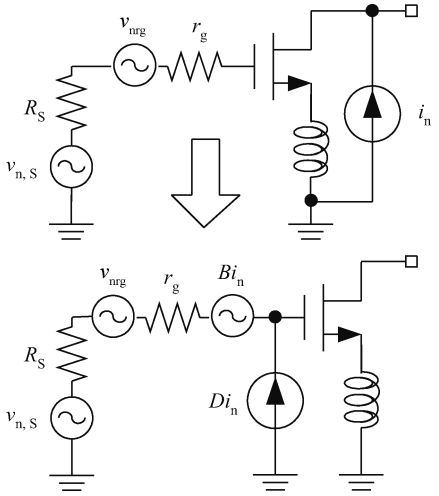

Fig. 6. The inductively degenerated circuit model for noise calculation.

$$\begin{aligned} F_{\text{noise}} &= \frac{\text{SNR}_{\text{in}}}{\text{SNR}_{\text{out}}} \\ &= \frac{4\kappa T r_{\text{g}} + |B + DR_{\text{S}}|^2 \, 4\kappa T \gamma g_{\text{d0}}}{4\kappa T R_{\text{S}}} \\ &= \frac{r_{\text{g}}}{R_{\text{S}}} + |B + DR_{\text{S}}|^2 \, \frac{\gamma g_{\text{d0}}}{R_{\text{S}}}, \end{aligned} \tag{8}$$

where SNR_{in} and SNR_{out} are input and output signal to noise ratio, respectively. B and D are parameters of the ABCD matrix expressed in Eq. (1).

Figure 7 shows the calculated NF of Fig. 6 without optimization, a simulated result of the proposed LNA is also included. It can be seen that the calculated result correctly reflects the NF frequency response without using the traditional 2-port network noise theory. The alternative way delivered in this work can be a substitute solution for NF estimation.

2.3. Linearity analysis

Normally, the $P_{1\text{dB}}$ and IIP_3 are used to evaluate the linearity of an LNA. The voltage-to-current (V–I) conversion can be

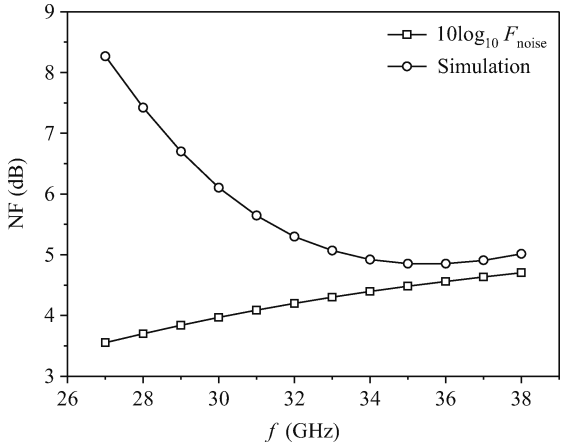

Fig. 7. The calculated NF of input stage and the simulated one of the proposed LNA.

expanded by Taylor's series with higher order terms neglected:

$$i\left(V_{\text{DC}} + v_{\text{gs}}\right) \approx C_0 + C_1 v_{\text{gs}} + C_2 v_{\text{gs}}^2 + C_3 v_{\text{gs}}^3. \tag{9}$$

According to Ref. [12], a 3-point method can be introduced to obtain the coefficient of Eq. (9). The IIP_3 is derived as:

$$\begin{aligned} \text{IIP}_3 &= \frac{2}{3}\left|\frac{C_1}{C_3}\right| \frac{1}{R_{\text{S}}} \\ &= \frac{4V_{\text{gs}}^2}{R_{\text{S}}}\left|\frac{g\,(0)}{g(V_{\text{gs}}) + g(-V_{\text{gs}}) - 2g(0)}\right|. \end{aligned} \tag{10}$$

Since, the V_{gs} arise from the input voltage (V_{S}) multiplying the input quality factor (Q_{in}), Equation (10) is rewritten as:

$$\text{IIP}_3 = \frac{4V_{\text{S}}^2}{Q_{\text{in}}^2 R_{\text{S}}}\left|\frac{g\,(0)}{g(V_{\text{S}}) + g(-V_{\text{S}}) - 2g(0)}\right|, \tag{11}$$

where

$$Q_{\text{in}} = \frac{V_{\text{gs}}}{2R_{\text{S}}\,|I_{\text{in}}|}. \tag{12}$$

Under matching conditions, I_{in} can be derived from Fig. 1(a):

$$\begin{aligned} I_{\text{in}} &= V_{\text{gs}} s C_{\text{gs}} + V_{\text{gd}} s C_{\text{gd}} \\ &\approx V_{\text{gs}} s C_{\text{gs}} + V_{\text{gs}} g_{\text{m}} s C_{\text{gd}} R_{\text{L}} + V_{\text{gs}} g_{\text{m}} s \frac{L_{\text{S}}}{L_{\text{D}}} C_{\text{gd}}\left(R_{\text{L}} + sL_{\text{D}}\right). \end{aligned} \tag{13}$$

Substituting Eq. (13) into Eq. (12),

$$Q_{\text{in}} \approx \frac{1}{2R_{\text{S}}\left[\omega C_{\text{gs}} + g_{\text{m}}\omega C_{\text{gd}}\left(R_{\text{L}} + \dfrac{L_{\text{S}}}{L_{\text{D}}}\sqrt{R_{\text{L}}^2 + (\omega L_{\text{D}})^2}\right)\right]}. \tag{14}$$

It can be concluded from Eqs. (11) and (14) that large C_{gs}, C_{gd} and L_{S} result in a high IIP_3, the significance of this conclusion will be demonstrated in the following section.

Table 1. Measured performance comparison.

Parameter	Process	S_{11} BW* (GHz)	Peak S_{21} (dB)	NF_{av} (dB)	P_{1dB} (dBm)	IIP_3 (dBm)	V_{dd} (V)	Power (mW)
This wok	90 nm CMOS	> 10 (29–higher)	9.7 @ 31.7 GHz	5.4**	–7.8	5.8	1.3	24
Ref. [5]	90 nm CMOS	14 (31–45)	7.3 @ 35 GHz	N/A	–12.7	0	1.5	10.5
Ref. [6]	90 nm SOI	0 in whole band	11.9 @ 35 GHz	3.6	–13	N/A	2.4	40.8
Ref. [7]	90 nm CMOS	> 26 (1.6–28)	10.7 @ 2.9 GHz	3.7	–9	+4	1.2	21.6
Ref. [9]	130 nm CMOS	6 (21–27)	15.6 @ 24 GHz	3.48	N/A	–12	1.2	22.07
Ref. [10]	130 nm CMOS	> 4 (24–higher)	9.2 @ 23.6 GHz	3.7	–2.9	N/A	1	2.78

*BW: bandwidth below –10 dB. **Simulated result.

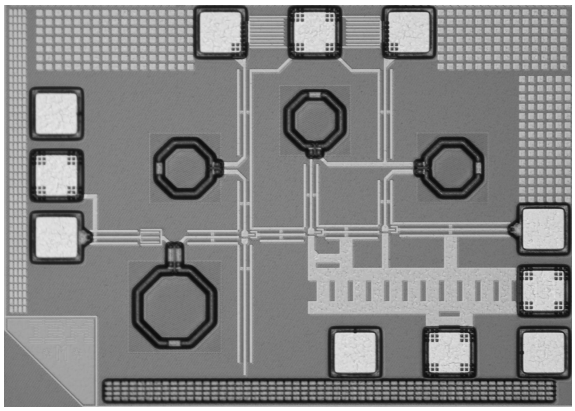

Fig. 8. Die photo of the proposed LNA.

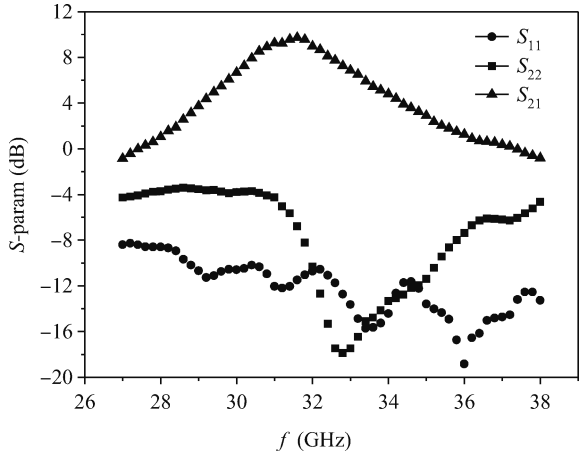

Fig. 9. Measured S-parameters and simulated NF against frequency.

3. Experiment results and discussions

The 3-stage common source cascaded topology shown in Fig. 4 was utilized for the purpose of validating the aforementioned wideband input matching technique. The chip snap-shot of the finished circuit is shown in Fig. 8. Finally, the measurements were performed and some results in terms of the S-parameter, P_{1dB}, and IIP_3 were obtained. The measured S-parameter is symbolized in Fig. 9. It is obvious that the measured S_{11} is lower than the –10 dB level from 29 to 38 GHz, exhibiting an excellent input matching performance and corresponding well with the previous analysis and simulation in Section 2. The maximum measured S_{21} is 9.7 dB at 31.7 GHz. Some shifts can be observed mainly in S_{22}; it may be attributed

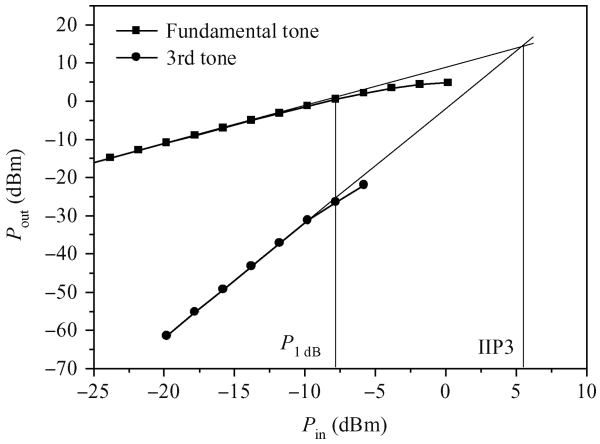

Fig. 10. Measured P_{1dB} and IIP_3 at 31.7 GHz.

to the parasitic capacitance induced by the output pad, which shifts the resonating frequency of the output matching network. To characterize the linearity of the proposed LNA, a dual-tone signal was imposed on the input to measure the output power with respect to the input power. The measured results shown in Fig. 10 indicate that the input P_{1dB} and IIP_3 are –7.8 dBm and 5.8 dBm, respectively. It can be concluded that the proposed LNA exhibits good circuit linearity. Table 1 summarizes various previously and recently published LNAs around 30 GHz for comparison. It is observed that the input matching and linearity of this work outperforms the compared LNAs. The proposed LNA obtained a moderate gain with moderate power consumption. It can be explained that larger L_S will improve the input matching and the linearity (explained by Eqs. (11) and (14)) but degenerate the power gain, larger C_{gs} and C_{gd} will improve the linearity as well as power gain at the expense of larger power consumption.

4. Conclusion

This paper proposed a 3-stage common source LNA with ultra-wideband input matching performance and high linearity, which is suitable for the frontend of 30-GHz RF transmitters. The LNA's features include that the S_{11} is lower than –10 dB, covering almost the whole testing band with a 9.7 dB maximum power gain at 31.7 GHz. The measured inputs P_{1dB} and IIP_3 are –7.8 dBm and 5.8 dBm, respectively. The whole circuit draws a current of 18.5 mA from one 1.3 V supply.

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