A digital background calibration algorithm of a pipeline ADC based on output code calculation

Shao Jianjian(邵健健)†, Li Weitao(李玮韬), Sun Cao(孙操), Li Fule(李福乐), Zhang Chun(张春), and Wang Zhihua(王志华)

Institute of Microelectronics, Tsinghua University, Beijing 100084, China

Abstract: This paper proposes a digital background calibration algorithm to correct linearity errors in a pipelined analog-to-digital converter (ADC). The algorithm does not modify the analog circuit of pipelined stages and calibrates the raw conversion output by using a backend digital logic. Based on the analysis of the output codes, the calibration logic estimates the bit weight of each stage and corrects the outputs. An experimental 14-bit pipelined ADC is fabricated to verify the algorithm. The results show that INL errors drop from 20 LSB to 1.7 LSB, DNL errors drop from 2 LSB to 0.4 LSB, SNDR grows from 57 to 65.7 dB and THD drops from –58 to –81 dB. The linearity of the pipelined ADC is improved significantly.

Key words: pipeline; ADC; output code calculation; background calibration
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1. Introduction

High performance analog-to-digital converters (ADCs) are required in high-quality wireless communications, image recognition, medical applications, and various other areas. Pipelined ADCs can provide high-resolution and high-speed data conversion with low power dissipation. The accuracy of a pipelined ADC is limited by nonideal factors, in which capacitor mismatch and finite opamp gain are the most critical. These two non-ideal effects change the inter-stage gain and cause conversion errors. Different calibration techniques were proposed to compensate for the nonideal effects and to relax the requirement of pipeline stages. In Refs. [1–3], errors were measured and stored in the digital form, and were compensated for in the digital or analog domain. In Ref. [4], the capacitor error-averaging technique was introduced, which generated two residue voltages containing complementary errors and averaged them by double sampling. In Refs. [5–8], a correlation-based calibration technique was given. A random signal was inserted into the MDAC, and calibration information was extracted by correlation analysis. All these techniques modify pipeline stages to allow extra control for calibration, which increases the complexity of the analog signal processing and may decrease the circuit speed. Alternatively, a digital background calibration algorithm without modifying pipeline stages was proposed in Ref. [9]. Based on code density testing, this algorithm calculated the correct codes according to the discontinuity in the histogram data. However, the calibration circuit implementation was complex because each output code need to be stored.

In this paper, a new digital background calibration scheme is proposed to calibrate the inter-stage gain error of the pipelined ADC. The algorithm estimates the bit weight of each stage and calculates the correct codes. The digital outputs of each stage are collected and classified to supply estimation information. Compared to the calibration techniques in Refs. [1–8], modification of pipelined stages is not required. Compared to the technique in Ref. [9], both the logic overhead and switching activity for calibration are lower. Test results show that the second harmonic is deceased from –76 to –85 dB, and the third harmonic is reduced from –76 to –88 dB. Total harmonic distortion drops from –58 to –81 dB. After calibration, the DNL errors reduced from 2 to 0.4 LSB, and INL errors drop from 20 LSB to 1.7 LSB.

2. Proposed calibration scheme

The proposed digital background calibration scheme is described in Fig. 1. The output codes are collected by estimation block to extract calibration information. The bit weight of each stage is estimated by the estimation block and supplied to a calculation block to calculate the correct output codes in real-time. With the calibration scheme, the typical pipelined stages need no modification and the calibration is processed during the normal analog-to-digital operation.

3. Proposed estimation algorithm

The proposed algorithm is applied to 1-bit/stage pipelined ADCs. For the output codes, there is a weight associated with each bit. Due to the inter-stage gain error, the bit weight of each stage deviates from the nominal design value. By estimating

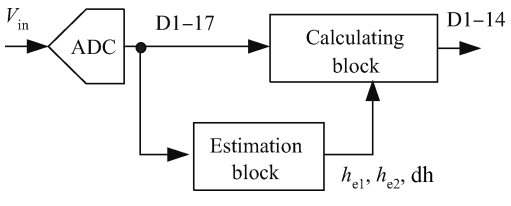

Fig. 1. The proposed calibration scheme.

† Corresponding author. Email: shao_x85@sina.com
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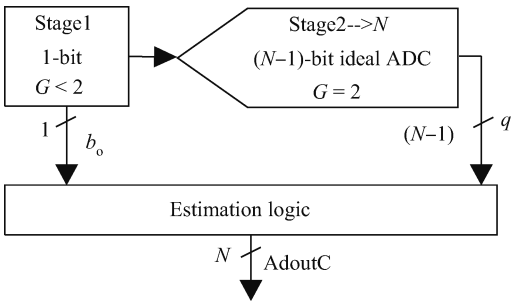

Fig. 2. N-bit pipelined ADC block diagram for single stage calibration.

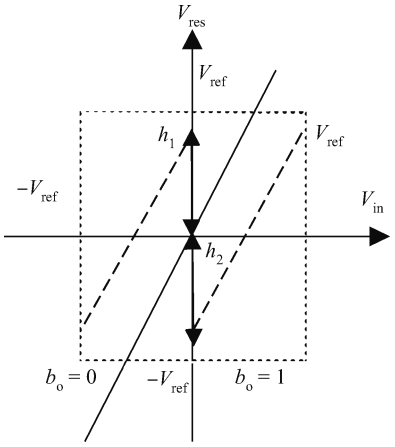

Fig. 3. Transformed transfer plot for calibration of stage 1.

the bit weigh of each stage, the algorithm calculates the correct digital outputs of the pipelined ADC.

3.1. Calibration of a single stage

An N-bit pipelined ADC is introduced to illustrate the calibration process of a single stage of a pipelined ADC. As shown in Fig. 2, the pipelined ADC is composed of a 1-bit stage and an ideal backend (N–1)-bit ADC. The digital output of the ADC before calibration is

$$A_{\text{dout}} = b_{\text{o}} w_1 + q, \tag{1}$$

where b_{o} is the digital output of stage 1, w_1 is the bit weight of stage 1, and q is the digital output of the ideal backend ADC. The chain line in Fig. 3 shows the transfer curve of stage 1 with nonideal effects taken into account. V_{in} and V_{res} are respectively the input and output analog voltage of stage 1, and V_{ref} is the reference voltage.

The value of the transition is equal to the bit weight of stage 1 and is labeled h, which can be written in the terms of h_1 and h_2.

$$h = h_1 + h_2, \tag{2}$$

where h_1 is the positive segment of the transition and h_2 is the negative segment of it. The estimation value of h, h_1 and h_2 are h_{e}, h_{e1} and h_{e2} respectively.

As seen in Fig. 3, the discontinuous transfer curve is transformed to a line by the parallel movement of the two segments. Correspondingly, D_{o} is defined by

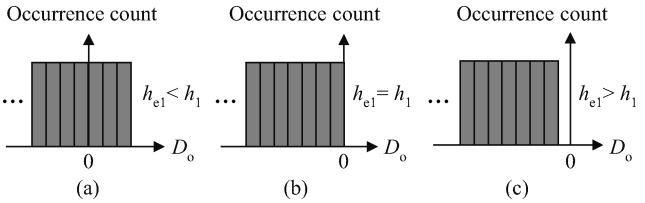

Fig. 4. Code occurrence count schematic diagram when $b_{\text{o}} = 0$.

$$D_{\text{o}} = \begin{cases} q - h_{\text{e1}}, & b_{\text{o}} = 0, \\ q + h_{\text{e2}}, & b_{\text{o}} = 1. \end{cases} \tag{3}$$

The estimation process of h_{e1} is discussed as follows. Assume that S output codes are collected. They are categorized into two overlapping types, one with $b_{\text{o}} = 0$ and the other with $D_{\text{o}} < 0$ in the case of $b_{\text{o}} = 0$. The occurrence counts of the two types of codes are labeled f_{a1} and f_{b1}, respectively. With different relationships between h_{e1} and h_1, D_{o} may be positive or negative when b_{o} is zero, as shown in Fig. 4, and f_{a1} may be not equal to f_{b1}, which can be described by

$$\begin{cases} f_{\text{a1}} > f_{\text{b1}}, & h_{\text{e1}} < h_1, \\ f_{\text{a1}} = f_{\text{b1}}, & h_{\text{e1}} \geqslant h_1. \end{cases} \tag{4}$$

The relationship between f_{a1} and f_{b1} indicates whether h_{e1} is bigger or smaller than h_1, which is the key idea behind the estimation. If $f_{\text{a1}} > f_{\text{b1}}$, h_{e1} increases by

$$h_{\text{e1}} = h_{\text{e1}} + \mu_1 (f_{\text{a1}} - f_{\text{b1}}), \tag{5}$$

where μ_1 is the step size to control the change of h_{e1}, and it is related to the initial value of h_{e1}. They all affect the algorithm performance. According to Eq. (5), the adjustment is unidirectional. In order to track the environmental and internal changes in real-time, the adjustment must be developed to be bidirectional. So, in the case of $f_{\text{a1}} = f_{\text{b1}}$, the value of h_{e1} decreases, which can be described by

$$h_{\text{e1}} = h_{\text{e1}} - \mu. \tag{6}$$

Based on f_{a1} and f_{b1}, h_1 can be estimated by successive approximation.

The scheme of adding windows is used to reduce the effect of the reference voltage instability of the comparator. Taken the jitter of reference voltage into account, the code density of stage 1 after the initial calibration is shown in Fig. 5. And the bit weight of stage 1 cannot be estimated correctly. Therefore, three windows are added to make sure the distribution of the code is uniform near the reference voltage of the comparator. Because the three windows are used to compensate for the reference jitter, width of windows should be approximate to the width of non-uniform code caused by jitter. Based on the calibration described above, the influence of jitter can be estimated. The length of the window is small enough to enhance the adaptability to different analog inputs. The occurrence counts of codes in the windows are N_1, N_2 and N_3 respectively. dh is defined as

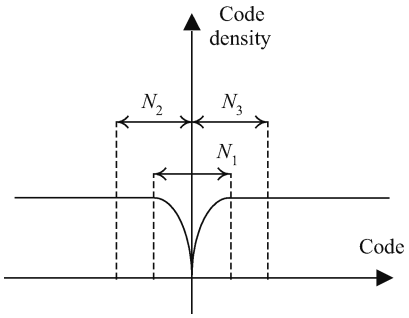

Fig. 5. Three windows used in stage 1.

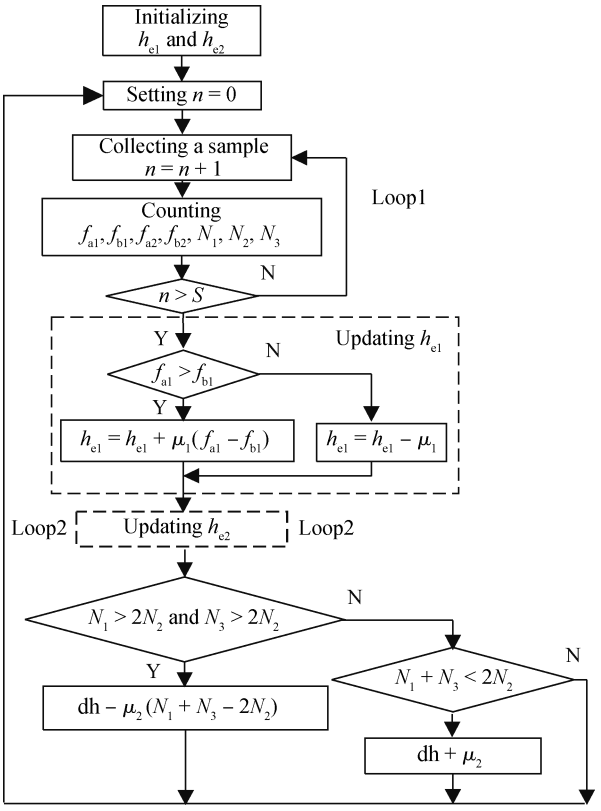

Fig. 6. Flowchart of the digital background calibration algorithm.

$$\mathrm{dh} = \begin{cases} \mathrm{dh} - \mu_2(N_1 + N_3 - 2N_2), \\ \qquad N_1 > 2N_2 \text{ and } N_3 > 2N_2, \\ \mathrm{dh} + \mu_2, \quad N_1 + N_3 < 2N_2, \end{cases} \tag{7}$$

where μ_2 is the step size. The bit weight is updated as

$$h_{e1} = h_{e1} + \mathrm{dh}. \tag{8}$$

The calibration process of h_{e1} is operated in two steps. h_{e1} is firstly estimated based Eqs. (5) and (6) until it is converged. Then the estimation of dh is operated according to Eq. (7) and the final adjustment of h_{e1} is operated by Eq. (8). The loop number is adaptively determined by the convergence speed.

With a similar method, the value of h_2 can be estimated. The calibration process of a single stage can be described by the flowchart shown in Fig. 6. With S samples collected in loop 1, the output codes are classified to estimate h_{e1}, h_{e2} and dh. The estimated values are stored to calibrate the raw conversion output and updated in a much lower speed compared to the sampling rate.

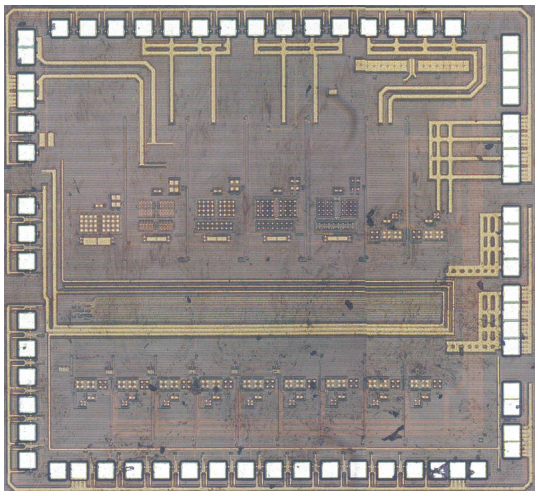

Fig. 7. Die micrograph.

3.2. Calibration of the higher level stages

A multistage pipelined ADC is calibrated from the lower level stages to the higher level stages. An M-bit pipelined ADC with the first T stages, which need calibration and an ideal backend $(M - T)$-bit ADC, is used to illustrate the calibration process. The calibration begins from stage T. With stage T calibrated, $h_{e1(T)}$, $h_{e2(T)}$, $\mathrm{dh}_{(T)}$ and $D_{o(T)}$ are obtained. $h_{e1(T)}$, $h_{e2(T)}$ and $\mathrm{dh}_{(T)}$ are stored to calculate the final digital output, and $D_{o(T)}$ is used to calibrate stage $T - 1$. The correct digital output of the M-bit pipelined ADC is described in Eq. (9), where q' is the digital output of the ideal backend $(M - T)$-bit ADC, and b_o is the original converted outputs of each stage.

$$\begin{aligned} \mathrm{AdoutC} = q' &+ \begin{pmatrix} -h_{e1(T)} - \mathrm{dh}_{(T)}, \text{ if } b_{o(T)} = 0 \\ h_{e2(T)} + \mathrm{dh}_{(T)}, \text{ if } b_{o(T)} = 1 \end{pmatrix} \\ &+ \begin{pmatrix} -h_{e1(T-1)} - \mathrm{dh}_{(T-1)}, \text{ if } b_{o(T-1)} = 0 \\ h_{e2(T-1)} + \mathrm{dh}_{(T-1)}, \text{ if } b_{o(T-1)} = 1 \end{pmatrix} \\ &+ \cdots + \begin{pmatrix} -h_{e1(1)} - \mathrm{dh}_{(1)}, \text{ if } b_{o(1)} = 0 \\ h_{e2(1)} + \mathrm{dh}_{(1)}, \text{ if } b_{o(1)} = 1 \end{pmatrix} \end{aligned} \tag{9}$$

4. Experimental results

A pipelined ADC is designed and fabricated to verify the proposed digital background calibration scheme. It is composed of ten 1-bit stages, five 1.5-bit stages and 2-bit backend flash ADC. The gain of 1-bit pipeline stages is designed to be 1.91 by setting the ratio of capacitors as 0.91/1. Due to the effect of the calibration algorithm on linearity error, the two-stage opamp without complex gain boosting is used, with the simulated gain less than 70 dB. As described in Fig. 1, the output codes are collected as the input of the algorithm. The last

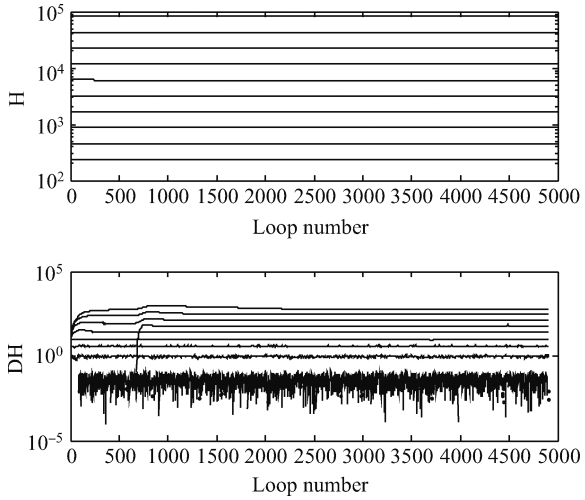

Fig. 8. Convergence process of weights.

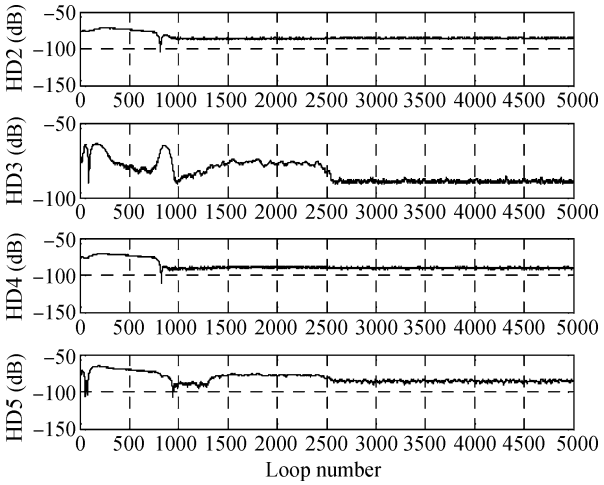

Fig. 9. Convergence process of harmonics.

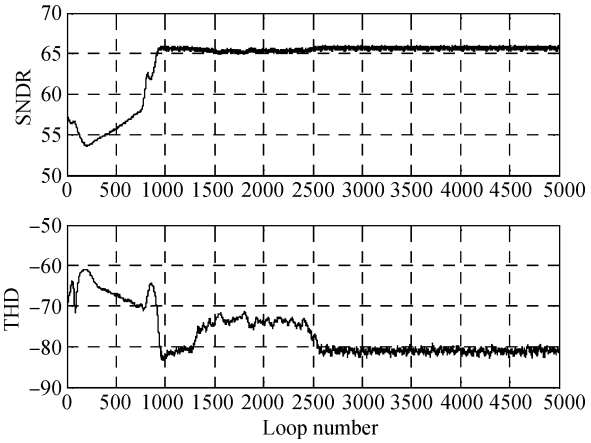

Fig. 10. The improvement of dynamic performance.

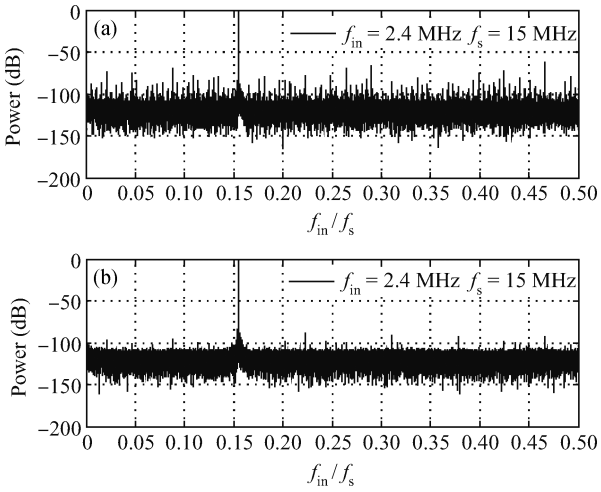

Fig. 11. Power spectra (a) before and (b) after calibration.

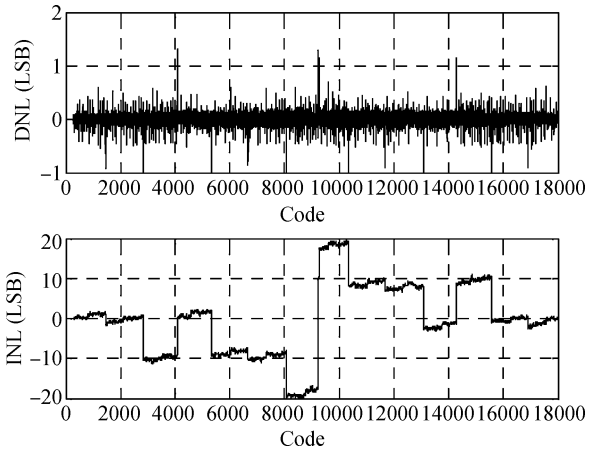

Fig. 12. Measured DNL and INL before calibration.

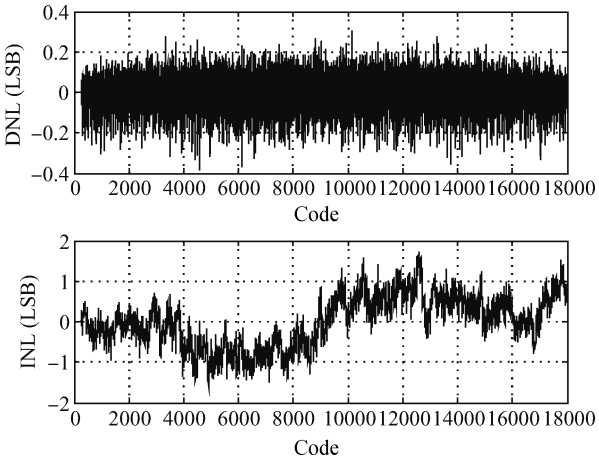

Fig. 13. Measured DNL and INL after calibration.

3-bit output of the pipelined ADC is truncated after calibration and a 14-bit binary output was obtained in real-time. As is shown in Fig. 7, the prototype chip is fabricated in a 180 nm 1P6M CMOS mixed-signal technology, occupying a die area of 2×2 mm^2.

Figure 8 shows the convergence process of the bit weights of the first 5 stages. In each cycle, 256000 samples are collected. Within 3000 cycles, both h_e and dh of each stage converges to a steady value. Correspondingly, the harmonics HD2, HD3, HD4 and HD5 drops significantly shown in Fig. 9. And the total harmonic distortion (THD) is suppressed from –58 to

–81 dB described in Fig. 10. SNDR grows from 57 to 65.7 dB and THD drops from –58 to –81 dB. Figures 12 and 13 show the static performance improvement. After calibration, the DNL errors reduced from 2 LSB to 0.4 LSB, and INL errors drop from 20 LSB to 1.7 LSB.

5. Conclusion

A cost-efficient digital background calibration algorithm is proposed to correct the inter-stage gain error. Test results show that the algorithm calibrates conversion errors due to random capacitor mismatch and finite opamp gain. The proposed algorithm calibrates pipelined ADCs without modifying pipeline stages and the logic overhead and switching activity of the calibration circuit are low, which is critical to high-speed and high-resolution ADC.

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