Full well capacity and quantum efficiency optimization for small size backside illuminated CMOS image pixels with a new photodiode structure*

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Abstract: To improve the full well capacity (FWC) of a small size backside illuminated (BSI) CMOS image sensor (CIS), the effect of photodiode capacitance (C_{PD}) on FWC is studied, and a reformed pinned photodiode (PPD) structure is proposed. Two procedures are implemented for the optimization. The first is to form a varying doping concentration and depth stretched new N region, which is implemented by an additional higher-energy and lower-dose N type implant beneath the original N region. The FWC of this structure is increased by extending the side wall junctions in the substrate. Secondly, in order to help the enlarged well capacity achieve full depletion, two step P-type implants with different implant energies are introduced to form a P-type insertion region in the interior of the stretched N region. This vertical inserted P region guarantees that the proposed new PD structure achieves full depletion in the reset period. The simulation results show that the FWC can be improved from 1289e– to 6390e–, and this improvement does not sacrifice any image lag performance. Additionally, quantum efficiency (QE) is enhanced in the full wavelength range, especially 6.3% at 520 nm wavelength. This technique can not only be used in such BSI structures, but also adopted in an FSI pixel with any photodiode-type readout scheme.

Key words: backside illuminated CMOS image sensor; photodiode; full well capacity; quantum efficiency; small size pixel

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1. Introduction

Pixel shrinking is a common trend in image sensors used in all fields of consumer electronics, including digital still cameras, mobile imaging, internet-based video conferencing, and surveillance[1]. In mobile and digital still camera applications, 1.75 μm and 1.4 μm pixels are widely used in production, and with the use of backside illuminated (BSI) technology, further pixel size reduction to an extremely small 0.7 μm has been achieved[1, 2]. However, as pixel size continues to shrink，the design of such small size pixels is now facing some new limitations, including low dynamic range, low signal to noise ratio and low sensitivity. These limitations will definitely deteriorate the quality of imaging and decrease the detectable full range of illumination in reality. All of the limitations stated above could be simultaneously solved through increasing the full well capacity (FWC), which is the maximum amount of charges that can be accumulated on a photodiode capacitance[3], and is given by

$$Q_{PD} = C_{PD}(V_{pinning} - V_{blooming}), \quad (1)$$

where C_{PD} is the photodiode capacitance, $V_{pinning}$ is the maximum voltage that an N-type region of a PPD can reach in a fully depleted state, and $V_{blooming}$ is the minimum voltage when the electrons exceed the pixel's FWC.

Solutions about how to increase the FWC have been reported, such as the method of decreasing $V_{blooming}$ or increasing $V_{pinning}$. Decreasing $V_{blooming}$ includes a method that uses a negative voltage applied on the transfer transistor (TX) only when the TX is off[4]. This technique does play a remarkable role in improving well capacity, but this negative voltage is hard to be generated by using the periphery circuits. Generally speaking, $V_{pinning}$ will be proportionally enhanced with an increased N-type doping dose[5]. It does help to increase FWC too, but this may lead to some electrons remaining in the photodiode (PD), causing image lag to degrade the pixel's performance[6]. Therefore, if we want to ensure excellent image lag performance, we should not enhance FWC using this method.

From the discussion above, this paper studies the feasibility of increasing FWC through increasing the capacitance of a PD. Similar methods have also been proposed[7, 8]. They all increased FWC by using a new PPD structure, which stores electrons in two lateral stratified layers, which are connected by a vertical "bridge" region. However, this particular bridge region is sensitive to misalignment, which may cause different pixels to have different FWCs. In our work, taking this bridge region's negative effect into account, we propose a new reformed structure to increase the FWC of small size pixel. Perfect image lag performance is achieved when using the FWC extension. Furthermore, the quantum efficiency (QE) of the BSI pixel is also improved.

2. Concept description of the proposed PD

Since the BSI pixel is the driving force of pixel shrinking,

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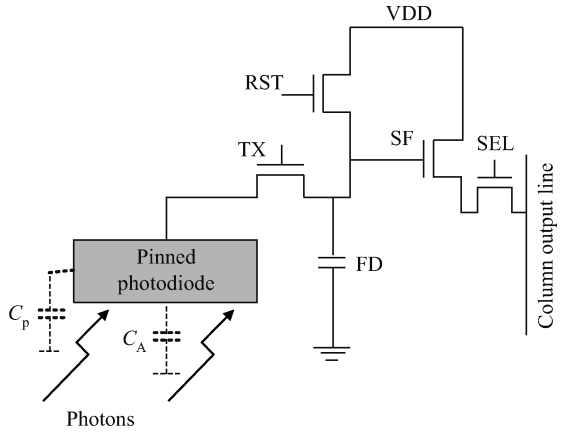

Fig. 1. Structure of a BSI CMOS 4-transistor pixel.

all small size pixel improvements in this paper are based on the original structure of a BSI CMOS 4-transistor pixel, as shown in Fig. 1. The structure includes a pinned photodiode (PPD), a transfer transistor (TX), a floating diffusor (FD), a source follower (SF), a reset transistor (RST), and a row select transistor (SEL). Compared with the original one, the optimized BSI PPD structure is achieved by using two main procedures: The first procedure is to form a depth stretched but doping gradient double N-type region to increase the side-wall capacitance of the PD. Secondly, in order to help this stretched double N-type region achieve full depletion, a new P type region is sequentially introduced after the double N region, which is the second procedure.

2.1. Double N-type region

In a PD-type CMOS APS pixel, a reverse-biased PN junction is used as the electron storage element. The FWC of the PD is directly determined by the total capacitance, which depends on bottom area junction capacitance and the side wall junction capacitance[9, 10] and is given by

$$C_{\mathrm{PD}} = C_{\mathrm{A}} A + C_{\mathrm{P}} P, \tag{2}$$

$$C_{\mathrm{A}}, C_{\mathrm{P}} = \sqrt{\frac{q\varepsilon_0\varepsilon_{\mathrm{si}}}{2}\frac{N_{\mathrm{A}}N_{\mathrm{D}}}{N_{\mathrm{A}}+N_{\mathrm{D}}}}\,(V_{\mathrm{bi}}-V)^{-\frac{1}{2}}, \tag{3}$$

where C_{A}, C_{P} are the unit area junction capacitances and unit peripheral junction capacitances; A, P are the top and bottom areas, and side wall areas of the photodiode region, respectively; V_{bi}, V are the built-in potential of photodiode and applied voltage, respectively; N_{A}, N_{D} are the doping concentration of P and N region, respectively; $\varepsilon_{\mathrm{si}}$, ε_0 are the dielectric constant of silicon and vacuum, respectively.

From the equation stated above, adopting a higher doping concentration of N_{D} is a conventional way to compensate the FWC reduction resulting from pixel shrinking, but this will result in image lag and random noise as the higher doping is not easy to be depleted by the periphery P region[11].

In this paper, the theory behind improving PD FWC in view of C_{PD} is that, if the PD region is restricted to a certain

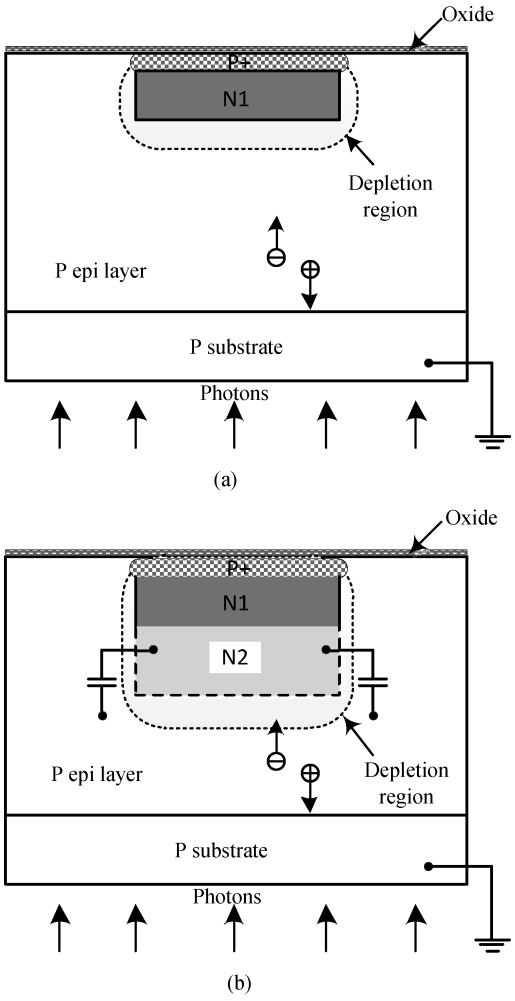

Fig. 2. Schematic of (a) the original PPD and (b) the double N-layer stretched PPD.

size, that is to say A_{top} will be unchanged, then the total capacitance of a PD could be increased by enlarging the vertical area of the N region in the substrate. The extended side-wall junction capacitances play an important role in collecting the photo-generated electrons near the edges of the PD. Thus, the FWC will be improved.

However, if the depth of an N-type region is extended by only implanting one high energy N-type impurity, this will make the extended N-region lack an obvious doping gradient, causing the electrons far from the TX gate become much more difficult to be transferred to FD node. This will result in image lag. So taking account of image lag, the optimized structure is implemented as shown in Fig. 2(b). After N-type region N1 is achieved in the same way as the one in Fig. 2(a), an additional N-type implant with a higher energy of 250 keV and with a lower dose is introduced, forming a second N-type doping region, N2, right below the N1 region to increase the side-wall capacitance of the PD. These successive two N-layers are formed with the same mask. The capacitances of the conventional region and the double N region are given by, respectively:

$$C_{\mathrm{PD}} = C_{\mathrm{A}}(A_{\mathrm{top}} + A_{\mathrm{bottom}}) + C_{\mathrm{P}} P, \tag{4}$$

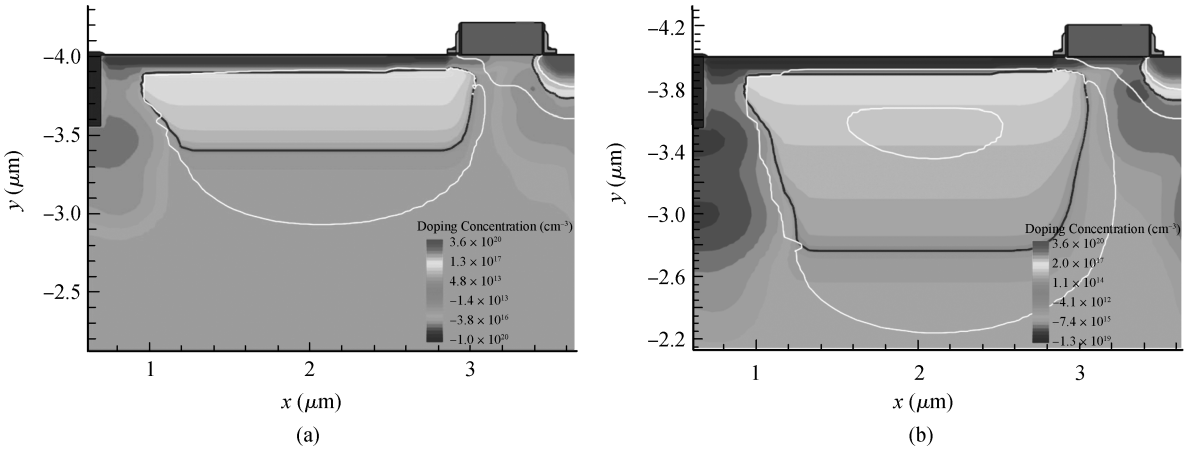

Fig. 3. Simulation structures of PPD (a) without the N2 region and (b) with the N2 region.

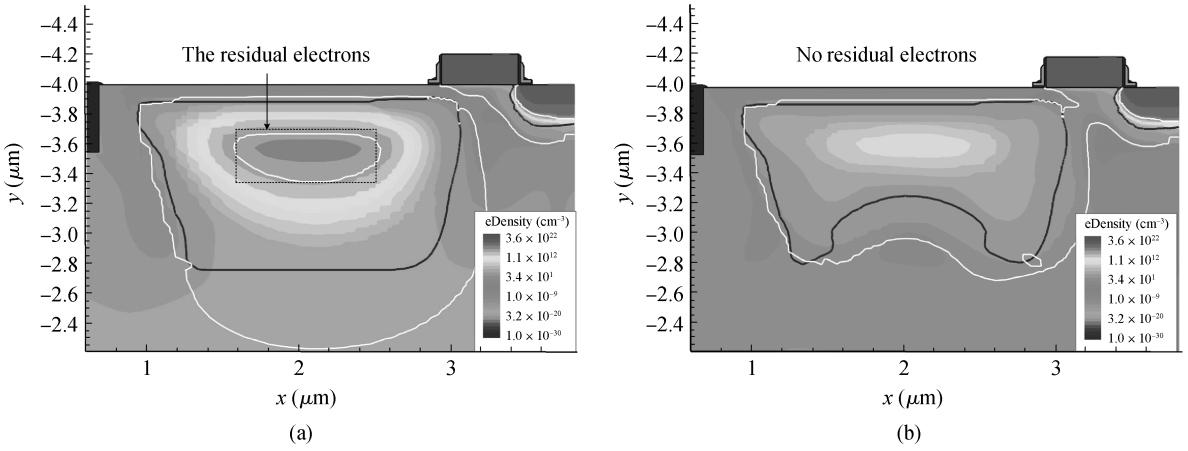

Fig. 4. Depletion performances of PPD structures (a) without the P-insertion region and (b) with the P-insertion region.

$$C'_{\mathrm{PD}} = (C_{\mathrm{A}} A_{\mathrm{top}} + C'_{\mathrm{A}} A'_{\mathrm{bottom}}) + [C_{\mathrm{P}} P + C'_{\mathrm{P}} \Delta P]. \quad (5)$$

The enhanced capacitance between these two structures is given by

$$\Delta C_{\mathrm{PD}} = C'_{\mathrm{PD}} - C_{\mathrm{PD}} = (C'_{\mathrm{A}} A'_{\mathrm{bottom}} - C_{\mathrm{A}} A_{\mathrm{bottom}}) + C'_{\mathrm{P}} \Delta P, \quad (6)$$

where A_{top} and A_{bottom} are the top and bottom areas of the PN junction, respectively; A'_{bottom} is the new bottom area of the stretched N region; C_{p} and C'_{p} are the unit side wall junction capacitances of the original and the stretched N region, respectively; P and ΔP are the conventional side wall areas and the increased side wall area, respectively.

As shown in Eq. (6), the improvement of overall capacitance is composed by two improvements: one comes from the stretched side wall areas and the other one comes from bottom capacitance variation. Since the difference between A_{bottom} and A'_{bottom} is so small that its contribution to the enhanced overall capacitance can be omitted, the improvement of FWC mainly results from the enlarged side wall area ΔP of the stretched N region.

Furthermore, from the simulation structures shown in Fig. 3, the depletion region can be expended to the backside so that QE of the stretched PPD will be optimized at the same time. This will be achieved by controlling the doping energy, which forms the N2 region. Since in the BSI pixel, the photons are projected from the backside surface of the substrate, the smaller the distance is between the depleted region and the backside surface, the more signal electrons will be collected, and the QE of the short and medium wavelength light will be improved more significantly. As the shallow-generated charge may diffuse laterally in the field-free substrate, giving rise to image blurring, this absorption of short wavelength light is also beneficial for reducing image blurring.

2.2. P-type insertion region

As stated above, extending the vertical side wall areas indeed increased FWC, however, it may cause only the outside circle of the extended double N-type region to be depleted, leaving the electrons in the inner circle of the double N-type region difficult to be depleted, as illustrated in Fig. 4(a), introducing serious random noise and image lag.

In this section, a P-insertion region is introduced into the double N-layer PPD structure to help the N region achieve full depletion and increase the available FWC once again. This P-insertion region is implemented by using two high energy P^+ doping implants. The drawing in Fig. 5 shows the schematic of the P-insertion double N-layer PD, called "P-insertion PD" for

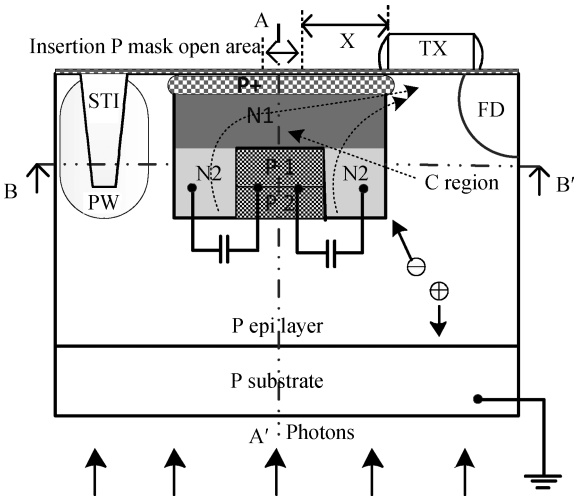

Fig. 5. Schematic of the P-insertion photodiode.

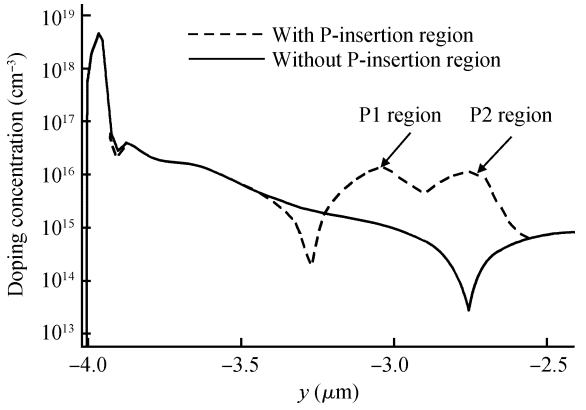

Fig. 6. Doping concentration profiles of the P-insertion PPD and the double N PPD at AA′ cross section.

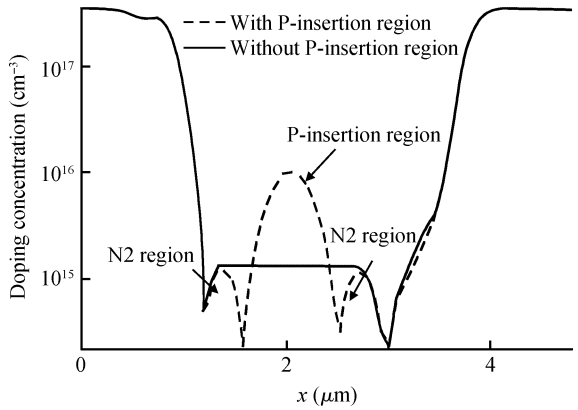

Fig. 7. Doping concentration profiles of the P-insertion PPD and the double N PPD at the BB′ cross section.

short below.

In this P-insertion PD, the front surface is covered with a high P^+ doping concentration layer, it is essential to reduce the dark current generated from the Si–SiO_2 interface state. After an N region is formed to be a depth stretched double N region as stated previously, two step P-type implants with different doping energies are sequentially implanted to form a new P-insertion region along the vertical direction. This vertical insertion P region is implanted using an additional mask. The new mask is located above the underlying double N region, and the mask has an open window of 0.20 μm, which is at a distance x from TX gate, as shown in Fig. 5. Since the implanted P-type impurity BF_2 will diffuse around after annealing, the distance X and the distance 0.20 μm are all optimized to ensure that the new N2 region is not be eaten up by this diffused P-insertion region, and to ensure there are enough N2 bottom areas to collect photo-generated electrons.

In order to plug this P-insertion region into the interior of the new stretched N region, the P vertical region is implemented by two energy P-type implants, respectively forming a P1 region and a P2 region, as shown in Fig. 5. The doping concentration of this P-insertion PPD along the AA′ and BB′ cross sections are respectively shown in Figs. 6 and 7. The P1 region is achieved by using a high energy BF_2 implant in which the energy is 1400–1800 keV with a medium doping dose, this step is essential to guarantee that the P-insertion region is at the core of the N region and achieve enough PN junction side wall areas, as illustrated in Fig. 5. Secondly, the P2 region is achieved by one higher energy of 2200–2600 keV with the same doping dose of BF_2 impurity, making the P2 region be implanted deeper, locating at the boundary between the substrate and N2 region. This is to ensure that the whole P insertion region has the same electrical potential as the substrate, avoiding the electrical potential of P1 region floating, because this could make the whole P-insertion region essentially act as an electrode between the two N2 region[8].

The P insertion region plays two important roles. The first role is to improve FWC through increasing C_{PD}, because this P insertion region can generate two extra inner side walls to further increase the overall side wall areas to increase C_{PD}, as shown in Fig. 5. The second and most important role is that this vertical insertion P region could be inserted into the inner core of the N1 and N2 regions to help residual electrons achieve full depletion. The residual electrons, which once remained in the C region in considerable numbers, are all depleted after adopting the P-insertion region, just as the depletion performances compared in Fig. 4. So the image lag performance of this P-insertion PPD structure could achieve excellent results, which is discussed in the next section.

Due to the new P-insertion location, the influence on FWC—coming from the mask misalignment which is particularly likely to occur in the stratified PPD[7, 8]—can be reduced in our structure. Because our new P-insertion region is implanted from the narrow window located at the middle of the PPD, the most sensitive factor to misalignment is changed to the depth of the C region rather than the lateral width of the bridge region, as in previous stratified structures. The lateral width will be affected by misalignment, but the depth of the C region will be only affected by the doping energy of the P1 region, which is easily adjusted.

A layout design is displayed in Fig. 8. In each of the pixels, thanks to the compact layout, the proposed P-insertion PPD can be integrated with the TX, RST, SF and SEL transistors together after successive processes. The P-insertion region is located in the middle of the PD, and the AA′ cross-section along

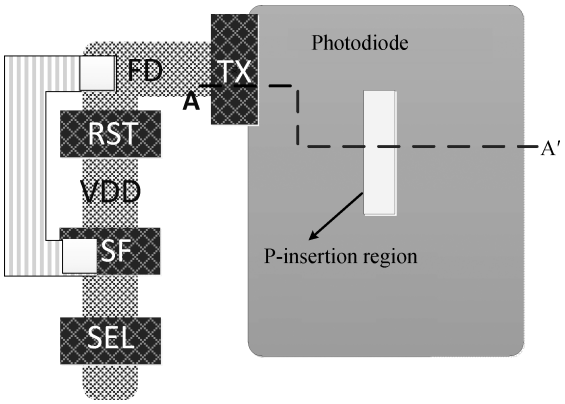

Fig. 8. Layout of the proposed P-insertion PPD pixel.

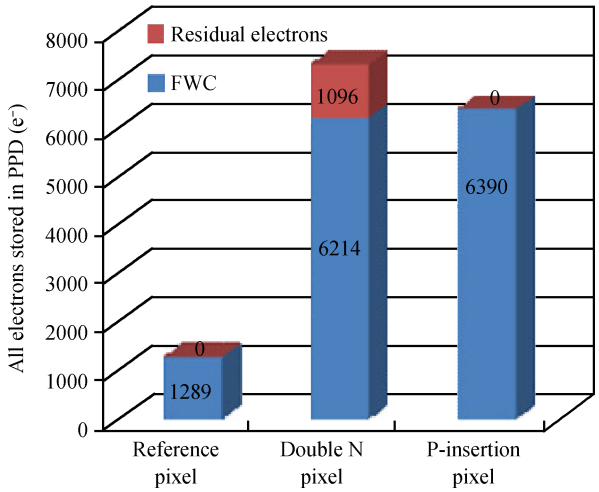

Fig. 9. Electron stored in reference pixel, double N pixel, and P-insertion pixel.

the layout can be well illustrated by the simulated structure, as shown in Fig. 4(b), in which the simulated width of the PPD is 1 μm rather than the width stated in Fig. 8.

3. Simulation results and discussion

Device models are developed to simulate photon injection, electron collection, transfer and reset for evaluating FWC, QE, and the image lag of these three structures. Figure 3(a) is the original reference structure model, Figure 3(b) is the double N buried layer structure model, while Figure 4(b) is the device model for the proposed P-insertion structure.

The device models used for the simulation are based on a 0.18-μm CMOS process. The operating voltage is 3.3 V. In these three structures, the simulations were based on a small sized pixel in which the PPD size is 2.0 × 1.0 μm^2, the size of active region is 4.8 × 1 μm^2, and the length of the transfer gate is 500 nm. The row select transistor and source follower transistor are both removed from the pixel structure as they do not affect photon conversion and collection[12].

3.1. Pixel FWC

For the measurement of these three structures' FWC, the integration time is set to $T_{\rm int}$ = 10 μs, the incident beam intensity is set to 2.89 × 10^{16} photons/(cm^2·s). It has been tested and shown that this strong incident beam intensity in the integration time can provide enough electrons to fill the capacity to full. The total electron quantities before and after light integration in the collecting region are extracted respectively from the original structure, the double N structure, and the P-insertion structure.

In order to prove that the enhanced FWC is indeed from the increase of $C_{\rm PD}$, the capacitances and FWC were respectively extracted from the original PPD and the proposed P-insertion PPD, the results are shown in Table 2 and Fig. 9. It was observed that the $C_{\rm PD}$ of the P-insertion structure increased by 3.25 times compared with the original capacitance, and the FWC achieves a 395.8% improvement as the result. This phenomenon indicates that the increased FWC does result from the improvement of the PD capacitance, and proves the idea's feasibility—to increase FWC by increasing PD capacitance.

The simulation results in Fig. 9 show the comparison of these three structures' FWC. For the original pixel, there are only 1289 electrons stored in the collecting region, all of these electrons are completely transferred to the FD node, contributing to FWC and leaving far smaller than one electron in the PPD. In the double N pixel, although the collected electrons obviously increase to 7310e–, there are only 6214 electrons contributing to FWC, leaving more than 1096 electrons in the PPD as a source of image lag. In the P-insertion PPD pixel, although 6390e– is less than 7310e– in the double N pixel, all of these could contributed to FWC. The FWC has achieved great improvement over 395.8%, higher than the original pixel's 1289e– FWC. Comparing the FWC of the double N pixel with the P-insertion pixel in Fig. 9, there is an improvement from 6214e– to 6390e–. This improvement could be explained by the contribution coming from the P-insertion's inner side walls.

3.2. Image lag

At the same time, image lag was also optimized to a perfect low level, this achievement is attributed to adopting a P-insertion region, because this P-insertion could help the residual electrons achieve full depletion, leaving no residual electrons to cause image lag. Figure 10 shows the residual electron density after reading out operation along the AA' cross-section, the maximum electron density in PPD drops by more than 6 orders from 6.6 × 10^{15} to 2.14 × 10^9 cm^{-3}, which achieves the same order of residual electron density as the original pixel.

To further prove the image lag performance of the P-insertion pixel, we expose the pixel once for 10 μs and output four frames successively. The voltage variations on the FD region before and after correlated double sampling (CDS) operation are extracted respectively from the double N pixel and the P-insertion pixel. This voltage variation could illustrate whether all of electrons stored in the PPD have been transferred. From Table 1, in the double N pixel, there was still 0.0322 V voltage outputted after the first frame, that is to say, there are residual electrons remaining in double N pixel after the first time reading out, this is the image lag; while in the P-insertion pixel, after the first frame operation, no CDS signals were obtained in the second and the next frame. That means, with the P-insertion region, the P-insertion structure achieves

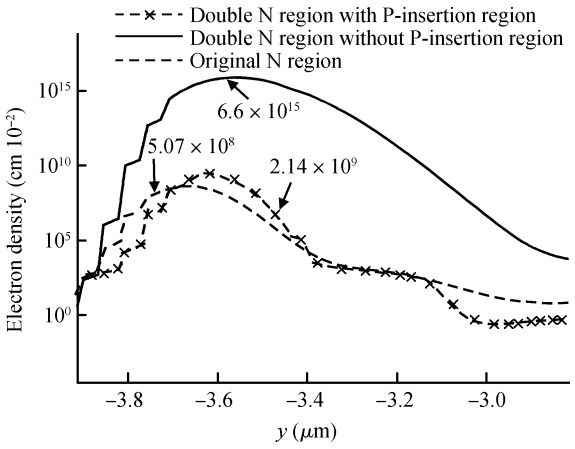

Fig. 10. Residual electron density after a reading out operation along the AA′ cross-section.

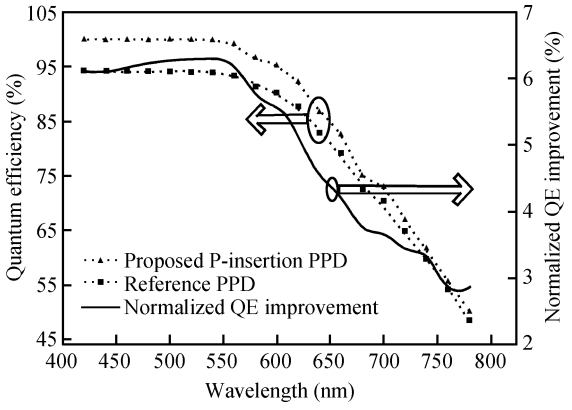

Fig. 11. Quantum efficiency improvement comparing the proposed PPD with reference PPD.

Table 1. CDS study to illustrate image lag.

Frame	CDS signal (V)	
	Double N pixel	P-insertion pixel
1st	1.0251	0.84154
2nd	0.0322	0
3rd	0.0107	0
4th	0.0065	0

total depletion without any image lag.

3.3. Quantum efficiencies (QE)

Quantum efficiencies of the original PPD and P-insertion PPD under the same simulation conditions were performed, and wavelength range was varied from 420 to 780 nm, with 20-nm steps. The QE, which is simulated as the inner quantum efficiency, the loss of incidental light by the flection of lens could not be taken into account in the model. Since in the BSI structure, the electrons need to get through the collection region before being recombined. The thickness of the silicon base could influence QE. So the substrate thinning process should be considered. The simulated thickness of the silicon base is the thickness having taken this into account.

QE simulation results for the reference and P-insertion PPD are illustrated in Fig. 11. As shown, QE improvement was observed in the proposed PPD at a full range of wavelengths. The most obvious improvement—more than 6.3%—was achieved at the wavelength of 520 nm, while the QE of deep-penetrating photons did not increase as much as the blue photons generated in the surface. This phenomenon has a good match with the theoretical analysis. It is because the depletion region is expended to the photon-injected surface, which is more effective at collecting blue and green electrons. By increasing the thickness of the silicon substrate to prolong the collection region for a long wavelength, a better improvement for QE at a long wavelength would be achieved.

3.4. Others

The dynamic range is defined as the ratio of the maximum well capacity to the electrons accumulated by the minimal illumination which could be detected[13]. The larger the FWC, the wider the dynamic range will be. Assuming that the minimal illumination would not be changed, this proposed P-insertion PPD could achieve a dynamic range extension of 17.9 dB, compared with the reference pixel thanks to the FWC's extension.

The comparison of the performance between the original PPD and the proposed P-insertion PPD are shown in Table 2. Parameter comparisons of the proposed PPD and Ref. [7] are summarized in Table 3. In order to compare with Ref. [7] at the same condition, we multiply the FWC 6390e– by 2.2, because 6390e– is the simulated result based on the width of PD is 1 μm, while the layout size is 2.2 μm, so that the actual FWC is 14058e–. In Table 3, by comparing we could find that the FWC has achieved the same level found in Ref. [7], and the FWC increment and the QE increment are both much better than that stated in Ref. [7]. The image lag performance has been optimized to a perfect level in this paper, while this parameter was not presented in Ref. [7].

The high energy doping implant in the proposed pixel may induce extra lattice defects in a silicon body, but this could be almost eliminated by successive multi-step annealing. Even though there are less residue defects, we could adopt a widely used technique to subtract dark current by adding several rows of dark pixels behind the pixel array, these addition pixels are fabricated by using the same pixel array process, so that the dark current in these pixels is similar. After reading out the signals and subtracting them, it could be effective in eliminating its influence.

As shown in Table 2, the maximum voltage swing of the proposed PPD decreases a little. Because in order to preserve the excellent image lag performance, the maximum voltage swing on the FD node is reduced by 0.295 V as V_{pinning} increases from 0.678 to 0.973 V. Further measures to decrease V_{pinning} are expected to be achieved in the next step. Furthermore, we want to evaluate the effect of a multi P-insertion region structure on improving a pixel's FWC in the next step. Three dimensional simulations could provide more desired results.

4. Conclusion

To increase a small size BSI pixel's FWC and optimize QE, a new PPD structure was proposed and evaluated. In this

Table 2. Comparison of the performance of the original PPD and proposed P-insertion PPD.

Parameter	Original PPD	Proposed P-insertion PPD	Change	Unit
PD area	2×1	2×1	–	μm^2
Full well capacity	1289	6390	395.8 × increase	e–
$V_{pinning}$	0.678	0.973	0.295 × increase	V
$V_{blooming}$	0.097	0.087	0.01 × decrease	V
C_{PD}	354.9	1153.9	325.1 × increase	pF
QE @ 420 nm	94.225	99.98	6.105	%
@ 560 nm	93.356	99.1335	6.189	%
@ 780 nm	48.489	50.0090	3.136	%
@ peak (520 nm)	93.993	99.9142	6.3	%
Image lag	< 1	0	–	‰

Table 3. Comparison of the performance of the PPD in Ref. [7] and the proposed PPD.

Parameter	Proposed	IISW 07's
Process	0.18 μm CMOS	0.13 μm CMOS
PD area (μm^2)	2×2.2	1.6×2.2
FWC*	14058e–	14600e–
FWC increment (%)	395.8	48.9
$V_{pinning}$ (V)	0.973	0.9
QE increment (%)	6.105 @ 420 nm	1 @ 420 nm
	6.189 @ 560 nm	2 @ 560 nm
	3.136 @ 780 nm	3 @ 780 nm
Image lag	0	NA

* It should be pointed out that the FWC in Table 3 is 14058e– rather than 6390e– because the 6390e– is the simulated result based on PD width of 1 μm, while in reality, the layout size is 2.2 μm, so that the layout FWC should be 14058e–.

method, electrons are stored in the original and stretched N region, and the P-insertion region is inserted into the interior of this new stretched N region to help the increased electrons deplete. Simulation results are consistent with the theoretical analysis. The FWC is increased from 1289 electrons to 6390 electrons, due to the side wall capacitance extension. In addition, the QE improves at full range of wavelength, especially achieving 6.3% improvement @ 520 nm. Furthermore, the image lag performance is preserved at a perfect low level after all of these optimizations. As a result, the proposed method was proven to be a useful solution, which could significantly improve FWC to overcome the limitations of a small size pixel, without any degradation of image lag performance.

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