CMOS analog baseband circuitry for an IEEE 802.11 b/g/n WLAN transceiver

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Abstract: An analog baseband circuit for a direct conversion wireless local area network (WLAN) transceiver in a standard 0.13-μm CMOS occupying 1.26 mm^2 is presented. The circuit consists of active-RC receiver (RX) 4th order elliptic lowpass filters (LPFs), transmitter (TX) 3rd order Chebyshev LPFs, RX programmable gain amplifiers (PGAs) with DC offset cancellation (DCOC) servo loops, and on-chip output buffers. The RX baseband gain can be programmed in the range of –11 to 49 dB in 2 dB steps with 50–30.2 nV/$\sqrt{\text{Hz}}$ input referred noise (IRN) and a 21 to –41 dBm in-band 3rd order interception point (IIP3). The RX/TX LPF cutoff frequencies can be switched between 5 MHz, 10 MHz, and 20 MHz to fulfill the multimode 802.11b/g/n requirements. The TX baseband gain of the I/Q paths are tuned separately from –1.6 to 0.9 dB in 0.1 dB steps to calibrate TX I/Q gain mismatches. By using an identical integrator based elliptic filter synthesis method together with global compensation applied to the LPF capacitor array, the power consumption of the RX LPF is considerably reduced and the proposed chip draws 26.8 mA/8 mA by the RX/TX baseband paths from a 1.2 V supply.

Key words: WLAN; analog baseband; active-RC filters; PGA; DCOC; operational amplifiers
DOI: 10.1088/1674-4926/33/11/115001 **EEACC:** 2570

1. Introduction

In recent years, with the rapid growth of the deployment of WLANs in offices, homes and hot spots, numerous single-mode WLAN transceivers have been reported[1, 2]. The proliferation of multiple WLAN standards (IEEE 802.11a/b/g/n) coupled with the increasing demand for portable applications suitable for battery-operated handheld devices has created the need for low-cost low-power multimode integrated transceivers[3, 4] that can provide mobile users with seamless connectivity when they roam between access points operating with different WLAN standards. Among these standards, the 802.11b standard ratified in 1999 and the 802.11g ratified in 2003 share the same three non-overlapping channels in the same 2.4-GHz ISM operation band, the 802.11g standard can provide either a high data rate of the 802.11a when operating in the orthogonal frequency-division multiplexing (OFDM) mode with data rates of 6–54 Mb/s or 802.11b compatibility when operating in the direct sequence spread spectrum (DSSS)/ complementary code keying (CCK) mode with data rates of 1–11 Mb/s. Ratified in 2009, the 802.11n standard can provide increased data rate, robustness, and range while occupying the same 20 or 40 MHz signal bandwidth as the legacy 802.11a/b/g WLAN by adding multiple-input multiple-output (MIMO) antennas to employ spatial diversity.

This paper describes a fully integrated analog baseband circuit of a direct conversion 2.4 GHz ISM band CMOS transceiver (Fig. 1) in compliance with the IEEE 802.11b/g/n standards. In Fig. 1, when switches SW_5, SW_6 are on, switches SW_3, SW_4 are turned-off and the TX filters and the RX output buffers provide a filter bandwidth calibration path. When switch SW_2 is turned on, the power detector (PD) measures the TX Up mixer's output of I or Q path and feeds the signal back to the RX baseband input to accomplish TX I/Q magnitude and phase calibrations. Switch SW_1 bridges the TX mixer output and the RX mixer input to calibrate the RX I/Q paths. All of the calibration processes mentioned above are carried on with the help of a digital baseband chip following the orders as: 1. filter bandwidth calibration; 2. TX I/Q calibration; 3. RX I/Q calibration. The proposed analog baseband provides the functions of RX/TX channel selection, signal amplification as well as signal paths for RX/TX calibration by circuit building blocks including I/Q channel selection filters, PGAs with DCOC servo loops, output buffers in the receiver path, and I/Q smoothing filters in the transmitter path.

2. Circuit implementation

2.1. RX/TX filters

The RX/TX filters are built with active-RC integrators for high linearity requirements with their 3-dB bandwidth being selected from 5 MHz, 10 MHz, and 20 MHz to cover the specifications of 802.11b/g/n WLANs. In the receiver path, a 4th order elliptic LPF prototype is chosen to band-limit the ADC input and optimize its dynamic range. Since no other filter of equal order has a sharper transition region than elliptic filters, for given stop-band attenuation specification, an elliptic filter of lower order is the best choice to maximize RX sensitivity and minimize the required dynamic range of RX ADCs with lowest power consumption and smallest die size. However, the highly spread capacitors required by elliptic filters greatly complicate the design with regard to filter frequency response ac-

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Received 1 May 2012, revised manuscript received 22 May 2012

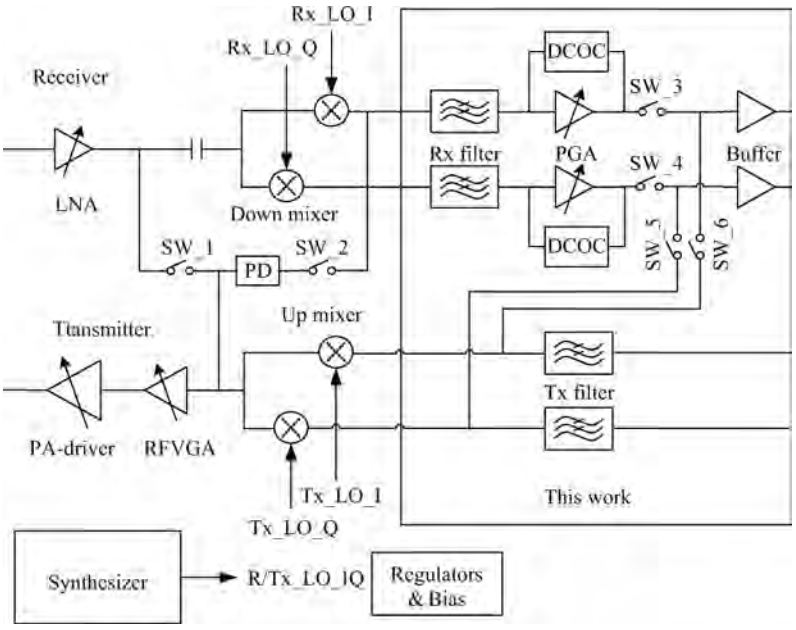

Fig. 1. Transceiver block diagram.

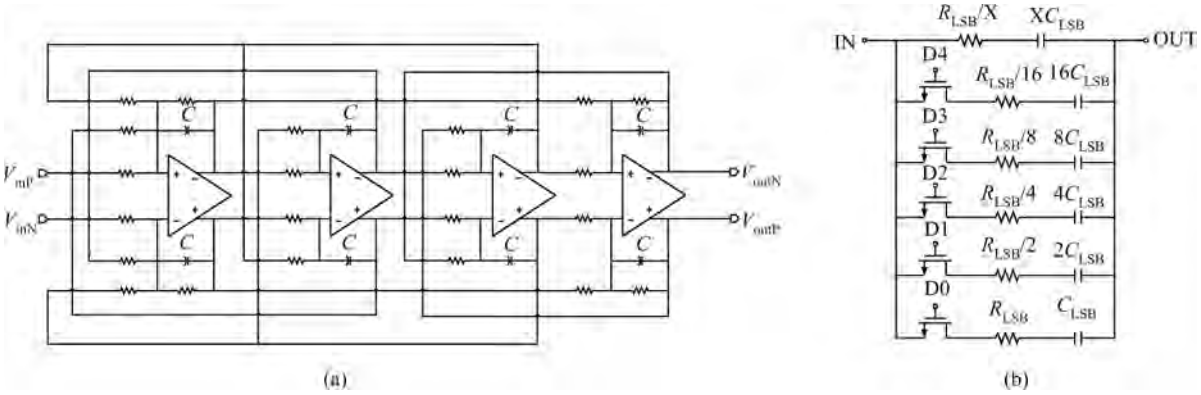

Fig. 2. (a) 4th order Elliptic lowpass filter for RX channel selection and (b) capacitor array for filter frequency tuning.

curacies over wide bandwidth tuning ranges.

In this design, a "zero capacitor spreading" method[5] is taken to synthesize the RX filter with identical integrators, as shown in Fig. 2(a). Using identical capacitor arrays makes wide range bandwidth programming/tuning easier to implement and filter realization more precise. Moreover, due to the elimination of the derivative capacitors which feed the signal back to the op-amp input, global integrator compensation as shown in Fig. 2(b) can be applied by adding a zero to the non-ideal integrator transfer function. The impedance of this capacitor array can be calculated as:

$$Z(s) = 1 + sR_{\mathrm{LSB}}C_{\mathrm{LSB}} \times \Big[s(C_0 + D_{N-1}2^{N-1}C_{\mathrm{LSB}} + D_{N-2}2^{N-2}C_{\mathrm{LSB}} + \cdots + D_1 2C_{\mathrm{LSB}} + D_0 C_{\mathrm{LSB}})\Big]^{-1}. \quad (1)$$

By making the frequency of the zero in array impedance, $1/R_{\mathrm{LSB}}C_{\mathrm{LSB}}$, equal to the filter op-amp unit bandwidth frequency (UGF) ω_{u}, a finite op-amp ω_{u} ideally exerts no effect on the integrator transfer function, which can save further power by choosing a smaller ω_{u}.

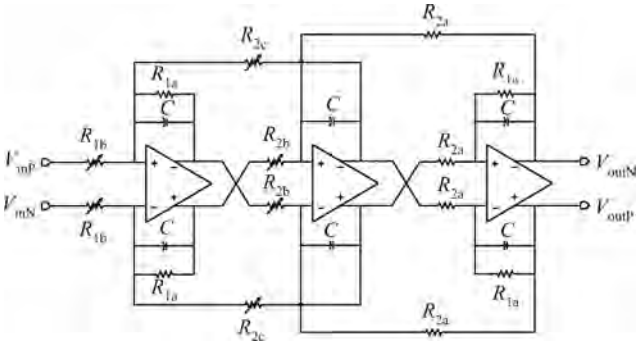

Fig. 3. 3rd order Chebyshev TX lowpass filter.

To reject the signal image generated by the DAC and meet the TX spectrum mask, a 3rd order active-RC Chebyshev LPF topology is chosen as a smoothing filter, as shown in Fig. 3. The

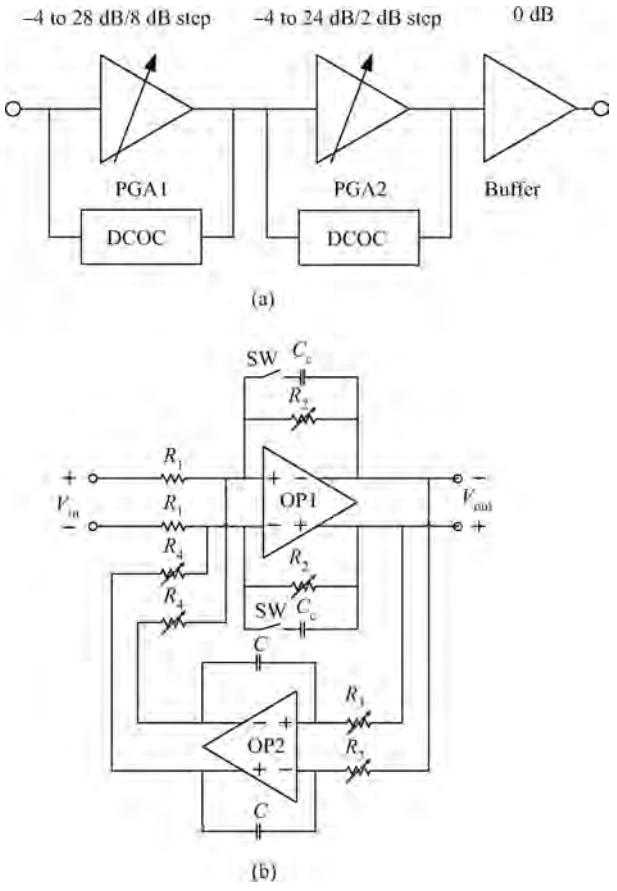

Fig. 4. (a) PGA topology with DCOC servo loops and (b) fully differential implementation of a single-stage PGA with a DCOC feedback loop.

resistor array R_{1b}, R_{2b}, R_{2c} can be tuned separately in 2.5 dB range by a 0.1 dB fine step in I/Q paths to achieve TX magnitude mismatch calibration. More specifically, resistor array R_{1b} implements 0.5 dB coarse tuning step while R_{2b}, R_{2c} are tuned in opposite directions to finely tune the LPF gain in 0.1 dB step.

2.2. PGAs and buffers

The op-amp based PGAs and output buffer stages are shown in Fig. 4(a). The 1st PGA implements coarse step gain tuning with an 8 dB step from –4 to 28 dB while the 2nd PGA finely tunes its voltage gain by a 2 dB step from –4 to 24 dB. The fully differential implementation of each PGA stage with its DCOC servo loop is shown in Fig. 4(b). The transfer function of the PGA stage at low frequencies can be approximated as:

$$T(s) \cong G_{\mathrm{DC}} \frac{1 + s/\omega_0}{1 + s/\omega_{\mathrm{P}}}, \tag{2}$$

$$G_{\mathrm{DC}} \cong \frac{R_4}{R_1} \frac{1}{A_2}, \tag{3}$$

$$\omega_0 \cong \frac{1}{A_2 R_3 C}, \quad \omega_{\mathrm{P}} \cong \frac{R_2}{R_4} \frac{1}{R_3 C} = \frac{R_2}{R_4} \frac{A_2}{\omega_0}, \tag{4}$$

where G_{DC}, ω_0, ω_{P} and A_2 stands for the DC rejection, zero and pole frequency of PGA stage at low frequencies, and the open loop gain of OP2, respectively. Here, R_4 is tuned in proportion to R_2 when the PGA gain is changed to make the 3-dB highpass frequency, i.e., ω_{P} constant and independent of PGA gain guarantees signal spectrum integrity. R_3 can be set to two different levels to fix this highpass frequency either to 700 kHz during the automatic gain control (AGC) tuning stage to make the RX baseband chain settle faster or to 10 kHz during the signal receiving stage to prevent any channel from highpass filtering. Moreover, capacitor C_{C} is applied by turning on the SW switches on when the corresponding PGA stage is set to low gain to guarantee stability by adding a global zero in the amplifier transfer function. When the PGA is set to high gain, the corresponding feedback factor determined by resistor ratio is low and the PGA is inherently more stable, these parallel capacitors are then detached from the PGAs in this high gain mode to achieve higher overall bandwidth.

The output buffer has 0 dB voltage gain. In total, the baseband chain can achieve a –8 to 52 dB gain range with 2 dB step. In this op-amp based structure, the PGA and buffer voltage gains are determined by on-chip resistor ratios, which can be made very accurate monolithically.

2.3. Op-amps

The op-amps used in the RX/TX filters and RX PGAs have the topology (shown in Fig. 5(a)) of a prevalent two-state structure to achieve large DC gain and large output swing simultaneously. C_{M} is applied as a Miller compensation capacitor, R_{Z} is used for canceling the right half plane (RHP) zero. Transistor M2a,b in parallel with the input pair M1a,b are added to suppress large input common-mode (CM) interferences. Auxiliary input pair M1c,d helps to form a common-mode feed forward (CMFF) path to improve the op-amp common-mode rejection ratio (CMRR) especially at high frequencies. In the left-most part of this figure, the common-mode amplifier constructed by the transconductor built with M5a,b and R_{S} compares the output CM voltage with the CM reference V_{CM}, amplifies and feeds the result back to current sources M3c,d to stabilize the output CM voltages.

The output buffers utilize op-amps with class-AB output stages (as illustrated in Fig. 5(b)) to enhance the output current drive capabilities. Based on the small signal equivalent circuit shown in Fig. 6(a), the op-amp has an equivalent small signal transconductor of:

$$G_{\mathrm{m}} = g_{\mathrm{m1}} + g_{\mathrm{m2}} \frac{1}{g_{\mathrm{m5}}} g_{\mathrm{m3}} \frac{1}{g_{\mathrm{m6}}} g_{\mathrm{m4}} \frac{1}{1 + s\dfrac{c_2}{g_{\mathrm{m5}}}} \frac{1}{1 + s\dfrac{c_3}{g_{\mathrm{m6}}}}, \tag{5}$$

where g_{m1}, g_{m2}, g_{m3}, g_{m4}, g_{m5}, g_{m6}, c_2, c_3 stands for the transconductance of transistor M4a, M4c，M9a, M8a, M10a, M8c and the total parasitic capacitance at the transistor M4c, M9a drain node. From Eq. (5), the two added poles of the class-AB op-amp transconductor situate at high frequency at the order of devices' f_{T}, their effects on the op-amp's frequency responses can thus be ignored.

Figure 6(b) illustrates the large signal equivalent circuit of the output stage, in which a CMOS translinear loop is formed by M11a, M11b, M10a, M9a with equal W/L ratio K.

Given: $(\frac{W}{L})_{\mathrm{M4c}}/(\frac{W}{L})_{\mathrm{M4a}} = (\frac{W}{L})_{\mathrm{M8c}}/(\frac{W}{L})_{\mathrm{M8a}} = N$, it follows that:

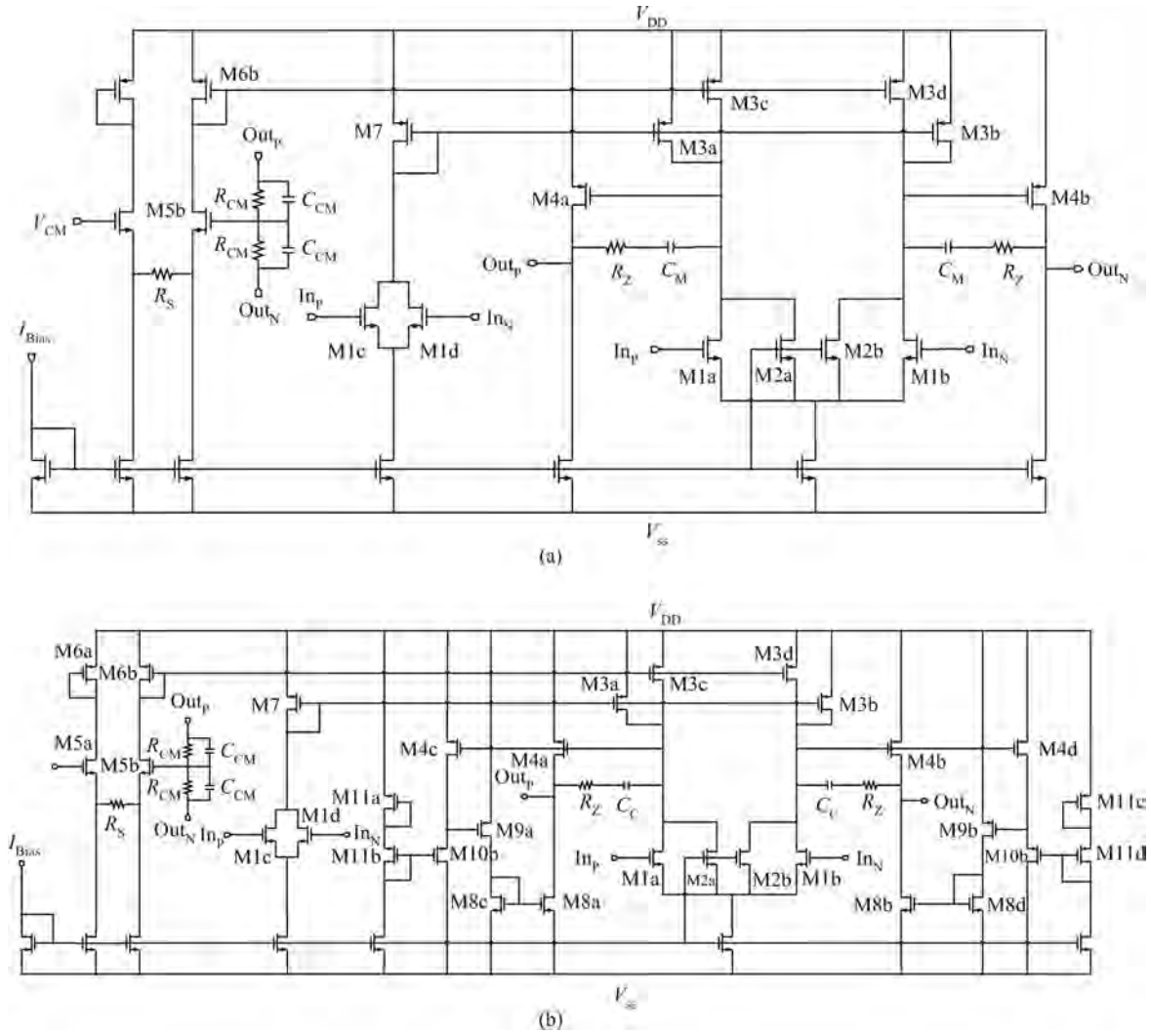

Fig. 5. (a) 2-stage op-amp and (b) 2-stage op-amp with a class-AB output stage.

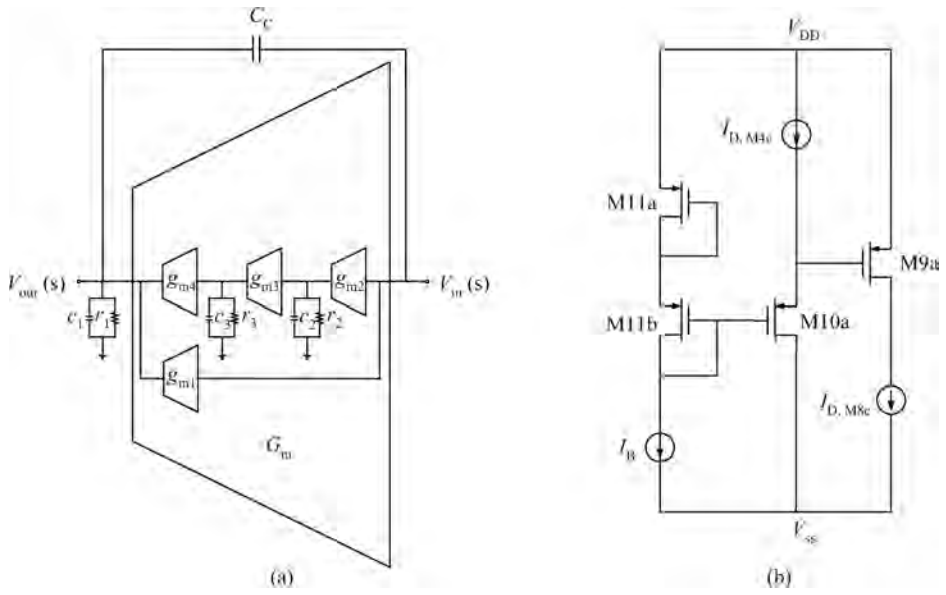

Fig. 6. (a) Small-signal equivalent circuit of the op-amp with a class-AB output stage and (b) large-signal equivalent circuit of its output stage.

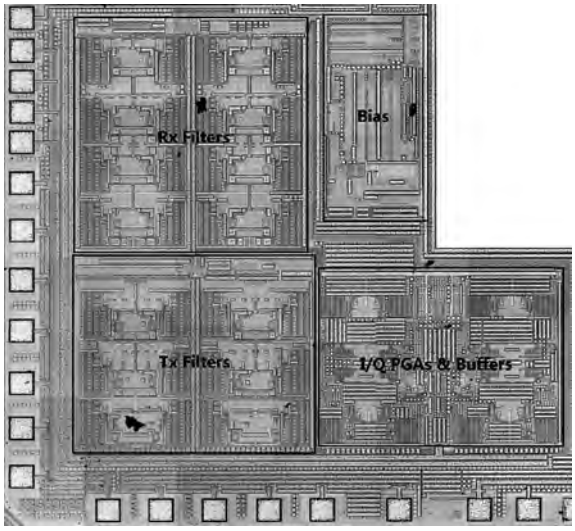

Fig. 7. Die photograph.

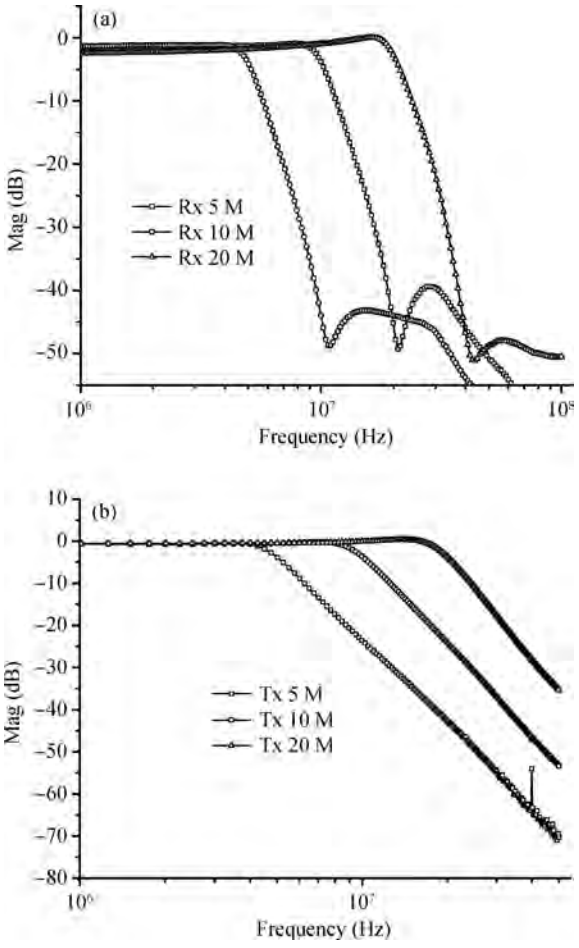

Fig. 8. Measured RX LPF (a) and TX LPF (b) transfer function.

$$2\sqrt{\frac{I_{\mathrm{B}}}{K}} = \sqrt{\frac{I_{\mathrm{push}}/N}{K}} + \sqrt{\frac{I_{\mathrm{pull}}/N}{K}}, \qquad (6)$$

where I_{push}, I_{pull} stand for the output transient push/pull current, respectively.

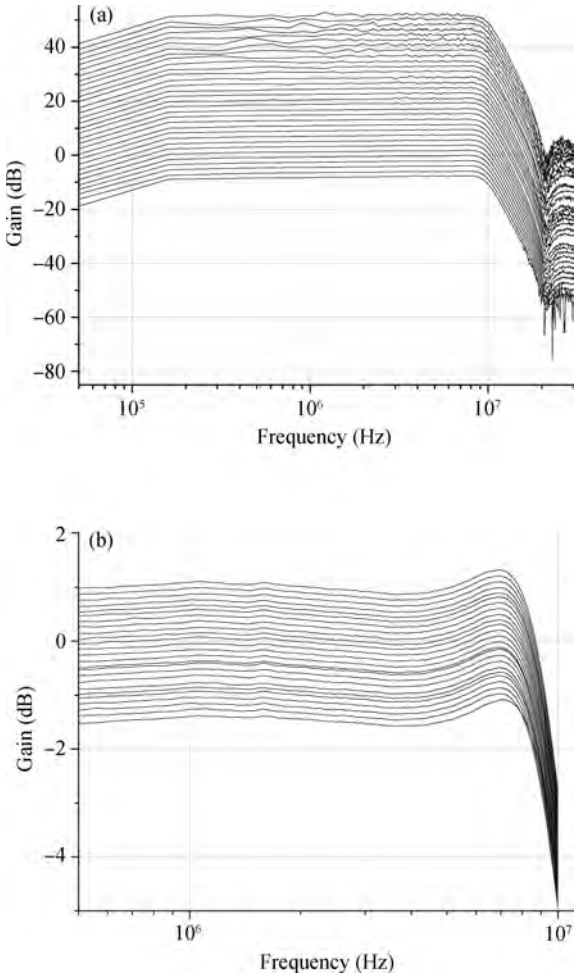

Fig. 9. Measured programmable frequency responses of the RX baseband (a) and TX baseband (b) with gain tuning.

3. Experimental results

The proposed WLAN transceiver analog baseband circuit is fabricated in a standard 0.13-μm CMOS process. Its die photograph is shown in Fig. 7 with the active area of 1.26 mm^2 occupied by I/Q RX/TX LPFs, RX PGAs, output buffers and bias circuits. The I/Q RX/TX baseband channels consume 26.8 mA/8 mA from a 1.2 V supply in total.

Figure 8 illustrates the measured RX/TX LPF frequency responses with 5 MHz, 10 MHz and 20 MHz 3-dB cut-off frequencies. Figure 9 shows the RX/TX baseband frequency responses at different gain levels, from which it can be concluded that the RX baseband gain can be varied from –11 to 49 dB with a 2 dB step and the gain of TX baseband I/Q paths can be tuned separately with a 0.1 dB fine step from –1.6 to 0.9 dB. The slightly lower RX baseband chain voltage gain compared to simulation results is attributed to the off-chip buffer loss of –2.4 dB.

The output noise spectrum of the RX/TX baseband is measured by connecting the device under test (DUT) output to a spectrum analyzer through the same off-chip buffer with –2.4 dB voltage gain, as shown in Fig. 10. It can be calculated that the noise figure at 1 MHz of RX baseband with maximum gain and the TX baseband is measured to be 30.6 dB and 31.9 dB, respectively, when referring to 50 Ω source

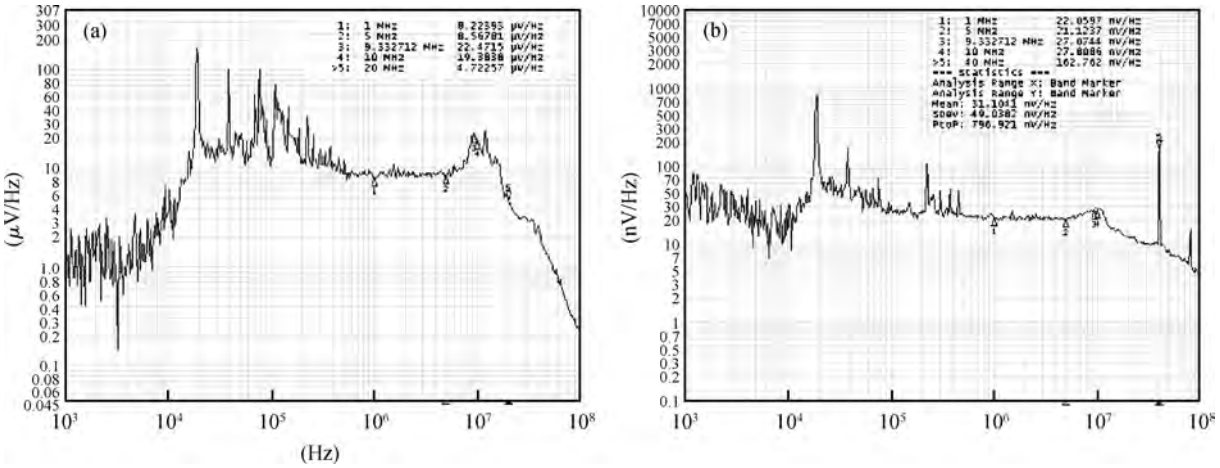

Fig. 10. (a) Measured output noise spectrum of the RX baseband at its maximum gain and (b) measured output noise spectrum of the TX baseband.

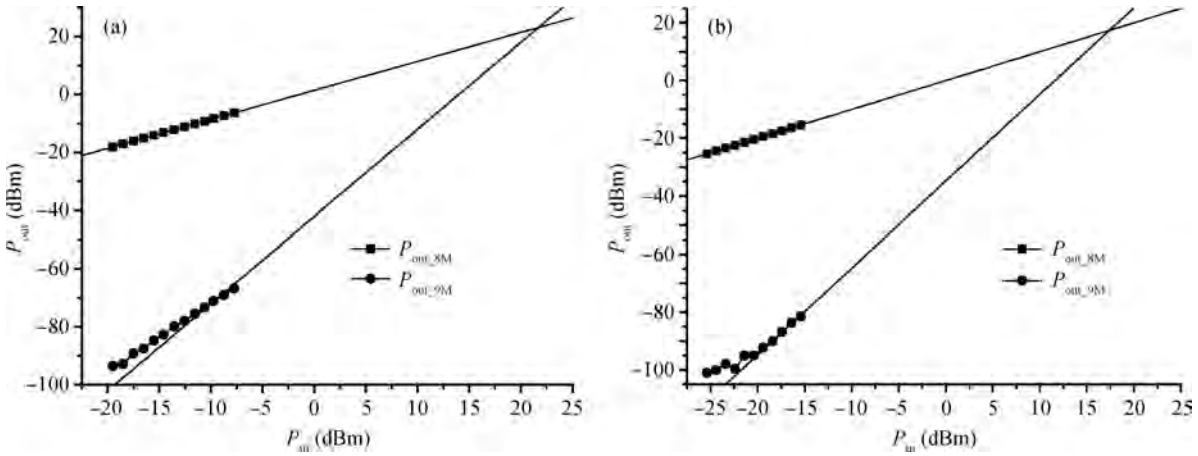

Fig. 11. (a) Measured IIP3 of RX baseband at its minimum gain and (b) measured IIP3 of the TX baseband.

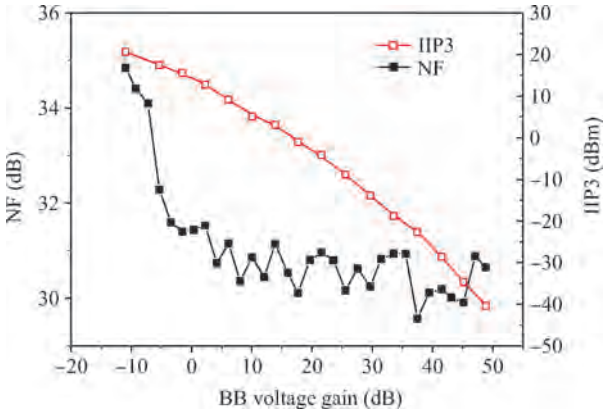

Fig. 12. Measured receiver analog baseband noise figure and IIP3 with respect to its voltage gain.

impedances.

The measured IIP3 of the RX/TX baseband circuit with the lowpass 3-dB cut-off frequency set to 10 MHz and input 2-tones at 7 MHz and 8 MHz is illustrated in Fig. 11. In Fig. 11(a), the RX baseband IIP3 at its minimum voltage gain is measured to be 22 dBm while in Fig. 11(b), the measured TX baseband IIP3 is 17.4 dBm at 0.6 dB voltage gain.

The measured receiver analog baseband IIP3 and noise figure with respect to its voltage gain is shown in Fig. 12. With the receiver baseband gain increasing from –11 to 49 dB, its noise figure varies within the range of 30.6–34.8 dB while its IIP3 decreases from 21 to –41 dBm accordingly.

The overall measurement results are summarized in Table 1 with comparison to the performances of recently published work[6]. Based on Table 1, it can be concluded that the proposed work consuming less power has a larger RX gain tuning range and occupies a smaller die area than the referenced work while achieving comparative performances to the latter except the relatively higher IRN. Since the IRN of the baseband path is dominated by the LPF's noise contribution, comparative noise performance can easily be obtained simply by scaling the LPF capacitance at the expense of a larger chip area. Taking the fact into account that in the referenced design, only the RX baseband is integrated on-chip in comparison to a fully integrated RX/TX baseband in the proposed work, there is still a big area budget to be allocated in order to make a fairer comparison to the proposed work.

4. Conclusion

An analog baseband circuit for an 802.11b/g/n direct con-

Table 1. Summarized experimental results.

Parameter		This work	Ref. [6]
Technology		0.13 μm CMOS	0.13 μm CMOS
Supply voltage (V)		1.2	2.5
3-dB cut-off frequency (MHz)		5/10/20	11
RX voltage gain (dB)		–11 to 49 (2dB step)	4–39 (2.5dB step)
TX voltage gain (dB)		0.6	–
Power consumption (mW)	RX bb	32.2	55
	TX bb	9.6	–
IRN @ 1 MHz	RX bb (nV/$\sqrt{\text{Hz}}$)	30.2–50	> 5
	TX bb (dB)	31.9	–
In-band IIP3 (dBm)	RX bb	21 to –41*	21 @ 4 dB gain**
(refer to 50 Ω R_S)	TX bb	17.4	–
Die area (mm^2)		1.26	1.65

* $f_{-3\text{dB}} = 10$ MHz, 2-tones @ 7, 8 MHz.
** $f_{-3\text{dB}} = 11$ MHz, 2-tones @ 3, 4 MHz.

version transceiver is implemented in a standard 0.13-μm CMOS process. By using an active-RC RX/TX filter topology and op-amp based PGA structures, both RX/TX baseband chains achieve low power, low noise, and high linearity simultaneously. A zero spreading capacitance synthesis method is adopted in building the RX elliptic LPFs, which provides a wide frequency programmable range with low power consumption when global compensation is applied by adding resistors in series with the integration capacitors. The RX/TX LPF cutoff frequency can be switched between 5 MHz, 10 MHz, and 20 MHz, and the RX baseband gain can be tuned from –11 to 49 dB with 2 dB steps to fulfill the multimode WLAN requirements.

Acknowledgments

The author would like to thank Wu Zhaosheng for his help with layout and testing.

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