A process/temperature variation tolerant RSSI*

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Abstract: A low power process/temperature variation-tolerant CMOS received signal strength indicator (RSSI) and limiter amplifier are designed using SMIC 0.13 μm CMOS technology. The limiter uses six-stage amplifier architecture for minimum power consideration. The RSSI has a dynamic range of more than 60 dB, and the RSSI linearity error is within ±0.5 dB for an input power from –65 to –8 dBm. The RSSI output voltage is from 0.15 to 1 V and the slope of the curve is 14.17 mV/dB. Furthermore, with the compensation circuit, the proposed RSSI shows good temperature independence and robustness against process variation characteristics. The RSSI with an integrated AGC loop draws 1.5 mA (I and Q paths) from a 1.2 V single supply.

Key words: limiter; RSSI; AGC; temperature compensation
DOI: 10.1088/1674-4926/33/12/125010 **EEACC:** 2220

1. Introduction

In a wireless communication system, channel factors such as multi-path fading and propagation loss cause the received signal strength in the receiver to vary over time. The magnitude variation increases the dynamic range loading in receiver circuits and complicates the synchronization mechanism. To alleviate this problem, a signal magnitude control mechanism needs to be provided at the last stage of the IF processor to keep the signal constant for further demodulation.

Generally, there are two types of circuits applied for magnitude control, namely the automatically gain-controlled amplifier (AGC) and the limiting amplifier (LA). An AGC consists of an amplifier with controllable gain and a magnitude detector for gain adjustment. Configured as a closed-loop structure, the AGC has a loop time constant[1]. On the other hand, an LA is an open-loop structure composed of a chain of gain stages, which saturate the input signal to a constant level. The limiting amplifier rather than the AGC is widely employed in wireless IF because it can handle a larger dynamic range while consuming less power with simple circuitry.

In addition, the received signal strength indicator (RSSI) is usually employed to represent the received signal strength. It can also be used to adjust the gains of the RF front end and baseband processors, and power down the receiver when there is no signal. The RSSI is generally realized in logarithmic-linear form because the wide dynamic variation of the received signal can be represented within a limited indication range[2, 3]. Successive-detection architecture is adopted for realizing the logarithmic amplifier.

2. Architecture designs

System-level considerations of the LA and RSSI will be presented in this section.

2.1. Piece-wise linear logarithmic amplifier

A logarithmic amplifier is widely used in the RSSI, since a wide dynamic variation of signal power can be represented within a limited voltage range. Successive detection architecture is used to implement a piece-wise linear logarithmic function[3, 4]. Several identical LAs are cascaded to obtain the limiter outputs. Each limiter stage output of the LAs is fed into rectifiers. The sum of the rectified outputs with a low pass filter (LPF) is the logarithmic output, which is used to measure the received signal strength.

Figure 1 shows a block diagram of the limiter and logarithmic amplifier. When input signal is small, all stages provide full gain. Therefore, the overall gain becomes A^n where A is a gain of each stage and n is number of stages. As input signal increases and reaches a certain level, the last stage begins to clip, and the overall gain becomes A^{n-1}. As input signal increases, more stages clip. As input signal increases further, finally all stages clip and the overall gain become one with the largest signal input. Therefore, the input signal strength determines overall gain piece-wisely. The input signal strength is measured when the overall gain is converted to a DC value with rectifiers and a LPF.

The RSSI information is extracted from the same chain of amplifiers. Input stage full-wave rectifiers are implemented to convert the voltage signal at each node into current, and then current from all the rectifiers are summed and converted back to voltage using an internal summing resistor. A capacitor is connected in parallel with the summing resistor to filter the AC component. The total sourcing current and the resistor R_{out} determine the output RSSI voltage.

2.2. System requirements

It is important to choose the number of stages in the limiter and RSSI design in order to achieve low power consumption, gain, bandwidth as well as allowable errors. Assuming

* Project supported by the Doctoral Scientific Starting Research from the Xi'an Polytechnic University.
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Received 3 May 2012, revised manuscript received 25 June 2012

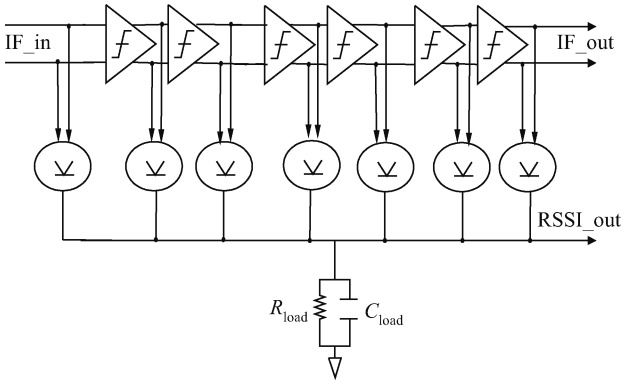

Fig. 1. Block diagram of the RSSI.

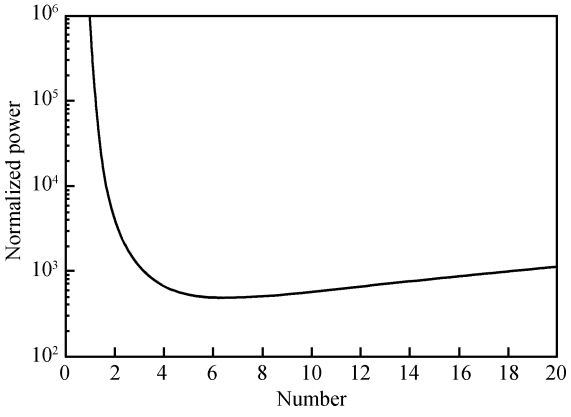

Fig. 2. Power consumption versus number of gain stages.

the limiting amplifier consists of N identical gain stages. The gain and bandwidth of the signal stage are represented as A_s and f_s, respectively. The overall limiting amplifier gain A_t and the overall bandwidth f_t are presented as follows[5]:

$$A_s = A_t^{1/N}, \tag{1}$$

$$f_s = \frac{f_t}{\sqrt{2^{1/N} - 1}}. \tag{2}$$

It can be seen that increasing the number of stages will reduce the overall bandwidth for the RSSI since more poles are introduced from each limiting amplifier. Moreover, power minimization in the IF stages of wireless applications is a more practical issue. The power P_t of the overall amplifier can be described as[1]

$$P_t = NP_s \propto N\,(\mathrm{GBW_s})^2\,, \tag{3}$$

where P_s is the power of each stage. There exists another trade-off between the stage number and GBW for power optimization. Figure 2 shows power P_t versus the number of stages when $A_t = 60$ dB and $f_t = 10$ MHz. It is found from Fig. 2 that when the number of stage is six or seven, minimum power consumption is achieved.

Besides power optimization, the number of limiting amplifier stages determines the precision of an RSSI. Since the piecewise linear logarithmic function is an approximation, the logarithmic output inherently has errors. As the number of stages

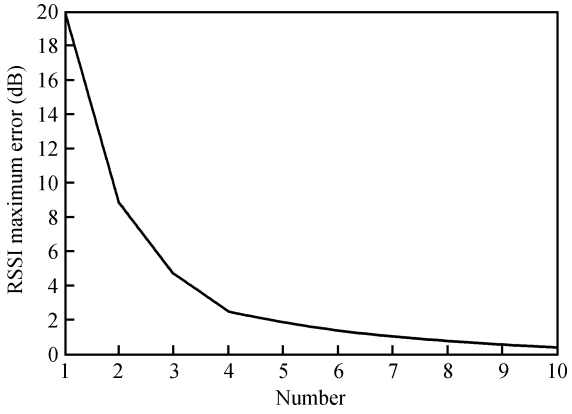

Fig. 3. Linear error versus number of gain stages.

increases, the error decreases. The maximum error compared with ideal logarithmic curve can be derived as[1]:

$$\mathrm{err_{max}(dB)} = \frac{10}{\ln 10} \times \left| 1 + \ln \left| \frac{A_s}{20} \ln 10 \right| + \ln \left| \frac{10^{A_s/20}}{10^{A_s/20} - 1} \right| - \frac{A_s}{20} \ln 10 \frac{10^{A_s/20}}{10^{A_s/20} - 1} \right|, \tag{4}$$

where A_s is the gain of each stage. The number of gain stages versus maximum error is illustrated in Fig. 3 when the total gain is 60 dB. Using six stages in the architecture, the voltage gain 10 dB of each stage can be determined. The relative error in the RSSI is smaller than ± 1 dB, which is satisfactory in our application.

3. Circuit designs

3.1. Limiting amplifier

The individual stage of the limiting amplifier circuit uses current mirrors to eliminate the load transistors body effect and is shown in Fig. 4[6]. This configuration can operate with a low power supply. As can be seen in Fig. 4, assuming transistor M3, M4, M7, and M8 are the same size, the input transistors have the same bias current as the load transistors. The voltage gain of this circuit can be shown as

$$A_V = \frac{g_{M1}}{g_{M5}} = \frac{\sqrt{(W_1/L_1)}}{\sqrt{(W_5/L_5)}}. \tag{5}$$

The voltage gain of the current mirrors is determined by the device ratios, which can be designed to be insensitive to process and thermal variations.

3.2. Full-wave current rectifier

The function of the FWCR (full-wave current rectifier) is to convert the voltage into current. The rectified currents are summed and terminated to a resistor and a capacitor loading in parallel to get the output RSSI voltage. The RSSI output slope is determined by the resistor value. The FWCR circuit

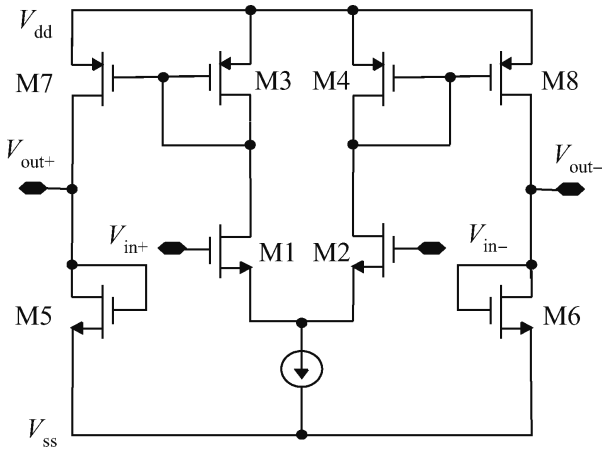

Fig. 4. Schematic of the limiting gain cell.

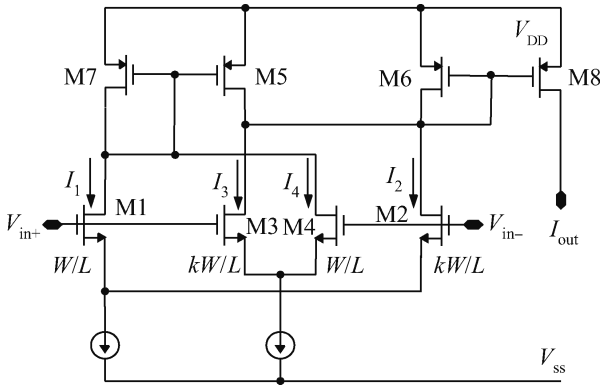

Fig. 5. Schematic of full wave current rectifier.

is shown in Fig. 5[4]. Unbalanced source coupled differential pairs generate rectified signals. One differential pair size is k times as large as the other differential pair size.

The output current I_{out} can be expressed as shown in equation below.

$$I_{out} = (I_2 + I_3) - (I_1 + I_4). \tag{6}$$

When there is no differential input voltage, the current of M2, M3 will be N-times larger than the current of M1, M4. When input voltage is small, most of current is flowing through larger size transistors (M2 and M3). Therefore, the current flow of the right-hand-side current mirror (M6 and M8) is larger than that of the left-hand-side current mirror (M5 and M7). Based on Eq. (6), I_{out} will be at its maximum value. When the differential input voltage increases, I_{out} decreases.

As input voltage increases, smaller size transistors (M1 and M4) start to contribute the current flow in the left side current mirror. Therefore, the current of the right-hand-side current mirror decreases and the current output is obtained depending on input voltage. The I_{out} will be almost zero when the differential input is large enough to make current flowing through M1, M3 or M2, M4 equal to the maximum tail currents. Since the rectifier configuration has only three stacked transistors, it can operate in low power.

The rectified current at the output of each FWR is summed and filtered to a first-order passive low-pass filter. The associate resistor and capacitor are internal, and the internal resistor

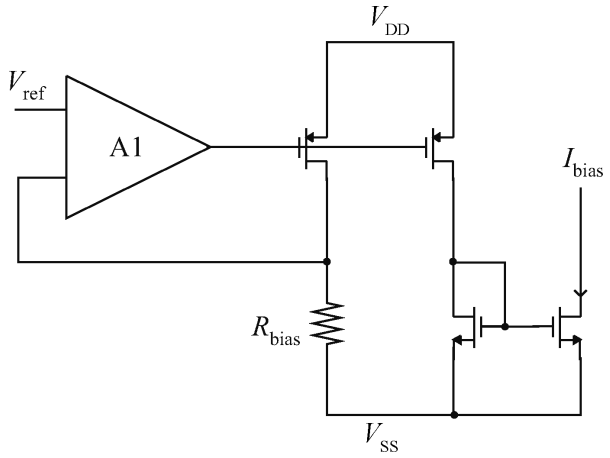

Fig. 6. Current bias generation circuit.

can regulate, thus the RSSI output slope and filter bandwidth are adjustable.

3.3. Bias generator

The output of the RSSI is a voltage obtained by applying the rectified currents of the gain stages to the on-chip resistor. To suppress the output error due to resistor process variation, the bias circuit generates bias currents that track the on-chip resistor value.

The designed bias generator in Fig. 6 bias all of the RSSI circuit blocks, including limiter amplifiers and rectifiers. As can be seen in Fig. 6, amplifier A1 forces its differential input voltage to zero using the negative feedback loop, so the voltage of the resistor R_{bias} is equal to V_{ref}. If the current mirror ratio is 1 : 1, the output current I_{bias} can be written as:

$$I_{bias} = V_{ref}/R_{bias}. \tag{7}$$

From Eq. (7), if only bandgap reference V_{ref} is fixed, the bias circuit output current I_{bias} is only concerned with the resistor R_{bias} when the temperature is changed.

The output current of the full-wave rectifier can be approximated to be positive with the bias current, then

$$I_{rssi} = \gamma I_{bias} \log V_{in}, \tag{8}$$

where γ is the coefficient, so

$$V_{rssi} = R_{rssi} I_{rssi} = \frac{R_{rssi}}{R_{bias}} \gamma V_{ref} \log V_{in}, \tag{9}$$

because R_{rssi} and R_{bias} are built with the same type of on-chip resistors and placed very close to each other, their matching is very good and nearly independent of process and temperature variation. If the coefficient γ is independent of temperature and process, then the proposed bias current used in the RSSI can extremely reduce the sensitivity of the RSSI out.

Figure 7 shows the simulated RSSI output at temperatures of –30, 30, and 90 ℃, respectively. As shown in Fig. 7(a), the proposed RSSI is strongly sensitive to temperature variation. The maximum deviation of the RSSI output from –30 to 90 ℃ is up to 100 mV. Adopting the bias current shown in Fig. 6, the

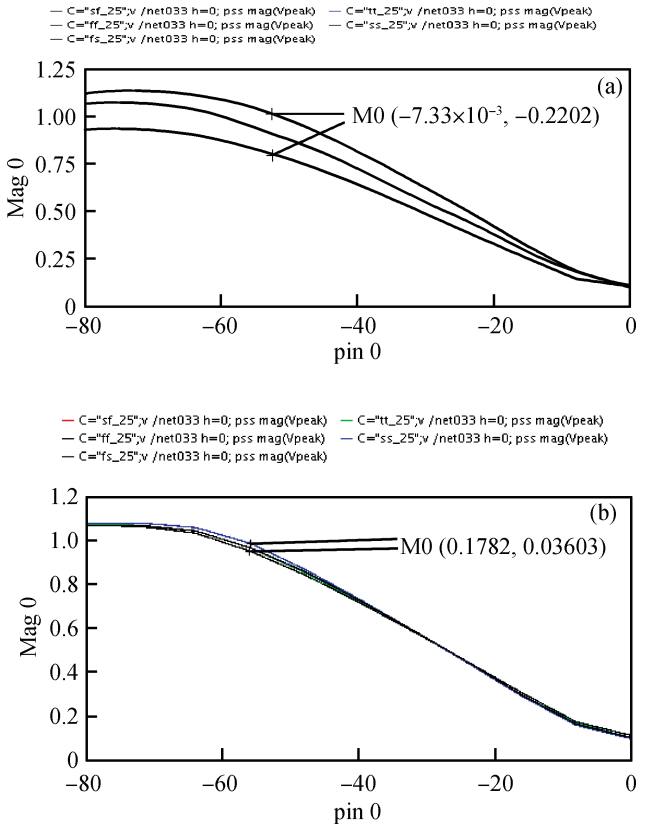

Fig. 7. The RSSI performance at different corners. (a) Without corner compensation. (b) With corner compensation.

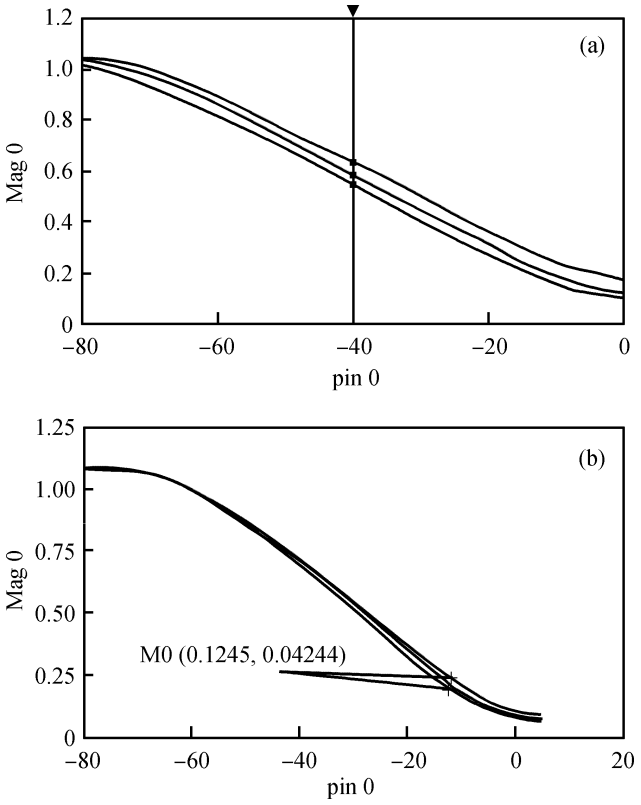

Fig. 8. The RSSI performance at different temperatures. (a) Without temperature compensation. (b) With temperature compensation.

proposed RSSI shows a good temperature-independent characteristic and is shown in Fig. 7(b). In the range of the input power from –80 to –10 dBm, the maximum output voltage deviation of the RSSI from –30 to 90 ℃ is less than 42 mV.

Figure 8 shows the RSSI performance at different corners, as can be seen in Fig. 8(a), the proposed RSSI is strongly sensitive to corner variation. The maximum deviation of the RSSI output from is up to 220 mV. From Fig. 8(b), we can see that the proposed RSSI shows good robustness against process variation.

3.4. Voltage generator

Figure 9 shows the bandgap reference circuit for generating reference voltage with low temperature dependence. To obtain low temperature dependence, we combine the negative TC voltage V_{BE} of a bipolar transistor with a weighted sum of positive TC voltage V_T to obtain the bandgap reference voltage[7]. The reference voltage is given by

$$V_{ref} = \frac{R_4}{R_2}\left(V_{BE} + \frac{R_2}{R_1} V_T \ln N\right). \tag{10}$$

A zero temperature coefficient of the reference voltage can be obtained by using an appropriate resistance ratio and transistor size ratio. Both ratios are functions of device parameters and can be optimized at the circuit level. Also, as shown in Fig. 9, transistors M1–M5 constitute a novel start-up circuit. When the bias circuit works normally ($I_D \neq 0$), the start-up circuit has no effect on the main bias circuit. When the bias circuit enters the zero-current degenerate state, the voltage at

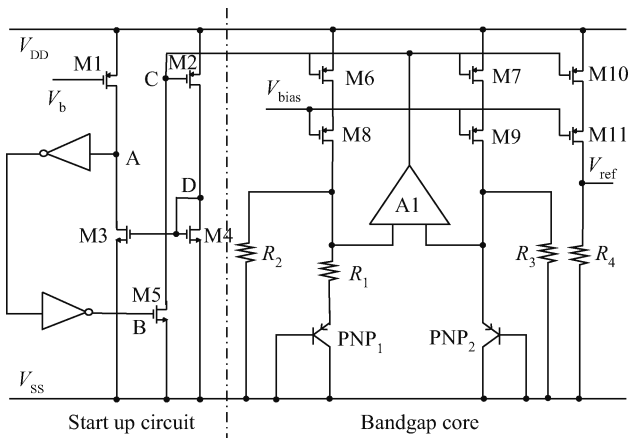

Fig. 9. Schematic of the bandgap circuit.

point C is approximately V_{DD}. Considering that transistor M1 is on due to the voltage of V_b being always zero, points A and B are almost V_{DD} to turn on the transistor M5. The start-up circuit starts to work and pull the gate voltage of transistor M2 far away from V_{DD}, ultimately pulling the bias circuit back to the normal operating state. After the bias circuit works properly, the start-up circuit must be cut off automatically to eliminate its effect on the bias circuit. The operation can be explained as follows: when transistor M2 is on, point D is high enough to turn on transistors M3 and M4, which induces point A to be nearly zero, the same as point B, transistor M5 is off, so the start-up circuit has no effect on the main bias circuit.

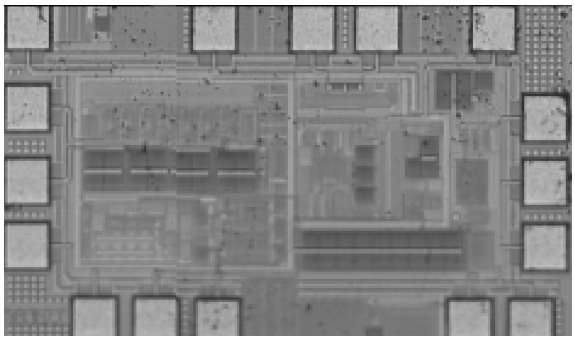

Fig. 10. Die photograph of the proposed RSSI with an AGC loop.

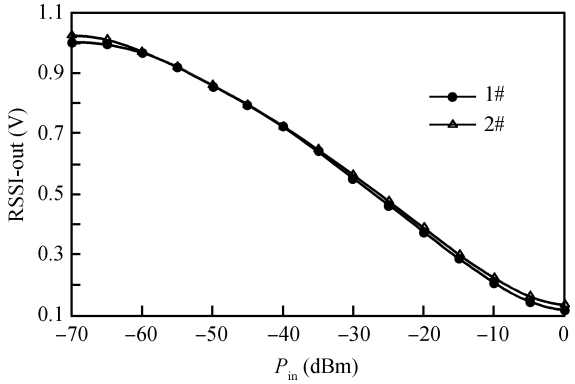

Fig. 11. RSSI output at two different chips.

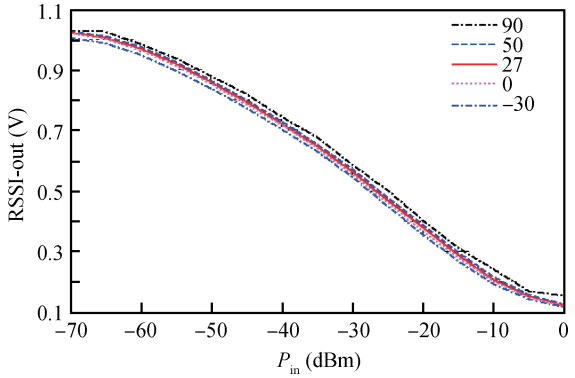

Fig. 12. RSSI output with temperature variation under a compensation circuit.

4. Measurement results

The proposed RSSI has been implemented in SMIC 0.13 μm CMOS technology with the supply voltage V_{DD} = 1.2 V, and the power consumption is 1.8 mW. Figure 10 shows the die micrograph of the proposed RSSI, which occupies an area of 0.4 mm^2 with pads.

The RSSI performance is measured with internal 10 pF capacitance and 22 kΩ resistance load. The resistive load can be varied to obtain the desired dc level. The measured transfer functions of the RSSI are shown in Figs. 11 and 12.

As can be seen in Figs. 11 and 12, the RSSI linear range is approximately 60 dB with linearity error of no more than ±0.5 dB and the RSSI output voltage is from 0.15 to 1 V. The measured RSSI sensitivity is obtained as 14.17 mV/dB in the linear range.

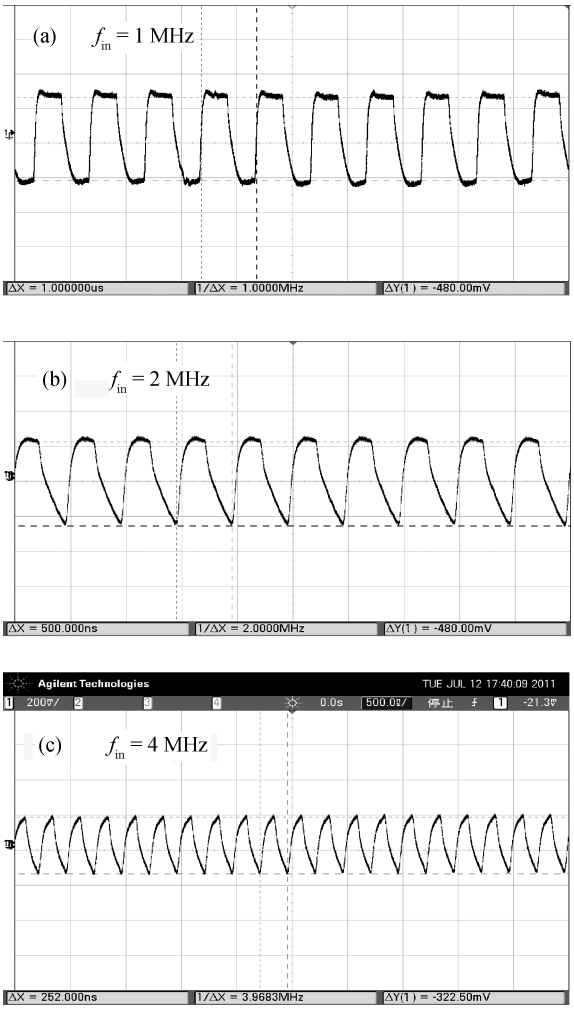

Fig. 13. Measured limiter outputs.

To evaluate the process tolerance of the RSSI, the transfer function was plotted for two randomly selected chips which can be seen in Fig. 11 and for one chip at five different temperatures, –30, 0, 27, 60 and 90 ℃ to evaluate the temperature variation, which can be seen in Fig. 12. As shown in Fig. 11, the proposed RSSI shows good robustness against process variation. And adopting the bias current shown in Fig. 6, the proposed RSSI shows a good temperature-independent characteristic in Fig. 12. In the range of input power from –80 to –10 dBm, the maximum output voltage deviation of the RSSI from –30 to 90 ℃ is less than 30–40 mV.

The measured outputs of the limiter at the frequency of 1, 2 and 4 MHz can be seen in Fig. 13. From Fig. 13, we can see that the output waves will generate serious distortion when the frequency increases. However, the simulated limiter output at 4 MHz did not have distortion. The reason is that the load capacitance is 2 pF as the real load when simulated, but when tested, the load capacitance is 10–20 pF, which distorts the output.

The measured limiter outputs with different temperatures are shown in Fig. 14. As can be seen in Fig. 14, the limiter output is 460 mVpp, which is independent of temperature variation.

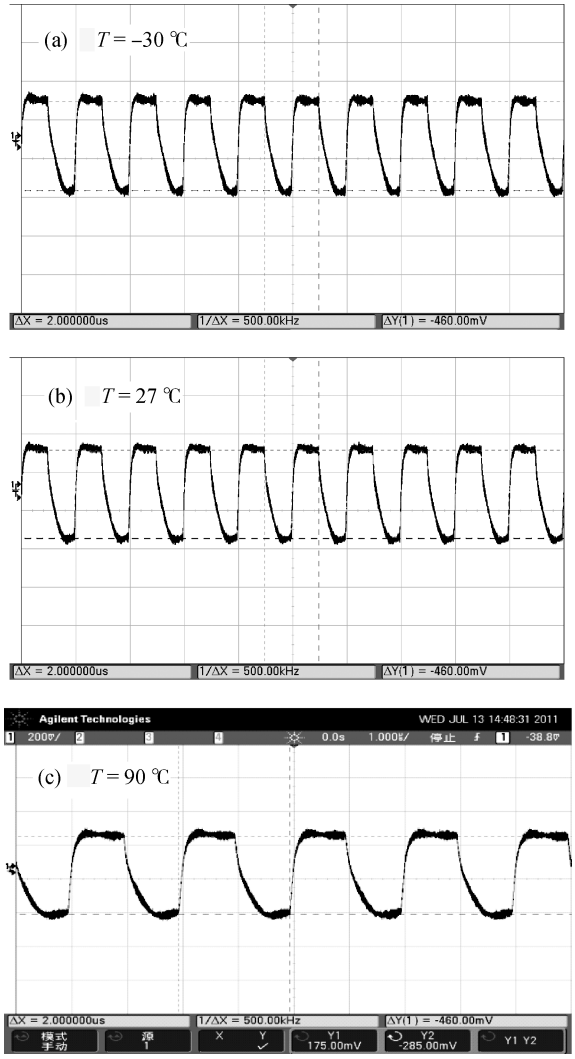

Fig. 14. Limiter outputs with different temperatures.

Table 1. Performances of the proposed limiter and RSSI.

Parameter	Value
Technology	SMIC 0.13 μm CMOS
Supply voltage	1.2 V
Chip area (with pads)	0.4 mm^2
Limiter output	480 mV
RSSI linear range	60 dB
RSSI output voltage	0.15–1 V
RSSI slop	14.17 mV/dB
RSSI error	$< \pm 0.5$ dB
RSSI variation with tem	30–40 mV
Total current (I and Q path)	1.5 mA

The measurement results of the proposed limiting amplifier and RSSI are summarized in Table 1 and a comparison with previous studies is given in Table 2. From the comparison, we can see that the proposed RSSI consumes small current to achieve 60 dB linear range, and the RSSI output voltage can be varied from 0.15 to 1 V. Furthermore, the proposed RSSI achieves less process and temperature variation.

Table 2. RSSI performances comparison.

Parameter	Ref. [8]	This work
Technology	IBM 0.18 μm	SMIC 0.13 μm
Supply voltage (V)	1.8	1.2
Chip area (mm^2)	0.2	0.4
RSSI linear range (dB)	75	60
RSSI output voltage (V)	0.02–0.27	0.15–1
RSSI slop (mV/dB)	3.33	14.17
Temperature variation error (dB)	$< \pm 2$ (0–85 ℃)	$< \pm 1.5$ (–30 to 90 ℃)
Process variation error (dB)	$< \pm 1.5$	$< \pm 0.5$
C_{load}	Off-chip/1 nF	On-chip/10 pF
Total current (mA)	2.5	1.5*

*I and Q path current

5. Conclusion

This paper presents a wide dynamic range RSSI for low voltage low power application. Measured results show that the RSSI has more than 60 dB linear range, good temperature-independence and good robustness against process variation characteristics, and the limiter output is 460 mVpp while consuming 1.5 mA from a 1.2 V supply.

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