A high linearity current mode multiplier/divider with a wide dynamic range*

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Abstract: A high linearity current mode multiplier/divider (CMM/D) with a wide dynamic range is presented. The proposed CMM/D is based on the voltage–current characteristic of the diode, thus wide dynamic range is achieved. In addition, high linearity is achieved because high accuracy current mirrors are adopted and the output current is insensitive to the temperature and device parameters of the fabrication process. Furthermore, no extra bias current for all input signals is required and thus power saving is realized. With proper selection of establishing the input terminal, the proposed circuit can perform as a multifunction circuit to be operated as a multiplier/divider, without changing its topology. The proposed circuit is implemented in a 0.25 μm BCD process and the chip area is 0.26×0.24 mm^2. The simulation and measurement results show that the maximum static linearity error is $\pm 1.8\%$ and the total harmonic distortion is 0.4% while the input current ranges from 0 to 200 μA.

Key words: high linearity; current mode; multiplier/divider; static linearity; THD

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1. Introduction

The evolution of integrated circuit technology and future scenarios of ubiquitous and pervasive computing have stressed the need for analog circuits with high linearity and wide dynamic range. The multiplier/divider, as a basic analog block, is widely used in controls, signal processing, instrumentations, and telecommunication systems such as modulators/demodulators, frequency doublers, and rectifiers[1]. The methods of achieving a multiplier/divider can be classified into voltage mode and current mode. Generally, compared with the voltage mode multiplier/divider, the current mode multiplier/divider (CMM/D) has received much more attention due to the advantages such as higher frequency, inherent overcurrent protection capability, and high efficiency[2]. A CMM/D based on a pure bipolar has the advantage of a wide dynamic range and high speed; however, more than ten bipolars are needed and therefore a larger die area is consumed[2−4]. Recently, CMM/D based on pure CMOS technique has become more popular due to its small area and integration capacity. However, pure CMOS CMM/D with the transistors operating in either the weak or strong inversion region suffers from a small dynamic range, large power consumption, and complexity[5−10].

In this paper, the proposed CMM/D is based on the voltage–current characteristic of the diode, therefore, wider dynamic range is achieved. High accuracy mirrors are adopted to improve the linearity in a wide dynamic range. In addition, the proposed CMM/D is insensitive to the process, voltage, temperature (PVT) various. The circuit behavior and design consideration are analyzed in detail. The circuit is implemented in a 0.25 μm BCD process and measurement results including a typical application are used to prove the validity and versatility of the proposed CMM/D.

2. Proposed architecture

The structure of the proposed CMM/D is shown in Fig. 1. The core CMM/D, enclosed by solid line, only consists of an operational transconductance amplifier (OTA) and four diodes. It is worth noting that no extra bias current is needed for the input and output signals. Hence power efficiency is improved.

The transistors M1–M6 operate as a cascade current mirror which samples the input current $I_{\rm in1}$ to the D1 with high accuracy, while the current mirror formed by M22–M23 forces the current of M23 to be a copy of $I_{\rm in1}$. Diode D5 is utilized to balance the drain voltage of M4 and M6, moreover, good symmetry can be achieved simultaneously. The current of diode D2 is just the input current $I_{\rm in2}$. Consequently, the voltage at node C is obtained as follows,

$$V_{\rm C} = V_{\rm D1} + V_{\rm D2} = \frac{kT}{q}\ln\frac{I_{\rm in1}}{I_{\rm so}} + \frac{kT}{q}\ln\frac{I_{\rm in2}}{I_{\rm so}} = \frac{kT}{q}\ln\frac{I_{\rm in1}I_{\rm in2}}{I_{\rm so}^2}, \quad (1)$$

where $I_{\rm so}$ is the saturation current, k is the Boltzmann constant, T and q are the absolute temperature and basic charge, respectively.

To achieve high linearity, a high accuracy current mirror[11−13] is needed. In this paper, the transistors enclosed by the dotted line also form a high accuracy current mirror without extra bias circuits. Transistors M17–M20 are used to improve the matching accuracy. Concrete causes are presented below: the drain source voltage of M16 is $V_{\rm gs17}$ while M15 is $V_{\rm gs20}$. As the current mirror consisted of M18 and M19, the current and gate source voltage of M17 should be approximately equal to that of M20. Hence the current of M15 should be a highly ac-

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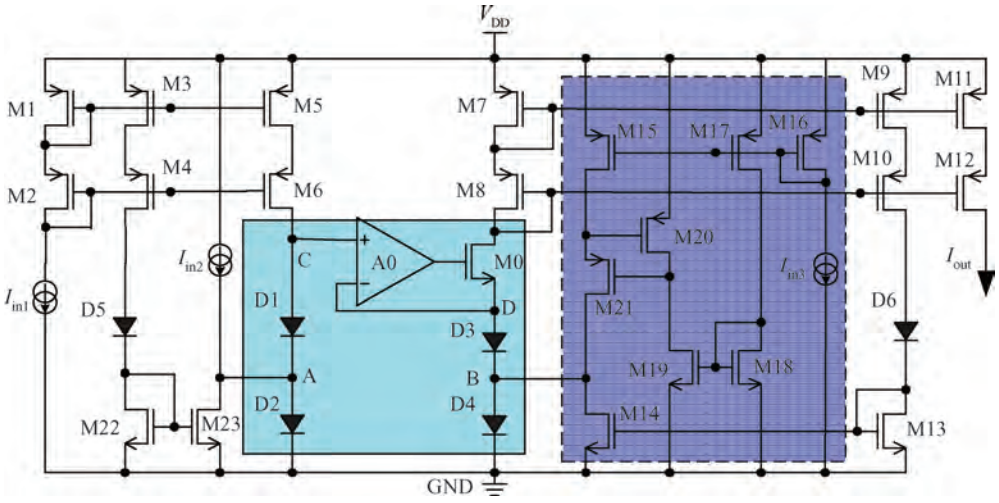

Fig. 1. Proposed CMM/D.

curate copy of M16, despite the "channel-length modulation". Just as analyzed before, D4's current is just the input current I_{in3}. Consequently, the voltage at node B is given as follows,

$$V_B = \frac{kT}{q} \ln \frac{I_{in3}}{I_{so}}. \tag{2}$$

The negative loop composed by M0 and OTA can stabilize the loop, while the OTA adjusts the gate voltage of transistor M0 so as to equalize the voltage of nodes C and D. Thus

$$\begin{aligned} V_{D3} = V_C - V_B &= \frac{kT}{q} \ln \frac{I_{in1} I_{in2}}{I_{so}^2} - \frac{kT}{q} \ln \frac{I_{in3}}{I_{so}} \\ &= \frac{kT}{q} \ln \frac{I_{in1} I_{in2}}{I_{in3}} \frac{1}{I_{so}}. \end{aligned} \tag{3}$$

And the output current I_{out} is obtained as follows:

$$I_{out} = I_{so} e^{\frac{V_{D3}}{kT/q}} = \frac{I_{in1} I_{in2}}{I_{in3}}. \tag{4}$$

It is clearly seen that the output current given in Eq. (4) yields the multiplication and the division based on logarithmic-antilogarithmic characteristics of the diode. In other words, the proposed circuit in Fig. 1 can be manipulated to function as multiplication or division by setting the proper selection of applied input currents to the circuit without changing its basic topology. It is worth noting that Equation (4) is independent of I_{so}, k, T and q, therefore, high linearity can be achieved because the output current of all types of the proposed functions are theoretically insensitive to temperature and device parameters in the fabrication process. More importantly, the dynamic range is only limited by the maximum allowable terminal currents of the core devices and the restricted DC power supply voltage of the circuits. Compared to other CMM/Ds, with the transistors operating in either the weak or strong inversion region, a wider dynamic range is achieved in the proposed CMM/D. The high linearity and wide dynamic range properties make the proposed CMM/D suitable for high accuracy control systems.

3. Design consideration

While exhibiting the ability of reducing nonlinearity, the circuit still has a linearity error due to the matching accuracy of the current mirrors and diodes, the offset of the OTA, and process errors. In order to attain the highest possible linearity, a cascade current mirror and a highly accurate current mirror, as mentioned before, are adopted. In addition, each current mirror should employ the same length for all of the transistors so as to minimize error due to the side-diffusion of the source and drain area. The length of the transistor is set much larger than the minimum required size to avoid the effect of "channel-length modulation"[14].

The rate of reverse saturation current I_s/I_{so} depends on the matching accuracy of the diode. Assuming the mismatching error is δ_i for D_i, Equation (3) can be rewritten as:

$$\begin{aligned} V_{D3} &= V_C - V_B \\ &= \frac{kT}{q} \ln \frac{I_{in1} I_{in2}}{(1+\delta_1)(1+\delta_2) I_{so}^2} - \frac{kT}{q} \ln \frac{I_{in3}}{(1+\delta_4) I_{so}} \\ &= \frac{kT}{q} \ln \frac{I_{in1} I_{in2}}{I_{in3}} \frac{(1+\delta_4) I_{so}}{(1+\delta_1)(1+\delta_2)}. \end{aligned} \tag{5}$$

And the output current I_{out} is obtained as follows:

$$\begin{aligned} I_{out} = (I_{so} + \delta_3) e^{\frac{V_{D3}}{kT/q}} &= \frac{I_{in1} I_{in2}}{I_{in3}} \frac{(1+\delta_3)(1+\delta_4)}{(1+\delta_1)(1+\delta_2)} \\ &\approx \frac{I_{in1} I_{in2}}{I_{in3}} [1 - (\delta_1 + \delta_2 - \delta_3 - \delta_4)]. \end{aligned} \tag{6}$$

In a 0.25 μm BCD process, the mismatching error is very small, typically $\pm 0.5\%$, and then the maximum output current error is $\pm 2\%$ which can be tolerated in most systems.

The OTA experiences no resistive loading, but owing to asymmetries, the OTA suffers from input "offset", and the OTA offset voltage introduces error in the output current. Several methods are employed to reduce the effect of offset voltage; a two-stage Miller amplifier[13] incorporates carefully chosen large input differential pair devices to minimize the offset.

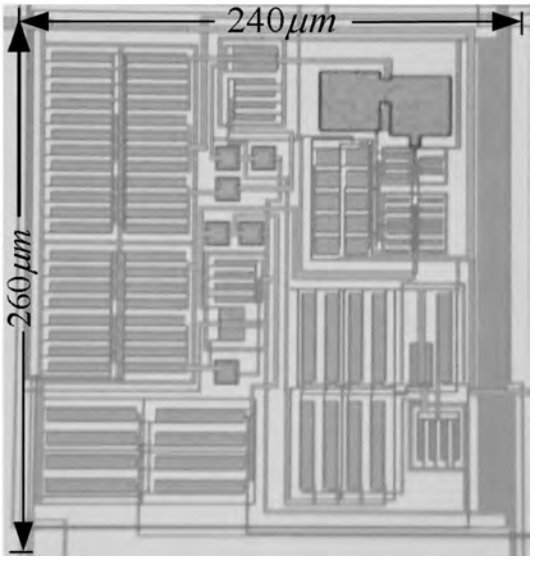

Fig. 2. Microphotograph of the proposed CCM/D.

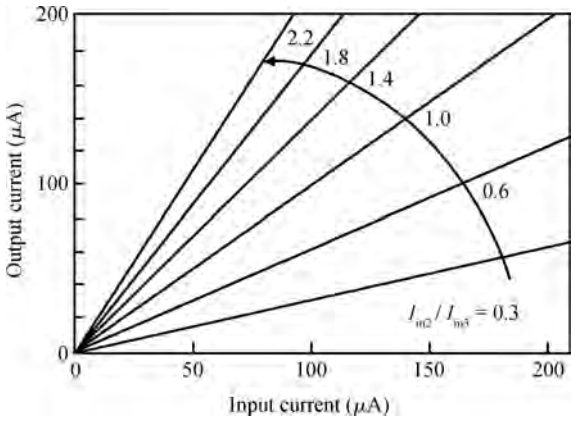

Fig. 3. Simulated DC transfer characteristics for $I_{in2}/I_{in3} = 0.3$, 0.6, 1.0, 1.4, 1.8, 2.2.

4. Implementation and measurement results

To verify the validity of the proposed CMM/D, the circuit in Fig. 1 is implemented in a 0.25 μm BCD process. The die photograph is shown in Fig. 2 and the area is about 0.26 × 0.24 mm^2.

To test the operation of proposed CMM/D, the DC transfer characteristics are simulated under the conditions of $I_{in2}/I_{in3} = 0.3$, 0.6, 1.0, 1.4, 1.8, 2.2 with the input current I_{in1} ranging from 0 to 200 μA. The simulated resultant relation between input and output currents is illustrated in Fig. 3. It shows that the proposed CMM/D exhibits behavior as expected according to the stated theory with respect to inputs when the input current ranges from 0 to 200 μA.

The corresponding static linearity errors are shown in Fig. 4. As can be seen, the linearity errors increase as the input current increases. The maximum linearity error is ±1.8% while the input current ranges from 0 to 200 μA. In particular, when the current gain is unity, the maximum linearity error is simulated to be –0.4%, in other words, high linearity is obtained.

To prove the simulation results of the proposed CMM/D,

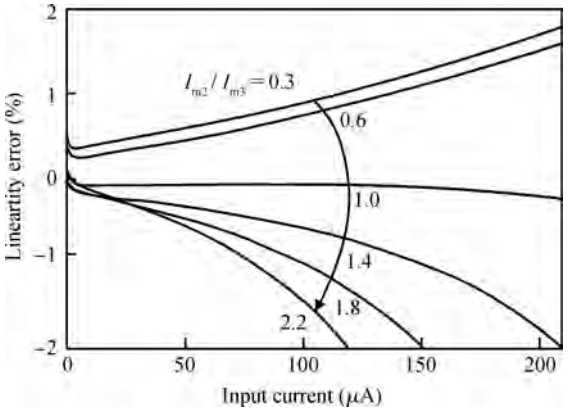

Fig. 4. Linearity error for $I_{in2}/I_{in3} = 0.3$, 0.6, 1.0, 1.4, 1.8, 2.2.

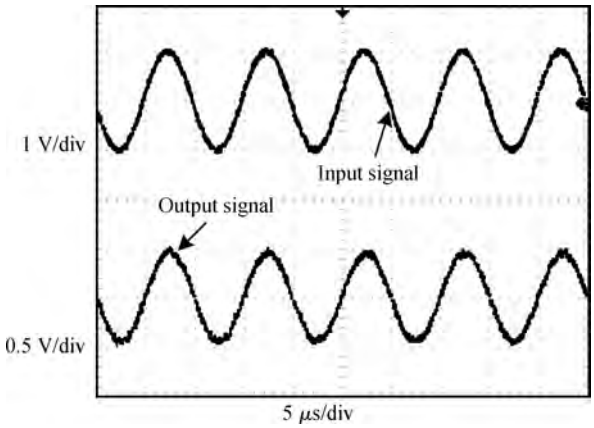

Fig. 5. Transient response of the multiplier.

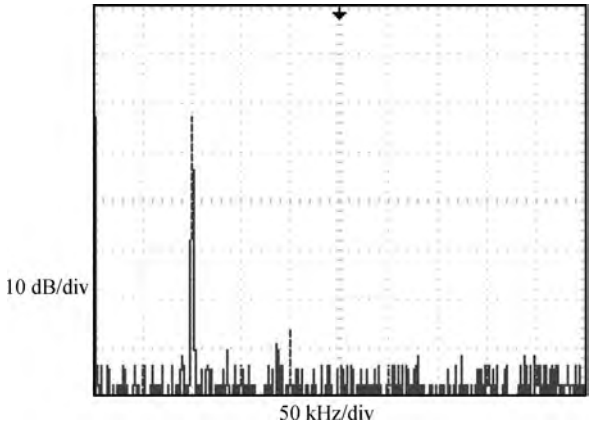

Fig. 6. Magnitude spectrum of the output current.

the transient response measurement results are given as follows:

(1) Working as a multiplier. The input current I_{in1} is set to be a sinusoidal signal at 200 μA_{p-p} with 100 kHz frequency while the current gain is $I_{in2}/I_{in3} = 0.45$. The output current is converted to voltage, which is shown in Fig. 5. Doing the FFT (fast Fourier transform algorithm) to the output waveform, the measurement result of the magnitude spectrum is shown in Fig. 6. It shows that the spurious free dynamic range (SFDR) is over 44 dB and the total harmonic distortion (THD) is 0.4%.

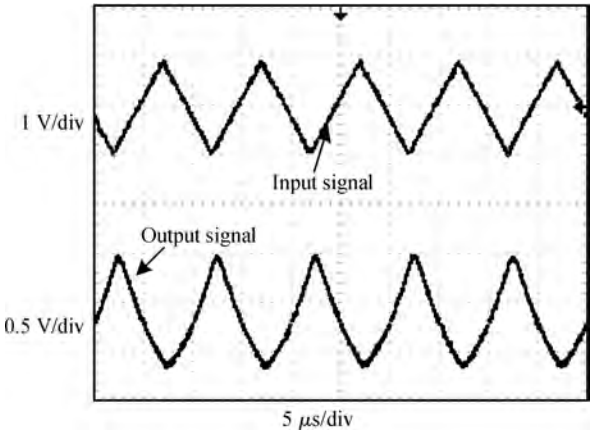

Fig. 7. Transient response of the divider.

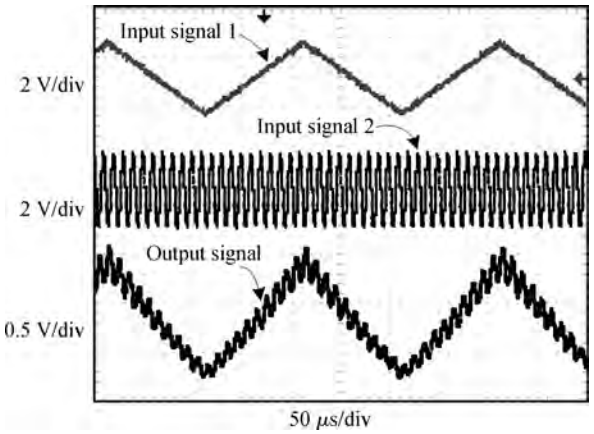

Fig. 8. Output of the CMMD as a modulator.

(2) Working as a divider. The input current I_{in3} is set to be a triangular signal at 200 μA_{p-p} with 100 kHz frequency, while the other bias currents are $I_{in1} = 50\ \mu A$ and $I_{in2} = 150\ \mu A$. The output waveform is shown in Fig. 7. The measurement results show that the proposed CMM/D performs a division function as predicted.

To underline its versatility, a typical application as a modulator is implemented. Figure 8 shows the experimental results obtained by modulating a 100 kHz high frequency sinusoidal signal with a 5 kHz low frequency triangular signal.

Consequently, all of the obtained simulation and measurement results demonstrate that the proposed circuit can operate well as multiplier or divider with high linearity in a wide range, as expected in the design idea. All of the key parameters and a performance comparison are given in Table 1.

5. Conclusion

Based on the voltage–current characteristic of the diode, a high linearity CMM/D with a wide dynamic range is presented in this paper. A wider dynamic range is achieved because of the adoption of the diodes. The output current is independent of the temperature and device parameters of the fabrication process, and highly accurate current mirrors are used to improve the linearity over a wide dynamic range. The circuit behavior and design consideration are analyzed in detail. The simulation and measurements, including a typical application, display that the maximum static linearity error is $\pm 1.8\%$ and the THD is 0.4% while the input current ranges from 0 to 200 μA.

Table 1. Performance comparison.

Parameter	Ref. [7]	Ref. [8]	This work
Technology	–	0.5 μm CMOS	0.25 μm BCD
Area (mm^2)	–	0.083	0.062
Bias for input signal	No	Yes	No
Output range (μA)	± 20	± 25	0–200
Maximum linearity error (%)	1.22	5	1.8
THD (%)	1.54	0.2	0.4
N of quadrants	4	2	1

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