A 72-dB-SNDR rail-to-rail successive approximation ADC using mismatch calibration techniques

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Abstract: When the voltage of an analog input signal is equal to the supply voltage, it is difficult for a conventional successive approximation ADC to correctly convert the analog signal into digital signal. This paper introduces an improved successive approximation ADC, which can convert the rail-to-rail input range and reduce sampling time through a track-and-hold circuit. Comparator offset cancellation and capacitor self-calibration techniques are used in this ADC. Measurement results show that the peak SNDR of this ADC reaches 72 dB and the signal effective bandwidth is up to 1.25 MHz. It consumes 1 mW in the test, and the figure of merit is 123 fJ/conversion-step.

Key words: rail-to-rail; mismatch calibration; THA; successive approximation ADC

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1. Introduction

The current successive approximation register (SAR) ADC is highlighted in a region having a resolution of 8 to 16 bits and a conversion rate of 1 to 100 MS/s. The SAR ADC is on the rise as a next-generation data converter with high efficiency due to its low electric power consumption. For the conventional SAR ADC, an external analog input signal charges the sample capacitor, and the sampling time is limited by the sampling capacitor value. By adding a sample and hold amplifier (SHA) at the front end of the SAR ADC to charge the capacitor, the input signal outside the scope of the SHA is not sampled correctly, especially when the input signal voltage is equal to the supply voltage, and the SHA output signal will become slightly smaller than the supply voltage due to this reason[1]. Therefore, this paper proposes an improved rail-to-rail successive approximation analog-to-digital converter for many portable applications, such as medical instruments and digital microphones. The SAR ADC can convert the input signal where amplitude is equal to the supply voltage, and shorten the sampling time through a track-and-hold amplifier (THA). Comparator offset cancellation and capacitor self-calibration techniques are used in this SAR ADC to further improve the conversion accuracy.

2. Rail-to-rail SAR ADC

The structure of the rail-to-rail SAR ADC outlined in this paper includes a THA with a voltage gain of less than one, a charge redistribution DAC array which can compensate THA output gain, a multi-level high-speed comparator with offset cancellation, a capacitor array mismatch calibration circuit, and a SAR register, as shown in Fig. 1.

When the analog input voltage is equal to the supply voltage, the THA with voltage gain less than one can track and hold input signal correctly in the rail-to-rail range. The charge redistribution DAC array with gain compensation can adjust the digital outputs of the converter, which are equal to the value directly sampled by DAC without gain compensation. The THA input capacitance can be independent of the DAC and the decreases of the input capacitance can increase the speed of the successive approximation ADC. The successive approximation ADC requires high speed and a precise comparator to distinguish the smaller voltage. In this paper a multi-level structure and offset cancellation are used in the comparator.

The accuracy of an SAR ADC is often limited by the mismatch of both the passive components and the ideally identical circuit transistors. Comparator offset voltage and capacitor mismatch can cause harmonic distortion and thus greatly influence the accuracy of an ADC. The SAR ADC uses a self-calibration technique to eliminate both comparator offset voltage and capacitor mismatches. The SAR ADC fixes an input, and searches for a digital output that is the closest to the input by successively changing a reference voltage. When an error occurs in the SAR ADC, it cannot be corrected. That is, although a desired digital code is 100100, when the D2 code outputs a value of 0 for capacitor mismatch, a general SAR ADC outputs a digital code of 100011. This paper focuses on an SAR ADC capable of correcting an error of a finally output digital code, so that the error generated during operation is corrected. The correction circuit includes a capacitor array and a capacitor self-calibration unit which corrects the digital signal of the capacitor array.

3. Circuit design

3.1. Track-and-hold amplifier with a voltage gain of less than one

A traditional SAR ADC uses an external analog input signal to charge the sample capacitor. Thus it is difficult to fully shorten the sampling time. In this paper, a THA is added to charge the capacitor to increase the sampling rate. The circuit of a THA with a voltage gain of less than one is shown in Fig. 2.

A differential structure is applied in the THA and it stays at

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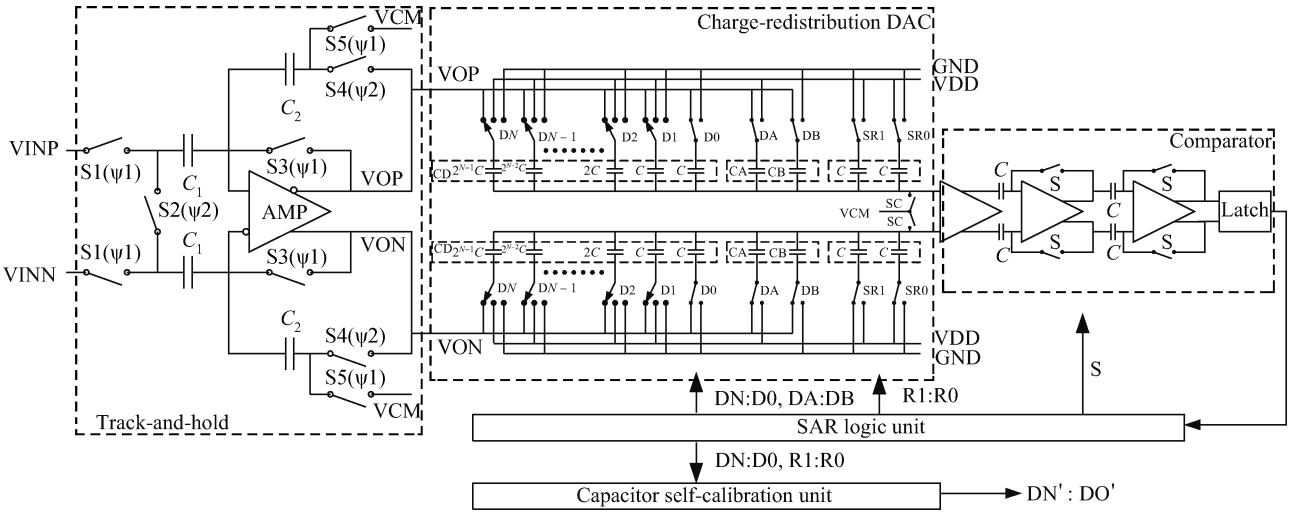

Fig. 1. Rail-to-rail SAR ADC structure.

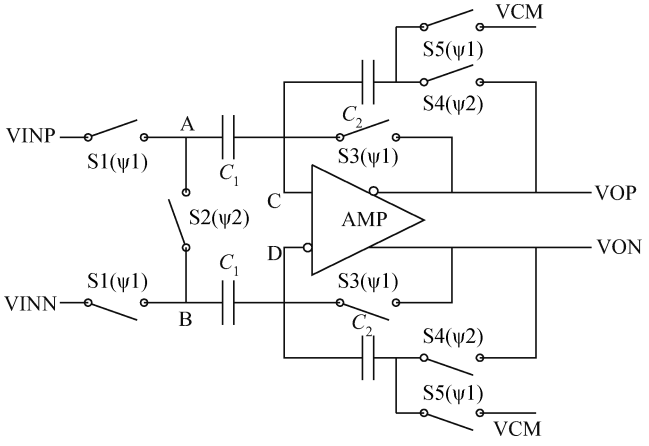

Fig. 2. Track-and-hold amplifier with a voltage gain of less than one.

the sample state or hold stage[2]. At the sample stage, switch S3 is closed. The voltage at node C and node D (VCM) is set at approximately half the supply voltage. Switch S5 is also closed, providing VCM to the bottom plate of capacitor C_2. Because the amplifier is not ideal, the voltage gap between node C and D is approximately equal to the amplifier AMP offset voltage. The signal of VCM is implemented by using a bandgap and low dropout linear regulator (LDO). The purpose of providing VCM to C_2 is to store the amplifier offset voltage so as to remove the offset voltage. Later on, switch S1 is closed, the input voltage VINP and VINN are provided to the bottom plate of the capacitor C_1, charge Q_{1P} and Q_{1N} stored in capacitor C_1 are, respectively:

$$Q_{1P} = C_1 (\mathrm{VINP} - \mathrm{VCM_{nodeC}}), \tag{1}$$

$$Q_{1N} = C_1 (\mathrm{VINN} - \mathrm{VCM_{nodeD}}). \tag{2}$$

In the meantime, charge Q_{2C} and Q_{2D} stored in capacitor C_2 are, respectively:

$$Q_{2C} = C_2 (\mathrm{VCM} - \mathrm{VCM_{nodeC}}), \tag{3}$$

$$Q_{2D} = C_2 (\mathrm{VCM} - \mathrm{VCM_{nodeD}}). \tag{4}$$

At the hold stage, switch S3 is switched off, leaving node C and node D floating. Switch S5 is also switched off and VCM is disconnected to the bottom plate of capacitor C_2. Switches S2 and S4 are closed and the voltage at node A and node B is equal to VCMB. If the voltage gain of amplifier is big enough, the equation of node C is:

$$\begin{aligned} &C_1 (\mathrm{VINP} - \mathrm{VCM_{nodeC}}) + C_2 (\mathrm{VCM} - \mathrm{VCM_{nodeC}}) \\ &= C_1 (\mathrm{VCMB} - \mathrm{VCM_{nodeC}}) + C_2 (\mathrm{VOP} - \mathrm{VCM_{nodeC}}). \end{aligned} \tag{5}$$

The equation of node D is:

$$\begin{aligned} &C_1 (\mathrm{VINN} - \mathrm{VCM_{nodeD}}) + C_2 (\mathrm{VCM} - \mathrm{VCM_{nodeD}}) \\ &= C_1 (\mathrm{VCMB} - \mathrm{VCM_{nodeD}}) + C_2 (\mathrm{VOP} - \mathrm{VCM_{nodeD}}), \end{aligned} \tag{6}$$

where VOP and VON represent the voltage node VOP and node VON respectively, Equation (5) subtracts Eq. (6),

$$(\mathrm{VOP} - \mathrm{VON}) = \frac{C_1}{C_2} (\mathrm{VINP} - \mathrm{VINN}). \tag{7}$$

By transferring the charge, even if the amplifier is not ideal, the output voltage can also be proportional to analog input voltage. By adjusting capacitors C_1 and C_2, the voltage gain can be set at less than one. When the analog input signal voltage is equal to the supply voltage, the THA can avoid amplifier saturation. The common voltage of output signals is equal to VCM. Therefore the THA can handle the input analog signal whose voltage range is rail-to-rail.

3.2. Charge redistribution DAC array with gain compensation

Because the voltage gain of the THA is set at less than one, the charge redistribution DAC array in the rail-to-rail SAR ADC needs to compensate the voltage decrease caused by the THA gain. The charge redistribution DAC array with gain compensation is shown in Fig. 3(a).

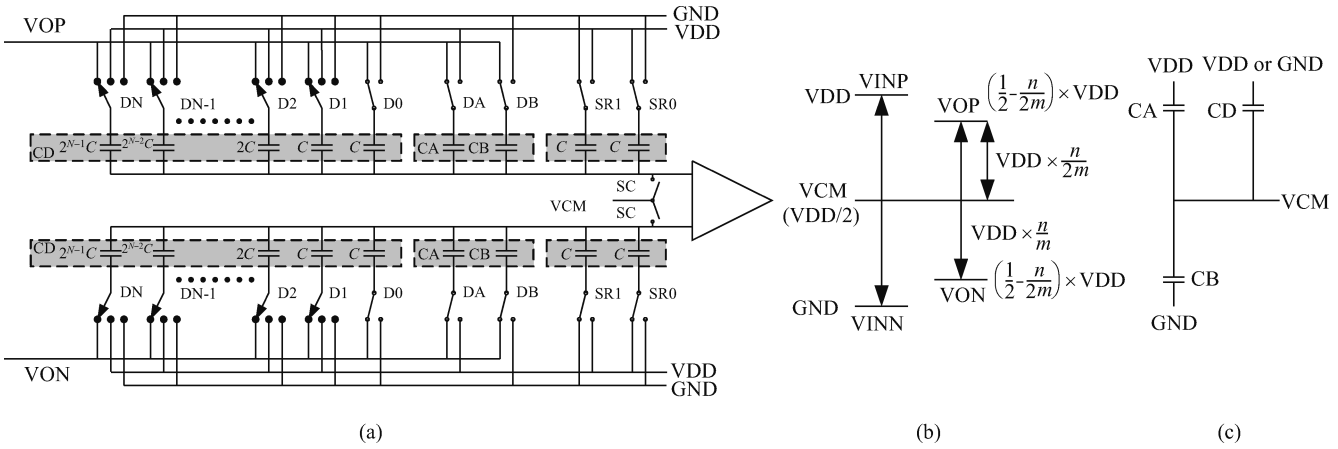

Fig. 3. Charge redistribution DAC array with gain compensation.

When the analog input voltage is equal to the supply voltage, sampled by the THA whose magnification is n/m, the output voltage of node VOP becomes equal to $(1/2 + n/2m)$ VDD, and the output voltage of node VON becomes equal to $(1/2 - n/2m)$VDD. As shown in Fig. 3(b), the voltage gap between output nodes is equal to (n/m)VDD. Figure 3(c) shows the equivalent structure of the charge redistribution DAC array with gain compensation capacitors at the conversion stage. Capacitor "CA" and capacitor "CB" represent respectively the total capacitors coupled to the VDD in the DAC capacitor array and the total capacitors coupled to the GND in the DAC capacitor array, whatever the output data of the comparator is and the capacitor "CD" represents the total capacitors coupled to the VDD or GND, which responds to the comparator outputs. According to the charge conservation law, when the comparator outputs are all "1",

$$\left(\frac{m+n}{2m}\mathrm{VDD}-\mathrm{VCM}\right)(\mathrm{CA}+\mathrm{CB}+\mathrm{CD})$$
$$=(\mathrm{VDD}-\mathrm{VCM})(\mathrm{CA}+\mathrm{CD})+(\mathrm{GND}-\mathrm{VCM})\,\mathrm{CB}. \quad (8)$$

When the comparator outputs are all "0",

$$(\mathrm{VDD}-\mathrm{VCM})\,\mathrm{CA}=(\mathrm{VCM}-\mathrm{GND})(\mathrm{CB}+\mathrm{CD}). \quad (9)$$

When VCM is equal to VDD/2, according to Eqs. (8) and (9), the gain compensation capacitors CA and CB are respectively described as

$$\mathrm{CA}=\frac{m}{n}\mathrm{CD}, \quad (10)$$

$$\mathrm{CB}=\frac{m-n}{n}\mathrm{CD}. \quad (11)$$

CD is the total capacitance value when there is no gain compensation for the charge redistribution DAC array. By increasing the gain compensation of capacitor CA and CB, the DAC array can adjust the comparator's input voltage, so as to obtain the same digital output values as that directly sampled by a conventional DAC without gain compensation.

3.3. Improved bootstrap switch

The improved bootstrap switch circuit in THA application is shown in Fig. 4. The circuit includes transistors

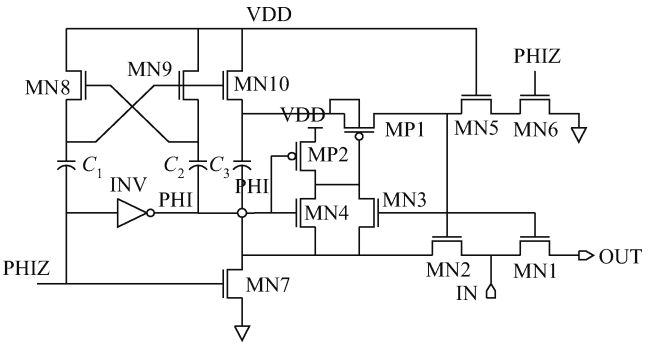

Fig. 4. Improved bootstrap switch.

MN1–MN10, MP1, MP2, inverter INV, capacitors C1, C2, C3, input node IN, output node OUT, and clock signal nodes PHI and PHIZ. NMOS transistor MN1 connected to terminal OUT is the bootstrapped switch. The circuit is used to increase the bandwidth of the THA at the front end of the SAR ADC.

The circuit of Fig. 4 operates as follows. First we focus on the charge pump formed by transistors MN8, MN9, capacitors C_1, C_2 and C_3, and the inverter INV. When PHIZ goes high, the bottom plate of C_1 will reach VDD. Since the bottom plates of C_2 and C_3 are grounded for this state, those capacitors are charged till their top plates reach voltage VDD − VTHN (where VTHN is the threshold voltage for NMOS transistors MN9 and MN10). When PHIZ goes low, the top plate of C_2 is pushed well above VDD, yielding complete charging of C_1 to VDD through the switch MN8. In the next phase, when PHIZ goes high again, since C_1 is charged to VDD, the top plate of C_1 will be pushed to 2VDD and C_2 and C_3 will be completely charged to VDD. In steady state, C_1, C_2 and C_3 will be charged to VDD and the voltage on the top plate of C_1 and C_2 will change between VDD and 2VDD.

When all the capacitors are charged to VDD, the bootstrapped switch operates as follows: when PHIZ goes high, the bottom plate of C_1 is grounded and switch MN10 is turned on, hence C_3 is charged to VDD; switch MP2 is also on, driving the gate of MP1 to VDD, hence MP1 is off and finally MN6 is on and grounds the gate terminal of the main switch MN1. Since their gate terminal is grounded, MN3, MN2 and MN1 are off. During this phase, the MN1 disconnects the input node

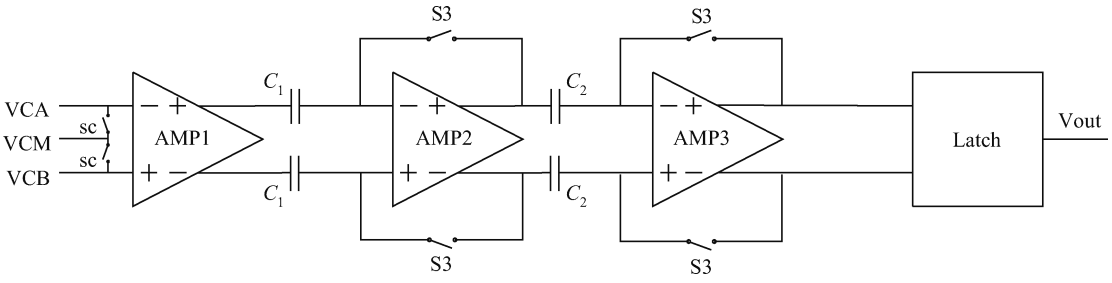

Fig. 5. Multi-level high-speed comparator with offset cancellation.

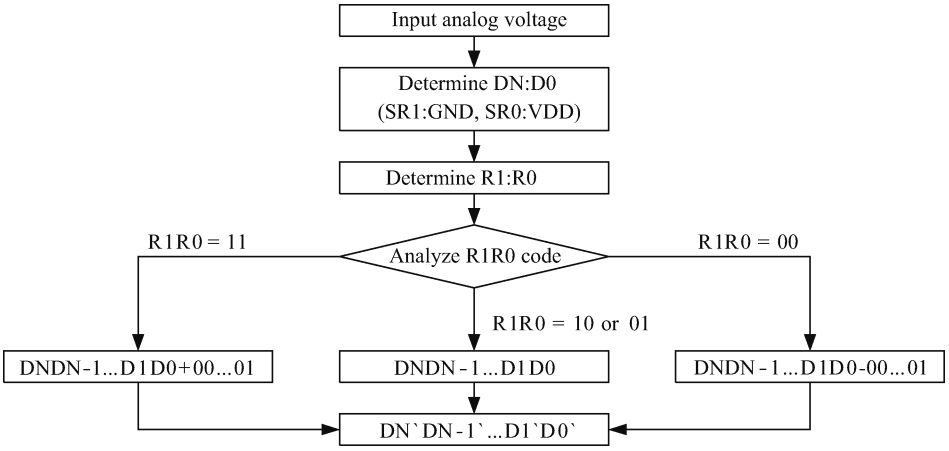

Fig. 6. Capacitor array mismatch calibration arithmetic.

IN from the output node OUT and charges C_3 to VDD. When PHIZ goes low, the gate terminal of MN1 has high impedance, since MN6 is off. Initially, the bottom plate of C_3 is floating, but because switch MN4 connects C_3 between the gate and source terminal of MP1, this transistor turns on immediately and the charge stored on C_3 starts flowing to the gate terminal of main switch MN1. While the gate voltage of switch MN1 rises, MN2 turns on and forces the bottom plate of C_3 towards the input voltage VIN, which pushes the top plate of C_3 to voltage VDD+VIN. Eventually this voltage appears at the gate of MN1 and as a result MN1 turns on completely to connect the input terminal IN to the output terminal OUT. MN2 turns on completely to connect input terminal IN to the bottom terminal C_3 and MN3 turns on completely to drive the gate of MP1 to the input voltage level. The gate-to-source voltages of all these four switches, namely MN1, MN2, MN3 and MP1, are all equal to VDD. In the traditional circuit, bootstrapped switch MN1 can be turned on by pulling the gate terminal of MP1 to ground, if the input signal is equal to VDD then the voltage difference between the gate and source of MP1 would be 2VDD. For the improved bootstrap switch, when the bootstrapped switch MN1 is turned on, the gate voltage on MP1 is forced to the input signal through MN3 so that the gate-to-source voltage of MP1 is bound within VDD, and hence reliability is enhanced.

3.4. Multi-level high-speed comparator with offset cancellation

We design a three preamp latched comparator, as shown in Fig. 5. The comparator includes three pre-amplifiers and a latch, the first of the three pre-amplifier should have low gain, high bandwidth, and the second and third amplifiers should have a high slew rate.

The comparator has two stages, the offset cancellation phase and comparison phase. The offset cancellation phase corresponds to the DAC sampling stage, where switches SC and S3 are closed, the first and second amplifier's offset voltage is stored in C_1, and the third amplifier's offset voltage is stored in C_2. The comparison phase corresponds to the DAC holding and converting stage, where switches SC and S3 are turned off.

In this paper, the supply voltage is 3.3 V, the conversion speed is 2.5 MSPS, and the precision is 14 bit, so that the precision of comparator is at least able to distinguish 1/2 LSB voltage, namely $3.3/2^{14}/2 = 100$ μV. The comparator speed is more than $2.5 \times 16 = 40$ MHz. Usually the input offset voltage of the latch is 50–100 mV. In order to ensure that the latch can effectively distinguish the input signal, the pre-amplifiers should enlarge the input signal 100 μV to 100 mV, which means the preamplifiers gain is bigger than 1000. The first stage amplifier should be able to enlarge the 100 μV input signal quickly. Therefore it needs a wide bandwidth. Under the premise of a certain gain-bandwidth product, the gain is smaller, and too large gain can lead to amplifier input offset saturation in capacitor C_1. So the final gain of the first amplifier is four and the unity gain bandwidth is 400 MHz. An input offset cancellation technique is used in the second and third amplifiers to avoid the saturation problem, so the gain of the second and third amplifier is about 20 and the unity gain bandwidth is 100 MHz.

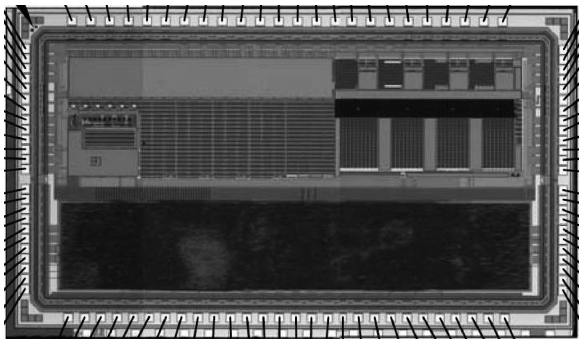

Fig. 7. Layout of the rail-to-rail successive approximation ADC.

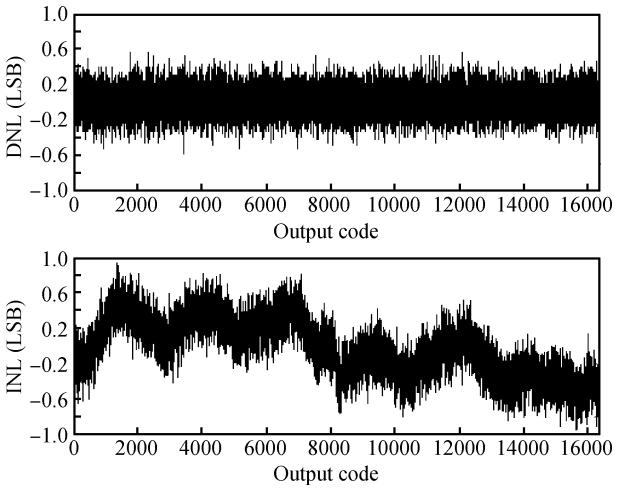

Fig. 8. Measured DNL and INL plots of the SAR ADC.

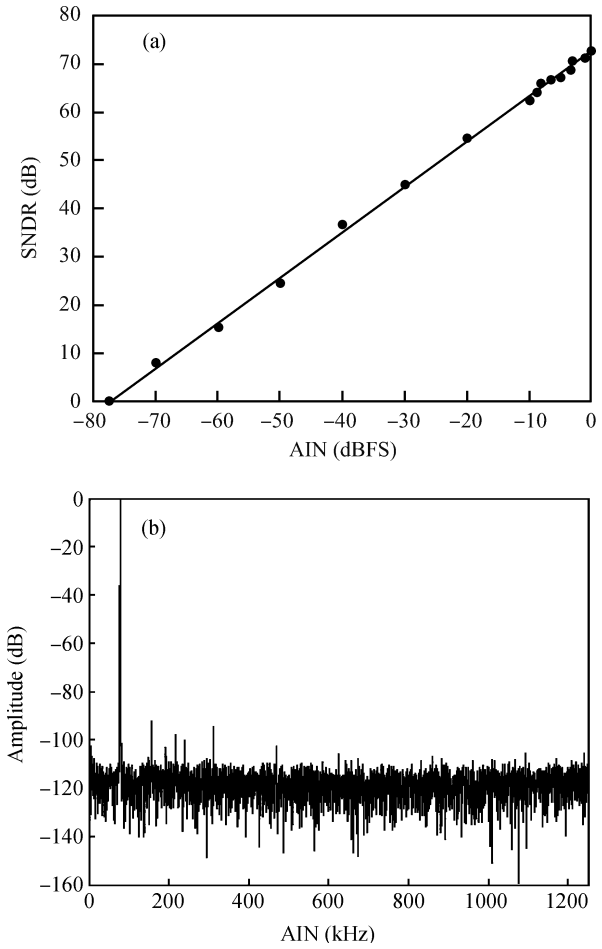

Fig. 9. (a) Measured SNDR versus stimulus amplitude. (b) Output spectrum of the SAR ADC with 0 dBFS 78.125 kHz input.

3.5. Capacitor array mismatch calibration

The correction circuit includes a correction capacitor array and a capacitor self-calibration unit correcting the digital signal of the bit capacitor array according to the digital signal of the correction capacitor array[3]. The correction capacitor array may perform a successive approximation operation after a successive approximation operation of the bit capacitor array is completed. When the digital signals of the first and second calibration capacitors are 11, the capacitor self-calibration unit will add one to the digital signal of the bit capacitor array. When the digital signals of the first and second calibration capacitors are 10 or 01, the digital signal of the bit capacitor array remains the same. When the digital signals of the first and second calibration capacitors are 00, the capacitor self-calibration unit will deduct one from the digital signal of the bit capacitor array. The mismatch calibration arithmetic is shown in Fig. 6.

4. Layout and result

The rail-to-rail successive approximation ADC is fabricated in an SMIC 0.18 μm one-poly four-metal CMOS process. The chip area is approximately 1×2 mm^2. The whole ADC chip is shown in Fig. 7.

The measured differential nonlinearity (DNL) and integral nonlinearity (INL) are shown in Fig. 8. The DNL is in the range of -0.6 to $+0.6$ LSB whereas the INL is within -0.9 to $+0.9$ LSB. Figure 9(a) plots the measure signal-to-noise-and-distortion ratio (SNDR) with respect to the stimulus amplitude. The result proves that the ADC indeed has a rail-to-rail input range. In addition, the ADC achieves a peak SNDR of 72 dB. It corresponds to an effective number of bits (ENOB) of 12 bits. Figure 9(b) shows the measured spectrum where the ADC achieves its peak SNDR. 32768 samples were used to derive the spectrum.

Table 1 lists the summary of the rail-to-rail SAR ADC design. The figure of merit (FOM) is referred here to compare the proposed ADC design with other state-of-the-art works.

$$\mathrm{FOM} = \frac{P}{2 \times f_{\mathrm{B}} \times 2^{(\mathrm{peakSNDR}-1.76)/6.02}}, \qquad (12)$$

where P, f_{B}, peakSNDR denote the total power dissipation, input signal bandwidth, and peak SNDR, respectively.

The FOM is from an energy perspective, instead of a power point of view. It represents the energy required to accomplish an effective ADC conversion step. Table 2 lists the comparison results. The rail-to-rail SAR ADC in this work operates at 1.25 MHz signal bandwidth with 1mW power dissipation, and achieves an FOM = 123 fJ/conversion-step.

5. Conclusion

The rail-to-rail SAR ADC in this paper includes a THA

Table 1. Summary of the rail-to-rail SAR ADC.

Parameter	Value
Process	SMIC 0.18 μm one-poly four-metal CMOS
Chip area	1×2 mm^2
Supply voltage	3.3 V
Clock frequency	40 MHz
Input signal effective bandwidth f_B	1.25 MHz
Peak SNDR	72 dB
ENOB	12 bit
Total power dissipation	1 mW

Table 2. Performance comparison.

Parameter	Ref. [4]	Ref. [5]	Ref. [6]	This work
Tech. (μm CMOS)	0.6	0.18	0.18	0.18
Supply voltage (V)	5	0.9	1	3.3
f_B (kHz)	500	100	50	1250
Peak SNDR (dB)	71.6	47.7	65	72
Power (mW)	15	0.00247	0.025	1
FOM (fJ/conversion-step)	4832	65	167	123

switch voltage gain of less than one and a charge redistribution DAC array with gain compensation capacitors. Measurement results show that the ADC can correctly handle a rail-to-rail input signal. At the same time, the THA input capacitance can be independent of the DAC, to further improve the speed of the SAR ADC.

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