Design of ternary low-power Domino JKL flip–flop and its application*

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Abstract: By researching the ternary flip–flop and the adiabatic Domino circuit, a novel design of low-power ternary Domino JKL flip–flop on the switch level is proposed. First, the switch-level structure of the ternary adiabatic Domino JKL flip–flop is derived according to the switch-signal theory and its truth table. Then the ternary loop operation circuit and ternary reverse loop operation circuit are achieved by employing the ternary JKL flip–flop. Finally, the circuit is simulated by using the Spice tool and the results show that the logic function is correct. The energy consumption of the ternary adiabatic Domino JKL flip–flop is 69% less than its conventional Domino counterpart.

Key words: adiabatic logic; Domino circuit; JKL flip–flop; switch-signal theory

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1. Introduction

Flip–flops are important circuit elements of the clocking sub-system in sequential circuits. They are widely used in very large-scale integrated chips, which employ high-performance clocking systems. Studies show that the energy consumption of the clocking sub-system is 30%–50% of total dynamic power dissipation[1]. So the research of low-power flip–flops is significant for reducing the energy consumption of the clocking sub-system and the total dynamic power dissipation. The adiabatic[2] flip–flops adopt AC pulse power source to change the type of irreversible energy conversion, which changes from electric energy to heat energy. The electric charge stored in the internal circuit nodes is recovered to power the source, realizing circulation utilization and reducing the energy consumption of the circuit.

With the development of semiconductor technology, the area percentage used for wiring in silicon wafers is increasing[3]. It is imposing restrictions on integrated level and information density. Using multiple-valued logic can improve the information content in one wire and reduce the number of wires, hence the area of chip is smaller and the data processing ability is more powerful[4−6]. Domino circuits are commonly used in high-performance circuits, such as processors, registers, and buffers, because of their excellent speed and area properties[7, 8]. So, integrated level and information density can be improved further by combining the multiple-valued logic with Domino circuits. Because of all this, applying adiabatic logic, multiple-valued logic, and Domino circuit to the design of flip–flops, we present a novel design of a low-power ternary Domino JKL flip–flop based on the switch-signal theory. First, the switch-level structure of the ternary adiabatic Domino JKL flip–flop was derived according to the switch-signal theory and its truth table. Then we get the ternary loop operation circuit and ternary reverse loop operation circuit employing the ternary JKL flip–flop. Finally, the circuit was simulated by using the Spice tool and the results showed that the logic function was correct. The energy consumption of the ternary adiabatic Domino JKL flip–flop was 69% less than its conventional Domino counterpart.

2. Switch-signal theory

According to the switch-signal theory[9, 10], we import the switch variables and signal variables, and the corresponding switching algebra and signal algebra, to provide a theoretical basis for the multiple-valued circuits design.

In the switching algebra, α, β are switch variables, their value are T or F, and basic operations are AND(·), OR(+), NOT(−). In the signal algebra, x, y are signal variables, their value used to represent m kinds of voltage signal are 0, 1,…, $m-1$, and basic operations are minimizing operation ($\cap$), maximizing operation ($\cup$), and literal operation ($^ix^i$).

The switch-state and the signal contact with each other, their relevance can be described by two-class connective operations, as shown in Fig. 1. In the connective operation I high-

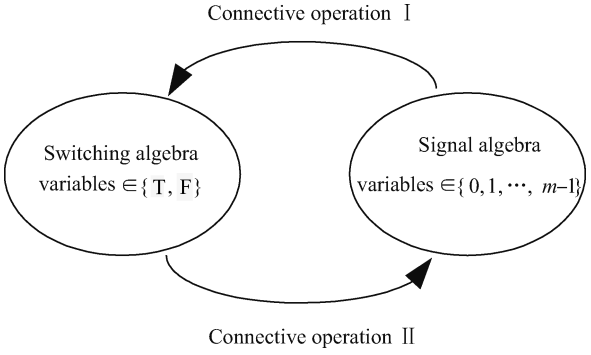

Fig. 1. Switch-signal algebra system.

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threshold and low-threshold comparative operations are introduced, their definitions are:

High-threshold comparative operation:

$$x^t = \begin{cases} \mathrm{T}, & x < t, \\ \mathrm{F}, & x > t. \end{cases} \tag{1}$$

Low-threshold comparative operation:

$${}^t x = \begin{cases} \mathrm{T}, & x > t, \\ \mathrm{F}, & x < t. \end{cases} \tag{2}$$

From Eqs. (1) and (2), their threshold comparative operations have the following characters:

$$\begin{cases} x^t \cdot y^t = (x \cup y)^t, \\ x^t + y^t = (x \cap y)^t. \end{cases} \tag{3}$$

$$\begin{cases} {}^t x \cdot {}^t y = {}^t(x \cap y), \\ {}^t x + {}^t y = {}^t(x \cup y). \end{cases} \tag{4}$$

In the connective operation II, transmission operation and union operation are introduced, their definitions are:

Transmission operation:

$$S * \alpha = \begin{cases} S, & \alpha = \mathrm{T}, \\ \Phi', & \alpha = \mathrm{F}. \end{cases} \tag{5}$$

Union operation:

$$S_1 * \alpha_1 \# S_2 * \alpha_2 = \begin{cases} S_1 * \alpha_1, & \alpha_1 = \mathrm{T}, \\ S_2 * \alpha_2, & \alpha_2 = \mathrm{T}. \end{cases} \tag{6}$$

In Eq. (5), S is transmission source, Φ' is high impedance state, * is transmission operation. In Eq. (6), the transmission operation * takes priority over the union operation #. Also, if $S_1 \neq S_2$ and $\alpha_1 = \alpha_2 = \mathrm{T}$ a voltage conflict arises between sources S_1 and S_2. This condition is not allowed.

Based on Eqs. (5) and (6), the following properties can be derived easily:

Series control law:

$$(x * \alpha) * \beta = x * (\alpha \cdot \beta). \tag{7}$$

Parallel control law:

$$x * \alpha \# x * \beta = x * (\alpha + \beta). \tag{8}$$

Distributive law:

$$(x * \alpha \# y * \beta) * \gamma = x * (\alpha \cdot \gamma) \# y * (\beta \cdot \gamma). \tag{9}$$

From above analysis, voltage switching can be used to control the output voltage signal's grounding short-circuit or sourcing short-circuit and can directly control the output voltage signal's transmission in CMOS circuits.

Table 1. The truth table of ternary JKL flip–flop.

J	0	1	2	d	d	d	d	d	d
K	d	d	d	2	0	1	d	d	d
L	d	d	d	d	d	d	1	2	0
Q	0	0	0	1	1	1	2	2	2
Q'	0	1	2	0	1	2	0	1	2

3. Ternary low-power Domino JKL flip–flop

The truth table of a ternary low-power Domino JKL flip–flop[9] is shown in Table 1. The signals J, K, and L are input signals, Q and Q' are the now state and the next state of the flip–flop, d is an arbitrary value, and $d \in \{0, 1, 2\}$. The truth table illustrates that the next state Q' depends on input signals and now state Q. So the flip–flop is a typical Mealy circuit, the now state Q should get through a buffer to serve as an input signal.

In general, only NMOS transistors or PMOS transistors exist in the evaluation network of a Domino circuit. The Domino circuit cannot distinguish logic 1 directly, so the input signals of ternary JKL flip–flop should get through the ternary literal operation circuit[11] first. Suppose that the output signals, which are J, K, L and now state Q get through the ternary adiabatic Domino literal operation circuit[11], are ${}^0J^0$, ${}^1J^1$, ${}^2J^2$, ${}^0K^0$, ${}^1K^1$, ${}^2K^2$, ${}^0L^0$, ${}^1L^1$, ${}^2L^2$, ${}^0Q^0$, ${}^1Q^1$, ${}^2Q^2$. The amplitude voltage of clk and $\overline{clk}$ is logic 2, the amplitude voltage of $\overline{clk}_1$ is logic 1, $\overline{clk}$ and $\overline{clk}_1$ are in-phase, clk is anti-phase with $\overline{clk}$ and $\overline{clk}_1$. According to the switch-signal theory and the truth table of ternary JKL flip–flop, the structural expressions of the ternary JKL flip–flop basic circuit could be derived.

The next state signal Q' has three logic values: 0, 1, 2. So, different control circuits are needed to generate logic 1 and logic 2 signals. Suppose that Y_1 and Y_2 are the control signals of logic 1 and logic 2 signals, their structural expressions as follows:

$$\begin{aligned} Y_1 = {} & clk * \overline{clk}^{0.5} \# clk * {}^{1.5}\overline{clk} * \Big[{}^{1.5}{}^0Q^0 * {}^{1.5}{}^1J^1 \\ & * \left({}^{1.5}{}^0K^0 + {}^{1.5}{}^1K^1 + {}^{1.5}{}^2K^2 \right) \\ & * \left({}^{1.5}{}^0L^0 + {}^{1.5}{}^1L^1 + {}^{1.5}{}^2L^2 \right) \\ & \#^{1.5}{}^1Q^1 * \left({}^{1.5}{}^0J^0 + {}^{1.5}{}^1J^1 + {}^{1.5}{}^2J^2 \right) \\ & * {}^{1.5}{}^0K^0 * \left({}^{1.5}{}^0L^0 + {}^{1.5}{}^1L^1 + {}^{1.5}{}^2L^2 \right) \\ & \#^{1.5}{}^2Q^2 * \left({}^{1.5}{}^0J^0 + {}^{1.5}{}^1J^1 + {}^{1.5}{}^2J^2 \right) \\ & * \left({}^{1.5}{}^0K^0 + {}^{1.5}{}^1K^1 + {}^{1.5}{}^2K^2 \right) * {}^{1.5}{}^2L^2 \Big] \\ = {} & clk * \overline{clk}^{0.5} \# clk * {}^{1.5}\overline{clk} * \left({}^{1.5}{}^0Q^0 * {}^{1.5}{}^1J^1 \right. \\ & \left. \#^{1.5}{}^1Q^1 * {}^{1.5}{}^0K^0 \#^{1.5}{}^2Q^2 * {}^{1.5}{}^2L^2 \right), \end{aligned} \tag{10}$$

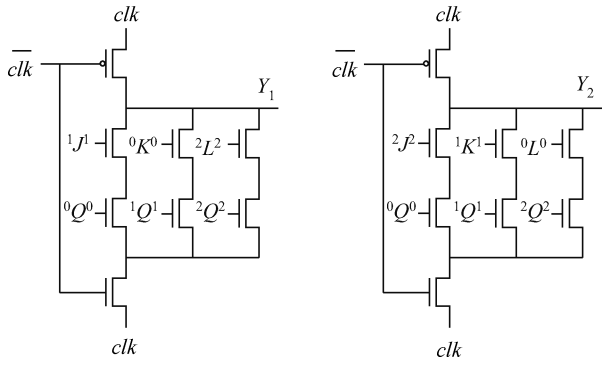

Fig. 2. Control circuits Y_1 and Y_2.

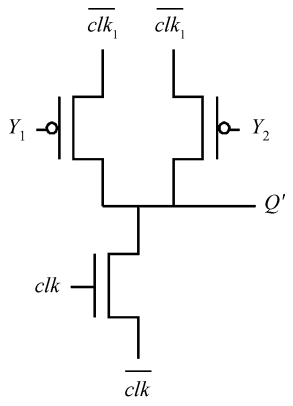

Fig. 3. Q' generating circuit.

$$
\begin{aligned}
Y_2 = {} & clk * \overline{clk}^{0.5} \# clk * {}^{1.5}\overline{clk} * \left({}^{1.5}{}^0Q^0\right. \\
& * {}^{1.5}{}^2J^2 * \left({}^{1.5}{}^0K^0 + {}^{1.5}{}^1K^1 + {}^{1.5}{}^2K^2\right) \\
& * \left({}^{1.5}{}^0L^0 + {}^{1.5}{}^1L^1 + {}^{1.5}{}^2L^2\right) \\
& \#{}^{1.5}{}^1Q^1 * \left({}^{1.5}{}^0J^0 + {}^{1.5}{}^1J^1 + {}^{1.5}{}^2J^2\right) \\
& * {}^{1.5}{}^1K^1 * \left({}^{1.5}{}^0L^0 + {}^{1.5}{}^1L^1 + {}^{1.5}{}^2L^2\right) \\
& \#{}^{1.5}{}^2Q^2 * \left({}^{1.5}{}^0J^0 + {}^{1.5}{}^1J^1 + {}^{1.5}{}^2J^2\right) \\
& * \left({}^{1.5}{}^0K^0 + {}^{1.5}{}^1K^1 + {}^{1.5}{}^2K^2\right) * {}^{1.5}{}^0L^0\Big) \\
= {} & clk * \overline{clk}^{0.5} \# clk * {}^{1.5}\overline{clk} * \left({}^{1.5}{}^0Q^0 * {}^{1.5}{}^2J^2\right. \\
& \#{}^{1.5}{}^1Q^1 * {}^{1.5}{}^1K^1 \#{}^{1.5}{}^2Q^2 * {}^{1.5}{}^0L^0\Big). \qquad (11)
\end{aligned}
$$

In Eq. (10), $clk * \overline{clk}^{0.5}$ indicates that when the $\overline{clk}$ is low voltage, the dynamic node Y_1 is charged by *clk*. The next term indicates that when the $\overline{clk}$ is high voltage, the electric charge stored in dynamic node Y_1 is recovered to *clk* on the basis of ${}^0Q^0, {}^1Q^1, {}^2Q^2, {}^1J^1, {}^0K^0, {}^2L^2$. The circuit expressed by Eq. (11) is similar to this. The structure of control circuits Y_1 and Y_2 can be obtained by Eqs. (10) and (11), as shown in Fig. 2.

The next state signal Q' can be obtained by using control circuits Y_1 and Y_2 to generate logic 1 and logic 2 signals. The structural expressions of next state signal Q' are as follows:

$$
\begin{aligned}
Q' = {} & \overline{clk_1} * clk^{1.5} * Y_1^{1.5} \# \overline{clk} * clk^{1.5} * Y_2^{1.5} \\
& \# \overline{clk} * {}^{1.5}clk \\
= {} & \overline{clk_1} * Y_1^{1.5} \# \overline{clk} * Y_2^{1.5} \# \overline{clk} * {}^{1.5}clk. \qquad (12)
\end{aligned}
$$

According to Eqs. (10) and (11), when Y_1 and Y_2 are low voltage, *clk* is low voltage too, so the structural expressions of next state signal Q' can be simplified as shown in Eq. (12), and the $\overline{clk}$ and $\overline{clk}_1$ would not short out. Because of the amplitude voltage of $\overline{clk}_1$ is logic 1 and the amplitude voltage of $\overline{clk}$ is logic 2, so the work process described by Eq. (12) is as follows: when the Y_1 is low voltage, next state signal Q' exports logic 1; when Y_2 is low voltage, next state signal Q' exports logic 2; when *clk* is high voltage, the electric charge stored in node Q' is recovered to $\overline{clk}$, next state signal Q' exports logic 0. The circuit structure expressed by Eq. (12) is shown in Fig. 3. And the whole ternary JKL flip–flop basic circuit can be consisted of the circuits shown in Figs. 2 and 3. Its circuit symbol and clocking waveforms are shown in Fig. 4.

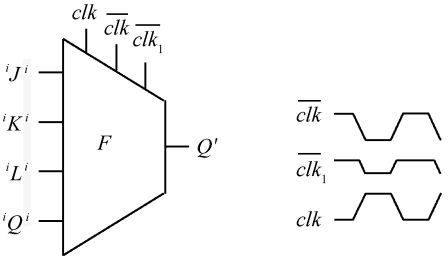

Fig. 4. Ternary JKL flip–flop basic circuit symbol and clocking waveforms.

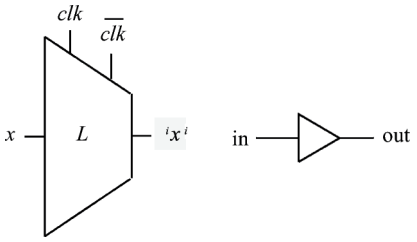

Fig. 5. Symbols of literal operation circuit and buffer.

Table 2. The truth table of the ternary loop operation circuit.

X	0	1	2
$X^{\rightarrow}$	1	2	0

The whole ternary JKL flip–flop consists of ternary JKL flip–flop basic circuit, ternary adiabatic Domino literal operation circuit[11], and adiabatic Domino buffer. The structure of the adiabatic Domino buffer is similar to ternary adiabatic Domino literal operation circuit; the difference being that the amplitude of the AC pulse power source in waveform transformation sub-circuits is diverse. The output signal of the adia-

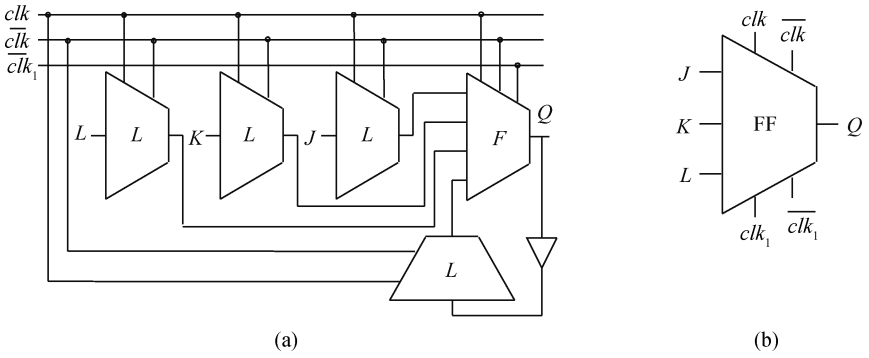

Fig. 6. Ternary adiabatic Domino JKL flip–flop. (a) Structure. (b) Symbol.

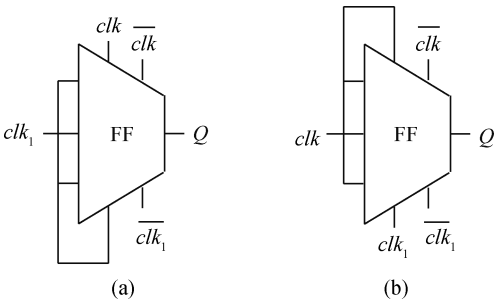

Fig. 7. (a) Ternary adiabatic Domino loop operation circuit. (b) Ternary adiabatic Domino reverse loop operation circuit.

batic Domino buffer is delayed by half a clock period as compared with the input signal. The symbols of literal operation circuit and buffer are shown in Fig. 5. Figure 6 is the structure and symbol of ternary JKL flip–flop, in which the buffer adopt three clocks:clk, $\overline{clk}$, clk_1.

4. Ternary loop and reverse loop operation circuit

The definition of ternary loop operation[12] is that:

$$X^{\rightarrow} = (X + 1) \bmod 3. \tag{13}$$

X and $X^{\rightarrow}$ are the input and output signal. Table 2 is the truth table of a ternary loop operation circuit. Compared with the truth table of the ternary JKL flip–flop, we can realize that their logical function is the same when the input signal of the ternary JKL flip–flop $J = K = L = 1$. So the ternary loop operation circuit can be achieved using the ternary JKL flip–flop.

The ternary adiabatic Domino loop operation circuit can be obtained by connecting the input signal J, K, L with the clk_1 in the ternary adiabatic Domino JKL flip–flop, as shown in Fig. 7(a). It can realize the function of counting the clock pulses. Similarly, the ternary adiabatic Domino reverse loop operation circuit can be obtained by connecting the J, K, L with the clk, as shown in Fig. 7(b).

5. Simulation and conclusion

The circuits mentioned above are simulated using the parameters of TSMC 0.25 μm CMOS device by using the Spice tool, the waveform is shown in Fig. 8. The voltages corresponding to logic values 0, 1, 2 are 0 V, 1.25 V, 2.5 V. The amplitudes of clk_1, $\overline{clk}_1$, clk, $\overline{clk}$ are 1.25 V, 1.25 V, 2.5 V, 2.5 V. The frequency of all clocks is 20 MHz. The breadth length ratio for NMOS transistor is 0.36 μm/0.24 μm, for PMOS transistor is 0.72 μm/0.24 μm. The load capacitance is 10 fF. J, K, L are the input signals, Q is the output signal. Figure 8 shows that the logical function of the circuits is consistent with the ternary JKL flip–flop truth table.

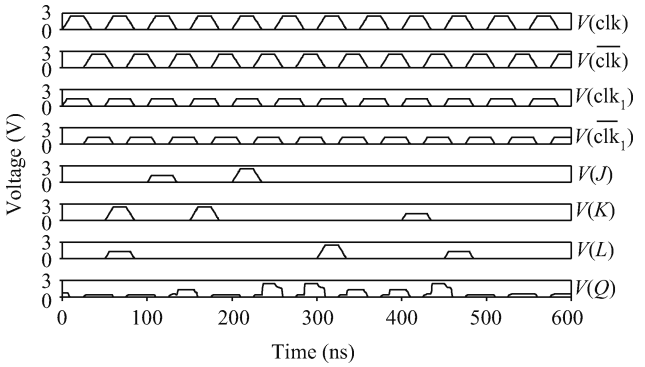

Fig. 8. Simulation waveforms of ternary adiabatic Domino JKL flip–flop.

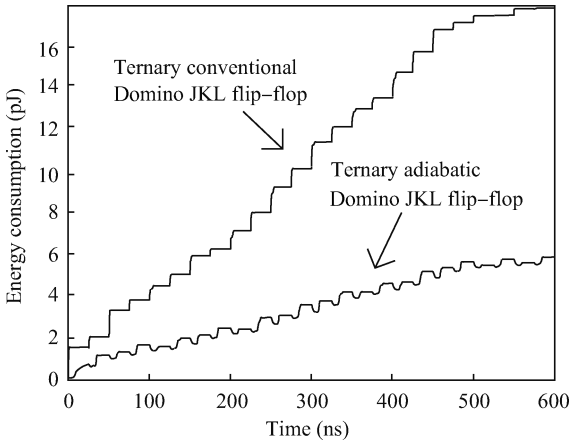

Fig. 9. Energy consumption comparison.

We compared the ternary adiabatic Domino JKL flip-flop energy consumption with the conventional Domino counterpart in the same parameters, and the result is shown in Fig. 9.

The conventional Domino JKL flip–flop adopts DC power source and the structure is almost the same as the ternary adiabatic Domino JKL flip–flop. The curve of the ternary adiabatic Domino JKL flip–flop energy consumption indicates that the electric charge is recovered to the power source, realizing circulation utilization and reducing energy consumption. Analytically, the ternary adiabatic Domino JKL flip–flop can save energy consumption by about 69%, showing excellent low-power characteristics.

According to the switch-signal theory, a novel design of low-power ternary Domino JKL flip–flop on switch-level was proposed. The scheme combines the adiabatic logic, multiple-valued logic, and Domino circuit. It also changes the method of irreversible energy conversion, which changes from electric energy to heat energy, reducing the energy consumption and improving the information density. On this basis, the ternary loop and reverse loop operation circuit are realized, promoting the practicability of the ternary digital system.

References

[1] Karimiyan H, Sayedi S M, Saidi H. Low-power dual-edge triggered state-retention scan flip–flop. IET Computers & Digital Techniques, 2010, 4(5): 410

[2] Reddy N S S, Satyam M, Kishore K L. Cascadable adiabatic logic circuits for low-power applications. IET Circuits, Devices & Systems, 2008, 2(6): 518

[3] Zhang W, Wu N, Hashizume T, et al. Multiple-valued logic gates using asymmetric single-electron transistors. 39th International Symposium on Multiple-Valued Logic, 2009: 337

[4] Lin S, Kim Y B, Lombardi F. CNTFET-based design of ternary logic gates and arithmetic circuits. IEEE Trans Nanotechnol, 2011, 10(2): 217

[5] Lin Mi, Lü Weifeng, Sun Lingling. A design for triple-valued NAND and NOR gates based on resonant tunneling devices. Journal of Semiconductors, 2007, 28(12): 1983

[6] Moaiyeri M H, Doostaregan A, Navi K. Design of energy-efficient and robust ternary circuits for nanotechnology. IET Circuits, Devices & Systems, 2011, 5(4): 285

[7] Akl C J, Bayoumi M A. Single-phase SP-Domino: a limited-switching dynamic circuit technique for low-power wide fan-in logic gates. IEEE Trans Circuits Syst II: Express Briefs, 2008, 55(2): 141

[8] Wang Jinhui, Gong Na, Feng Shoubo, et al. A novel p-type Domino AND gate design for sub-65 nm CMOS technologies. Journal of Semiconductors, 2007, 28(11): 1818

[9] Wu Xunwei, Chen Xiexiong. Design principle of multi-valued logic circuits. Hangzhou University Press, 1994: 1 (in Chinese)

[10] Hang Guoqiang, Lu Huijuan. Novel current-mode CMOS ternary Schmitt trigger. Journal of Zhejiang University (Engineering Science), 2006, 40(7): 1141

[11] Yang Q, Wang P, Zheng X. Design of ternary adiabatic Domino literal operation circuit on switch-level. Journal of Circuits and Systems, 2012, 17(4): 36

[12] Wang Pengjun, Li Kunpeng, Mei Fengna, et al. Design of ternary adiabatic counter on switch-level. Journal of Zhejiang University (Engineering Science), 2011, 45(8): 1502