Design of low noise class D amplifiers using an integrated filter

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Abstract: This paper investigates the noise sources in a single-ended class D amplifier (SECDA) and suggests corresponding ways to lower the noise. The total output noise could be expressed as a function of the gain and noises from different sources. According to the function, the bias voltage (V_B) is a primary noise source, especially for a SECDA with a large gain. A low noise SECDA is obtained by integrating a filter into the SECDA to lower the noise of the V_B. The filter utilizes an active resister and an 80 pF capacitance to get a 3 Hz pole. A noise test and fast Fourier transform analysis show that the noise performance of this SECDA is the same as that of a SECDA with an external filter.

Key words: class D amplifier; low noise; filter; noise derivation

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1. Introduction

Class D amplifiers are gaining increasing prevalence due to their higher power-efficiency performance compared to traditional linear amplifiers[1, 2]. Such an advantage is obtained by controlling the output transistors to operate in the fully ON or fully OFF status instead of the active region, and makes class D amplifiers extremely attractive for systems-on-chip (SoC) in mobile devices and low-power applications, for which battery life and heat dissipation are crucial parameters[3].

It is widely recognized that noise is a key factor in the total harmonic distortion plus noise (THD+N) and signal to noise ratio (SNR) which are primary factors affecting the quality of the sound. Unfortunately, the relatively large noise is a potential drawback of class D amplifiers compared with their linear counterparts due to the combination of linear and switching mode operations[4, 5]. Ways to lower the noise in a class D amplifier have been discussed for a long time[6, 7]. In this paper, a low cost way to get a low noise class D amplifier is proposed. Noise sources in a single-ended class D amplifier (SECDA) are investigated and expressions to describe the relationship between the noise and the gain of a SECDA are derived. Then, an integrated filter is applied into the design of the SECDA to lower the noise. Lastly, the noise test and fast Fourier transform (FFT) analysis results are shown.

2. Design of low noise class D amplifiers

2.1. The sources of noise in class D amplifiers

Figure 1 shows the schematic diagram of a SECDA. The input stage of the SECDA comprises amplifiers A1 and A2 configured to set the gain and to enhance the load ability of an input audio signal (V_{IN}). The amplifier A1 is configured to receive V_{IN} via an input capacitance (C_{IN}) and a bias voltage signal (V_B) directly. It operates substantially as an inverting amplifier with a gain V_{O1}/V_{IN} that is decided by R_F/R_{IN}. The amplifier A2 operates approximately as a unity gain inverting amplifier to provide a signal V_{O2} whose phase is 180° different from V_{O1}. So the gain from V_{IN} to the differential signal V_{O12} ($V_{O1} - V_{O2}$) is

$$A_{VIN} = 2\frac{R_F}{R_{IN}}. \tag{1}$$

A modulation stage of the SECDA compares the differential signal V_{O12} with a high frequency carrier (> 200 kHz) V_{SAW} to generate a pulse width modulation (PWM) signal. This PWM signal is further amplified by a power stage in order to drive a speaker[8]. The gain of modulation stage is

$$A_{VM} = \frac{R_4}{R_3}. \tag{2}$$

For better understanding, the A_{VM} is assumed to be a constant value of 2 here and in the following text. And thus the gain of the SECDA could be expressed as

$$A_V = 2\frac{R_F R_4}{R_{IN} R_3} = 4\frac{R_F}{R_{IN}}. \tag{3}$$

V_B is a bias voltage which may be equal to half of the power supply voltage ($V_{DD}/2$) or other constant voltage. The noise of V_B may be amplified by amplifier A1 and A2. Assuming V_{IN} is from an ideal voltage source, then

$$V_{O12} = \frac{2R_F C_{IN} S}{1 + R_{IN} C_{IN} S} V_B. \tag{4}$$

Normally, the RC value of the input filter is set higher than 50 ms to pass audio frequency (20 Hz–20 kHz). That means the low frequency (lower than 20 Hz) noise on V_B will be filtered while the high frequency noise on V_B will be amplified for $2R_F/R_{IN}$ times. For noise with a frequency higher than 20 Hz, the gain from V_B to the output of the SECDA signal is

$$A_{VB} = 2\frac{R_F R_4}{R_{IN} R_3} = A_V. \tag{5}$$

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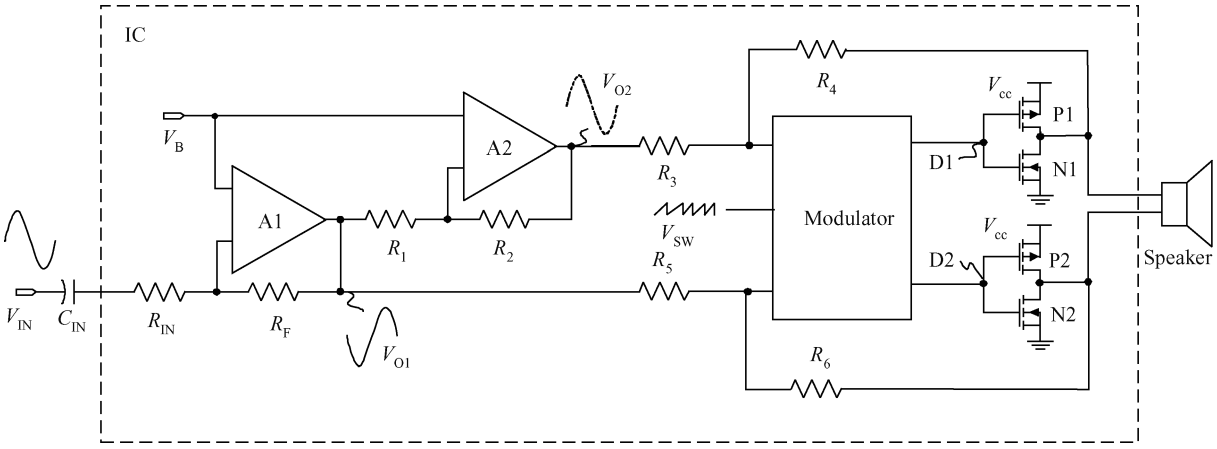

Fig. 1. A single-ended input class D amplifier.

So, the output noise voltage due to the noise on V_B is

$$\overline{V_{OB}^2} = \overline{V_B^2} A_V^2. \tag{6}$$

According to Ref. [9], thermal noise on R_{IN} and R_F can be viewed as an equivalent input noise which is given by

$$\overline{V_{IR}^2} = 4kT(R_{IN} \parallel R_F)\Delta f. \tag{7}$$

Wherein k is the Bolzmann's constant and Δf is the bandwidth in Hz. At room temperature $4kT$ is equal to 1.66×10^{-20} V·C. So, the output noise voltage due to the thermal noise on R_{IN} and R_F is

$$\overline{V_{OR}^2} = 4kT(R_{IN} \parallel R_F)\Delta f A_V^2. \tag{8}$$

The other noise sources, such as the thermal noise on R_1 and R_2, high switching signals, jitter in switching frequency, and substrate injection also contribute to a large part of the total output noise. However, noise due to these sources nearly always does not change with the gain. Assuming the total noise due to the above sources is $\overline{V_{OC}^2}$. Since all the noise sources are independent from each other, the total output noise is given by

$$\begin{aligned}\overline{V_O^2} &= \overline{V_{OB}^2} + \overline{V_{OR}^2} + \overline{V_{OC}^2} \\ &= \overline{V_B^2} A_V^2 + 4kT(R_{IN} \parallel R_F)\Delta f A_V^2 + \overline{V_{OC}^2}.\end{aligned} \tag{9}$$

Noise from the modulation stage could be suppressed by increasing the order of the loop filter[3]. But noise from the input stage may be more serious since it may be amplified rather than suppressed by the modulation stage. According to Eq. (9), output noise can be lowered by reducing the noise on V_B and/or applying a small $R_{IN} \| R_F$. For $R_{IN} \| R_F = 60$ kΩ, $\Delta f = 20$ kHz, and $A_V = 10$, $\overline{V_{OR}^2}$ is only about $(4.5 \times 10^{-6})^2$. So, reducing the noise on V_B is more important when considering reducing the total output noise.

The traditional way to get a relative low noise bias voltage is to use a low pass RC filter, as shown in Fig. 2. Normally, to get a 5 Hz pole, an integrated R_B is set around several kilo ohms and an external capacitance C_{BE} is set around 1 μF. As C_{BE} is too large to be integrated inside the chip, the external large capacitance, an additional pin for connecting the capacitance,

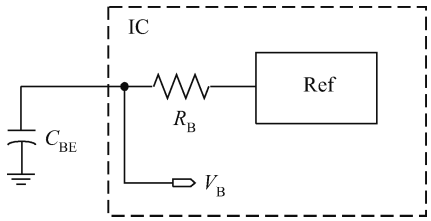

Fig. 2. A filter with external capacitance.

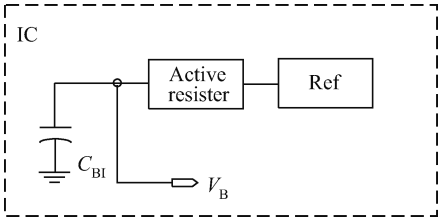

Fig. 3. The proposed integrated filter.

bonding wires, and the pad layout increase the cost of the class D amplifier.

2.2. Design of an integrated filter with a 3 Hz pole

As shown in Fig. 3, to obtain a low noise bias voltage with a low cost, an integrated filter with a 600 MΩ active resister and 80 pF capacitance C_{BI} is proposed.

Figure 4 depicts the schematic circuit of the proposed filter. A switch, M1, is used to set the gate voltage of switches M2 and M3. M3 and C_{B1} form a filter to filter the reference voltage V_{REF} and generate a low noise signal V_B. M4 and R_7 provide a current to charge C_{B1} in a short time which depends on the value of M2 and C_1. The current of M1 could be given by

$$I_{D1} = \frac{1}{2} K \frac{W_1}{L_1} (V_{GS} - V_{TH})^2. \tag{10}$$

Wherein, K is a ratio decided by the process, W_1 and L_1 is the channel width and length of M1, V_{GS} is the voltage difference between the gate and the source, and V_{TH} is the threshold voltage of M1. Unlike M1 which is working in the saturation region, M3 is working in the linear region[10]. The current

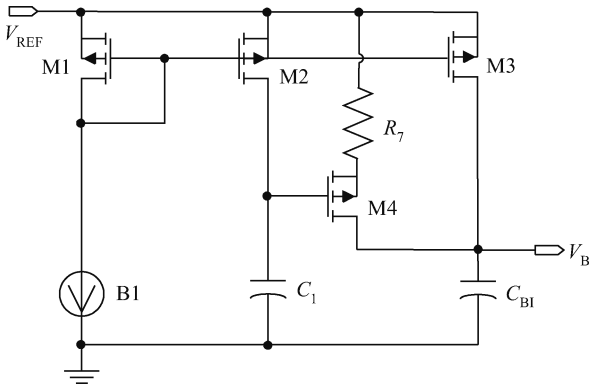

Fig. 4. The proposed filter.

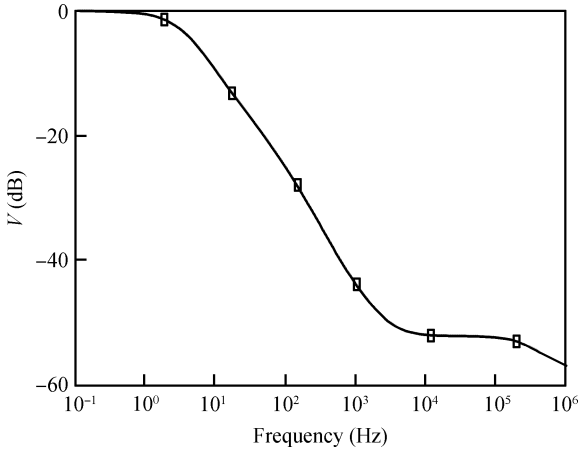

Fig. 5. Simulation result of the proposed filter.

flowing through M3 could be given by,

$$I_{D3} = K\frac{W_3}{L_3}(V_{GS} - V_{TH})V_{DS3}. \tag{11}$$

V_{DS3} is the voltage difference between the drain and source. The resistance of M3 could be given by,

$$R_{M3} = \frac{\partial V_{DS}}{\partial I_{DS}} = \frac{\sqrt{W_1}L_3}{\sqrt{2KI_{D}L_1}\times W_3}. \tag{12}$$

Wherein $W_1/L_1 = 4\times10^3$, $W_3/L_3 = 10^{-2}$ and I_{D1} is about 1 μA, K is about 50 μA/V^2. The pole of the filter is,

$$f_{M3} = \frac{1}{2\pi R_{M3}C_{BI}}. \tag{13}$$

Figure 5 shows the frequency response simulation result of the filter. The filter has a 3 Hz pole, and taking account the 80 pF capacitance, the resistance is about 600 MΩ.

The current of M3 is so small that it may take too long to charge C_{B1} to the final value. The current through M4 is used to charge C_{B1} when the voltage on C_1 is too small. M4 will continue to charge C_{B1} until the voltage on C_1 is high enough to cut off M4. Then, C_{B1} will be charged by M3 only.

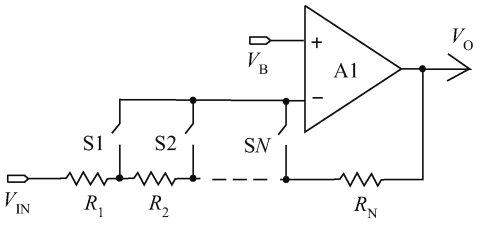

Fig. 6. A gain control unit.

3. Design of a low noise class D amplifier with gain control

According to Eq. (9), noise from different sources can be obtained by measuring the total output noise at different gains if $R_{IN}\|R_F$ is a function of gain. This could be achieved by using a potentiometer ($R_{IN}+R_F$) configured to determine the unit gain according to a digital control signal (D_G). Figure 6 shows a commonly used gain control unit to explain a method to control the gain of the SECDA. D_G is a 6 bits digital data signal that is decoded to turn ON/OFF switches S_1–S_N. Assuming the D_G is 111111, switch S1 is ON (closed) while the others are OFF (opened), the gain of gain control unit is

$$A_{V1} = (R_2 + R_3 + \cdots + R_N)/R_1. \tag{14}$$

Then, if DG is changed to 111110, the gain is given by

$$A_{V2} = (R_3 + R_4 + \cdots + R_N)/(R_1 + R_2). \tag{15}$$

A variety of gains could be obtained once the switches are in different ON or OFF states according to the different status of the D_G.

As shown in Fig. 7, a low noise class D amplifier is obtained by integrating the filter shown in Fig. 2 into the class D amplifiers. The $R_{IN} + R_F$ is set at 300 kΩ, and an ADC is utilized to generate a 6 bit D_G according to a volume control signal V_{OL}. The gain of the class D amplifier varies from –75 to 24 dB with 64 steps. According to Eq. (3), $R_{IN}\|R_F$ could be expressed as

$$R_{IN} \parallel R_F = \frac{1.2\times10^6\times A_V}{(4+A_V)^2}. \tag{16}$$

Then, substituting Eq. (16) into Eq. (9), it is given by:

$$\begin{aligned}\overline{V_O^2} &= \overline{V_{OB}^2} + \overline{V_{OR}^2} + \overline{V_{OC}^2}\\ &= \overline{V_B^2}A_V^2 + 4kT\frac{1.2\times10^6\times A_V}{(4+A_V)^2}\Delta f A_V^2 + \overline{V_{OC}^2}\\ &= \overline{V_B^2}A_V^2 + \frac{4\times10^{-10}\times A_V^3}{(4+A_V)^2} + \overline{V_{OC}^2}.\end{aligned} \tag{17}$$

4. Simulation and test results

The class D amplifier described above has been fabricated in HHNEC with 0.6 μm Bi-CMOS technology. The layout micrograph of the Class D amplifier (left and right channel) is

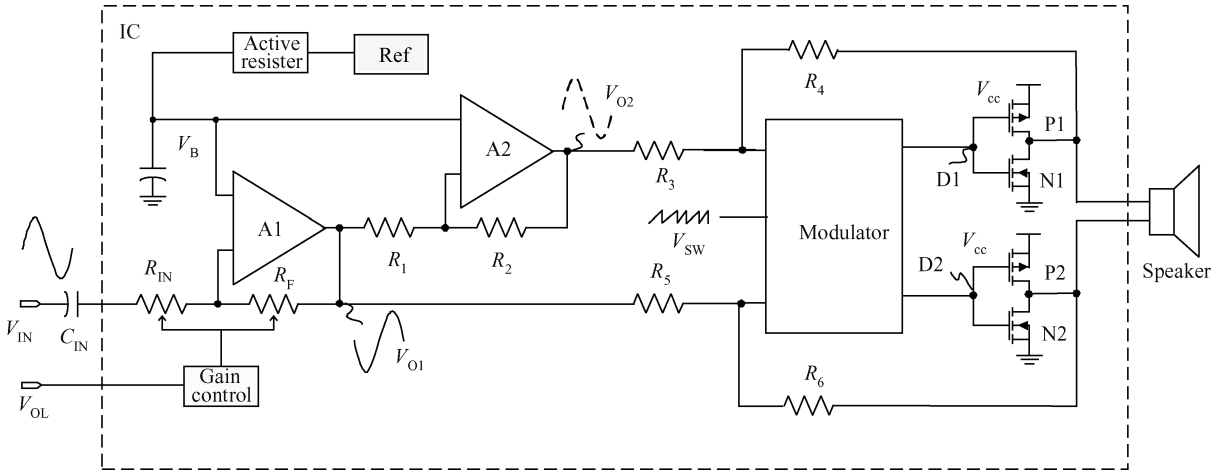

Fig. 7. The proposed low noise class D amplifier.

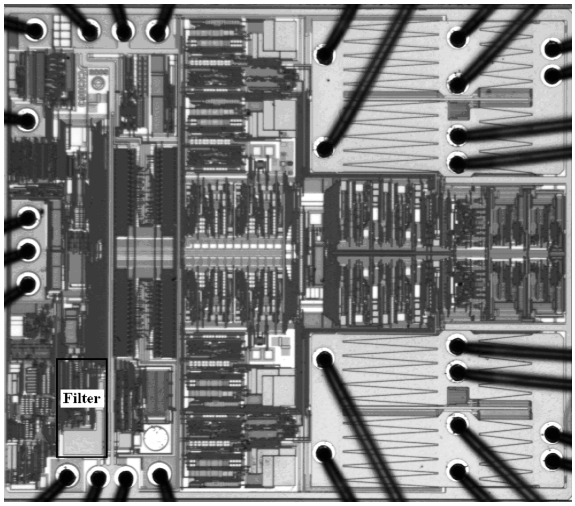

Fig. 8. Layout micrograph of the class D amplifier.

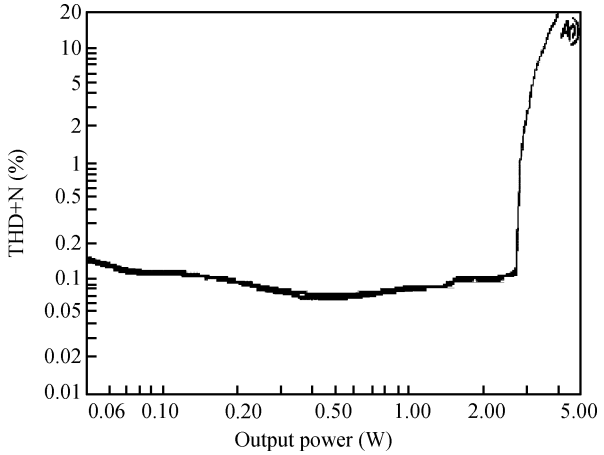

Fig. 9. THD+N versus output power with a 4 Ω speaker.

shown in Fig. 8. The voltage reference and the filter are placed far away from the switching areas and are well isolated from other areas. The filter takes about 0.05 mm^2 out of the class D amplifier, which is about 1% of the die size.

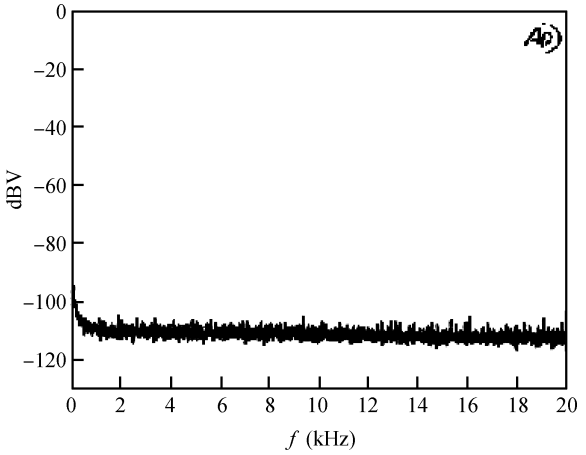

Fig. 10. FFT analysis of the output signal.

Figure 9 shows the test results of the THD+N as a function of output power. The V_{CC} is 5 V, the input signal is set at 1 kHz, and the load is 4 Ω. For small output amplitude cases, THD+N are limited by the noise and hence decreases as the output power increases. The max power for each channel with a 8 Ω load is about 3 W. The line with a lower THD+N is the test result for the class D amplifier with external filter while the line with a higher THD+N is the test result for the class D amplifier with an integrated filter. The two lines are so close that there would be no obvious difference in THN+N performance.

The noise (20 Hz–20 kHz) of the output signal is about 100 μV when the gain is set at around 20 dB. Figure 10 depicts the FFT results of the output signal. This result is substantially the same as the test result of a class D amplifier with an external 1 μF filter[11].

Figure 11 depicts the measurement (Meas) result of the noise at different gain. Observing the tested line, the total output noise is about 42 μV when the gain is very low, and then rises quickly as the gain increases. The theoretical (Theo) line shown in Fig. 11 depicts Eq. (17) with $\overline{V_{OC}} = 42$ μV and $\overline{V_B} = 8.4$ μV. So, Equation (17) is inconsistent with the test result.

Figure 11 also depicts the noise due to the thermal noise on R_{IN} and R_F (V_{OR}) and the output noise due to noise on

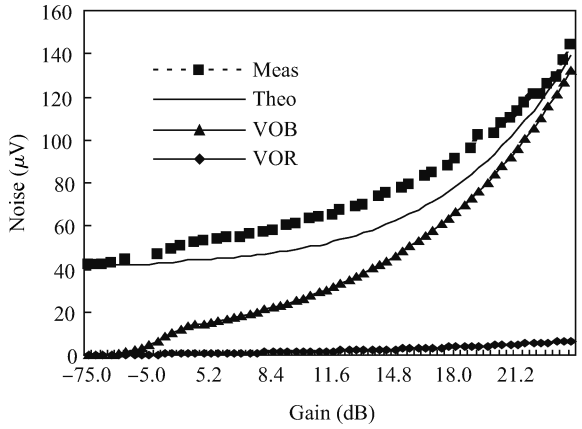

Fig. 11. Noise at different gains.

V_B (V_{OB}). As the gain changes, V_{OR} changes slowly while V_{OB} changes quickly. V_{OB} is nearly equal to the output noise when the gain is larger than 20 dB. So, for a SECDA, the output noise due to noise on the bias voltage plays a more important role in the output noise, especially when the gain of the amplifier is high.

5. Conclusion

This paper investigates and verifies the relationship among noise, especially the sources of noise and gain. For a single-ended class D amplifier, the bias voltage is a primary variable noise source. The noise on bias voltage is amplified by both the input stage and the modulation stage, which plays an important role in the output noise, especially when the gain of the amps is high.

This paper presents an integrated filter to lower the noise of bias voltage. The filter can lower the noise of bias voltage to around 10 μV and the noise of the SECDA to 100 μV at a 20 dB gain. Test results and FFT analysis show that it is substantially the same performance as an amplifier using an external filter. The presented filter could also used for LDO, bandgap voltage references and other applications.

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