Effect of underlap and gate length on device performance of an AlInN/GaN underlap MOSFET

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Abstract: We investigate the performance of an 18 nm gate length AlInN/GaN heterostructure underlap double gate MOSFET, using 2D Sentaurus TCAD simulation. The device uses lattice-matched wideband $Al_{0.83}In_{0.17}N$ and narrowband GaN layers, along with high-k Al_2O_3 as the gate dielectric. The device has an ultrathin body and is designed according to the ITRS specifications. The simulation is done using the hydrodynamic model and interface traps are also considered. Due to the large two-dimensional electron gas (2DEG) density and high velocity, the maximal drain current density achieved is very high. Extensive device simulation of the major device performance metrics such as drain induced barrier lowering (DIBL), subthreshold slope (SS), delay, threshold voltage (V_t), I_{on}/I_{off} ratio and energy delay product have been done for a wide range of gate and underlap lengths. Encouraging results for delay, I_{on}, DIBL and energy delay product are obtained. The results indicate that there is a need to optimize the I_{off} and SS values for specific logic design. The proposed AlInN/GaN heterostructure underlap DG MOSFET shows excellent promise as one of the candidates to substitute currently used MOSFETs for future high speed applications.

Key words: MOS-HEMT; underlap; heterostructure; ultrathin body; interface traps; effective mass
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1. Introduction

AlInN has recently attracted considerable attention as a promising candidate for replacing the conventionally employed AlGaN barrier layer in GaN based HEMT and metal oxide semiconductor HEMTs (MOS-HEMT) devices[1−4]. Lattice matched AlInN/GaN heterostructure devices have shown superior performance in comparison to conventional AlGaN/GaN heterostructure devices, primarily because of the substantially higher spontaneous polarization-induced two-dimensional electron gas (2DEG) density[5]. Lattice matching in AlInN/GaN heterostructures also avoids the problem of interface and bulk defects occurring in AlGaN/GaN structures with high Al content due to strain relaxation[6]. $Al_{0.83}In_{0.17}N$ is nearly lattice-matched to GaN, and high-quality AlInN/GaN heterostructure can be grown by metal-organic vapor phase epitaxy (MOVPE)[7]. High electron mobility in the range of 1200 to 2000 $cm^2/(V{\cdot}s)$ and high 2DEG sheet carrier densities of 3.2×10^{13} cm^{-2} have been reported previously[7, 8]. As a consequence of lattice matching, less strain and lattice defects occur at the interface.

In HEMT devices, gate leakage current is an important factor limiting its performance and reliability[5]. Thus, a thin gate dielectric oxide layer is often inserted between the gate metal and the AlInN wideband gap barrier layer[9−12] forming a MOS-HEMT. The use of a gate oxide helps to improve gate contact, reduce gate leakage and increase drain current, however, it partly reduces the transconductance because of a larger gate-to-channel separation[12]. Furthermore, there is shift of V_t due to a decrease of gate-to-source capacitance (C_{gs}) in the MOS-HEMT devices. MOS-HEMT devices exhibit a gate leakage reduction of six to ten orders of magnitude compared to a Schottky barrier HEMT of similar design[13].

Remarkable progress has been made recently in the fabrication and device performance of single gate MOS-HEMT devices, using InP/InGaAs, AlGaN/GaN and AlInN/GaN heterostructures[14−16]. The effect of atomic layer deposited (ALD) high k HfO_2, ZrO_2, and Al_2O_3, on the gate current leakage are also analyzed[17]. Although several single gate MOS-HEMT devices are reported, there are no reported double gate and underlap double gate MOS-HEMT structures to date, to the best of our knowledge.

In this paper, for the first time, we report an 18 nm gate length AlInN/GaN underlap DG MOSFET. Extensive device simulations of major device metrics such as drain induced barrier lowering (DIBL), subthreshold slope (SS), delay, V_t, I_{on}/I_{off} ratio, and energy delay product have been done for a wide range of gate lengths (L_g) and underlap lengths (L_{un}). Underlap DG MOSFET structures reduce the short-channel effects considerably, but degrade device performance by reducing the drive current due to an increase in the effective channel length with underlap. On the contrary, HEMT devices offer high ON current and ultrafast performance due to III–V material in the channel. However, their off-state control, gate leakage, and scalability need to be addressed[18]. Thus, in this work, we intend to arrive at a novel device that takes into account

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Table 1. Physical properties of $Al_{0.83}In_{0.17}N$ and GaN.

Material	GaN	$Al_{0.83}In_{0.17}N$
E_g (eV)	3.4	4.7
CBO (eV)	0.57	–
VBO (eV)	0.73	–
ε_o	9.5	11.7
Lattice constant (Å)	3.186	3.190
μ_e (cm^2/(V·s))	940	1540
μ_h (cm^2/(V·s))	22	82

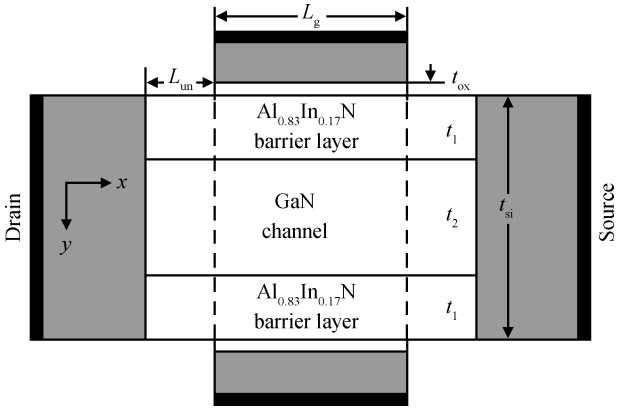

Fig. 1. Heterostructure underlap DG MOSFET showing underlap near the source and drain sides. The channel consists of an undoped narrow bandgap GaN ($t_2 = 4$ nm) region and two wide bandgap $Al_{0.83}In_{0.17}N$ ($t_1 = 1$ nm) regions. Source/drain region doping is 10^{20} cm^3, with 5 nm length. The gate length $L_g = 18$ nm, the equivalent oxide thickness EOT is 1.2 nm, and body thickness $t_{si} = 6$ nm.

both high performance and low leakage, but remains in the quasi-MOS regime, which makes it achievable to fabricate the device without wide deviation from existing technology. The newly proposed III–V heterostructure underlap DG MOSFET consists of a double heterostructure in the channel employing AlInN/GaN, with buried channels at the hetero interface. The device is intended to attain a high ON-state current requirement using bulk conduction arising from an HEMT-like mechanism, and good off-state control by using a DG MOSFET-like mechanism[18].

2. Device description

We analyze the performance of an $Al_{0.83}In_{0.17}N$/GaN underlap DG MOSFET device (Fig. 1) having a gate length of 18 nm, symmetrical underlap lengths of 5 nm on both the source and drain sides, with an undoped ultrathin body (UTB). The source/drain region lengths are 5 nm; the front and back gate has a high-k Al_2O_3 dielectric with an equivalent oxide thickness of 1.2 nm. The AlInN and GaN layers are kept undoped to minimize mobility degradation due to scattering. The device source/drain regions are doped at 10^{20} cm^3 and use an abrupt doping profile at the source and drain ends. A narrow bandgap GaN layer ($t_2 = 4$ nm) is sandwiched between the two wide bandgap AlInN barrier layers ($t_1 = 1$ nm) and the channel is confined at the heterostructure interfaces. The barrier layer used has the conduction band edge offset with the channel and is nearly lattice matched with the narrowband layer to minimize traps at its interface with the channel. The barrier

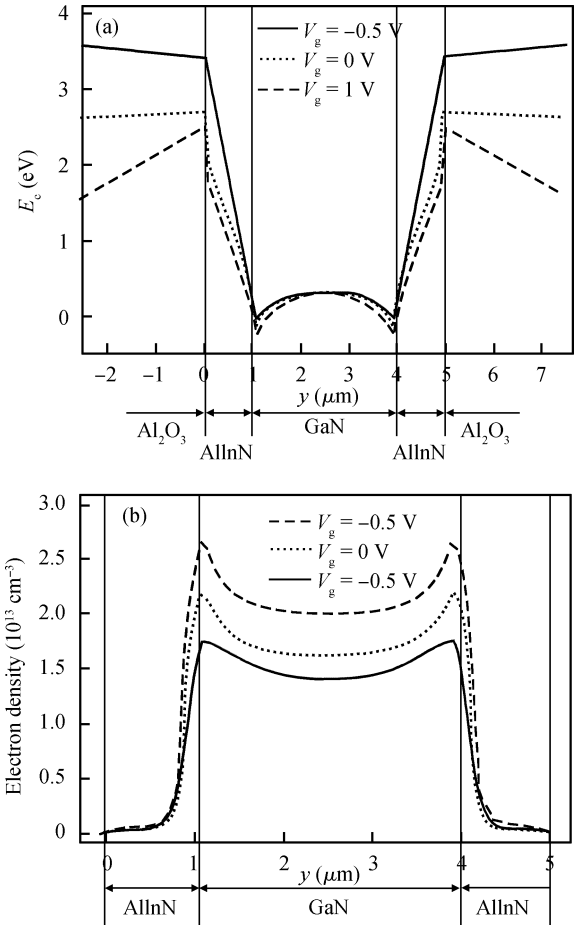

Fig. 2. (a) Simulated conduction band profile and (b) electron density distribution for $V_{gs} = -0.5$ V, 0 V, 1 V, at the center of the gate along the direction normal to the transport direction for $V_{ds} = 0$ V. 2DEG confined at the AlInN/GaN interface is observed.

layers provide: (1) strong carrier confinement in the quantum well at the hetero interface; and (2) minimizes junction leakage and MOSFETs off-state leakage current I_{off}[19]. The physical properties of the narrow bandgap GaN and the wide bandgap $Al_{0.83}In_{0.17}N$ are listed in Table 1.

Figure 2(a) shows the conduction band (E_c) distribution at the center of the gate in a direction normal to the transport direction for $V_{gs} = -0.5$ V, 0 V and 1 V at $V_{ds} = 0$ V. In the off-state $V_{gs} < -0.5$ V, downward shift of E_c in the whole region under the gate is observed. For $V_{gs} > -0.5$ V channel is formed at the AlInN/GaN interface and 2DEG density increases with V_{gs}. With the increase in V_{gs} beyond 1 V, E_c in Al_2O_3 bends downwards and a very slightly increase in 2DEG density is observed. Figure 2(b) shows the spatial distribution of electrons in the channel at the center of the gate, along the y direction. A peaking of electron density near the AlInN/GaN interface ($y = 1$ nm) indicates the confinement of 2DEG. A significant increase in confinement occurs as V_{gs} increases from –0.5 to 1 V.

3. Simulation model calibration and experimental comparison

For validating the simulation model, comparison of the

Table 2. Polarization charge density at each interface.

Parameter	n_{sp} (GaN) (10^{13} cm^{-2})	n_{sp} (AlInN) (10^{13} cm^{-2})	Total (10^{13} cm^{-2})
Al_2O_3/AlInN	—	−4.54	−4.54
AlInN/GaN	–1.81	4.54	2.73

simulated transfer characteristics is done with experimental transfer characteristics[13] for an AlInN/GaN MOS-HEMT. The model parameters are chosen to get perfect matching between experimental and simulation results. After achieving the matching, the model is applied for simulating our proposed underlap DG MOSFET, which also has a similar body material combination (AlInN/GaN).

Two-dimensional hydrodynamic numerical simulations are done using the Sentaurus TCAD device simulator G2012.06[20]. The hydrodynamic model (HD) accurately explains non-equilibrium conditions such as quasi-ballistic transport in the thin regions, and the velocity overshoot effect in the depleted regions. Additionally, the model accounts for several physical effects such as bandgap narrowing, variable effective mass, and doping dependent mobility at high electric fields. For high speed devices, the electron acquires high energy and the transport can be out of equilibrium; the electron velocities under these conditions can be much greater than its steady-state value. Drift diffusion models are not capable of describing the non-equilibrium electron transport in III–V heterostructures effectively. Accurate simulation results can be obtained by solving Boltzmann's transport equation using Monte Carlo simulation, but it consumes a lot of time and memory. Therefore, we use the hydrodynamic model to simulate and analyze device performance. The HD model solves the Poisson equation and continuity equations as follows:

$$\nabla \cdot \varepsilon \nabla \varphi = -q(p - n + N_D - N_A) - \rho_{trap}, \quad (1)$$

$$J_n = q\mu_n(n\nabla E_c + kT_n\nabla_n + kn\nabla T_n - 1.5nkT_n\nabla \ln m_n), \quad (2)$$

where ε is the electrical permittivity; φ is the electrostatic potential; q is the electronic charge; n and p are the electron and the hole densities; N_D is the ionized donor concentration; N_A is the ionized acceptors concentration; ρ_{trap} is the charge density contributed by traps and fixed charges; E_C is the conduction band edge energy; T_e is the electron temperature and m_e is the electron effective mass.

As mobility is not only doping and field dependent, in HD simulation the electron mobility model is expressed as[21]:

$$\mu_{n,\,dop} = \mu_{min} + \frac{\mu_d}{1 + (N_{dop}/N_0)^A}, \quad (3)$$

$$\mu_{n,\,field} = \frac{\mu_{n0} + \left(\frac{v_{sat}}{E_0}\right)\left(\frac{F}{E_0}\right)^4}{1 + (F/E_0)^4}, \quad (4)$$

$$\frac{1}{\mu_n} = \frac{1}{\mu_{n,\,dop}} + \frac{1}{\mu_{n,\,field}} - \frac{1}{\mu_{n0}}, \quad (5)$$

where μ_0 is the low field mobility, $\mu_{n,\,dop}$ is the mobility due to impurity scattering, and $\mu_{n,\,field}$ is the field dependent mobility at low doping, F is the driving force; N_{dop} is the doping concentration, μ_d, N_0, and A are temperature-dependent coefficients; v_{sat}, μ_{min}, and E_0 are cited from Refs. [22–24]. We have also applied bandgap narrowing across all regions in the simulation because if bandgap narrowing is not implemented there will be distortions in the energy band diagrams and electron transport across regions of potential barriers may be blocked. For recombination, the Shockley–Read–Hall (SRH) model is used with SRH, radiative and Auger recombination values of $\tau_{SRH} = 60$ ns, $C_{rad} = 1.4 \times 10^{-9}$ cm^3/s, and $C_{Auger} = 4 \times 10^{-29}$ cm^6/s[21]. For considering impact ionization, the van Overstraeten–de Man model is implemented.

Table 3. Values of v–E curve parameters for GaN and AlInN used in the simulations.

Parameter	GaN	AlInN
μ_{low} (cm^2/(V·s))	800	1581
v_{sat} (10^7 cm/s)	3.3	4.5
β	1	2

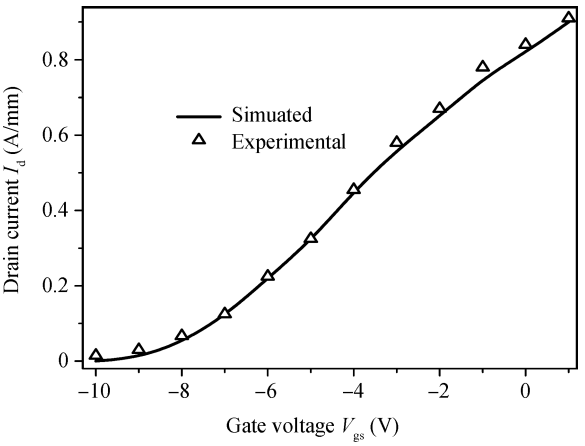

Fig. 3. Experimental (symbols) and simulated (solid lines) transfer characteristics for an AlInN/GaN buried channel MOSFET[13], showing very good agreement between the two results.

For considering spontaneous polarization in an AlInN/GaN heterostructure, the fixed charge (n_{SP}) shown in Table 2 was introduced at each interface. Table 3 summarizes the low field mobility and velocity parameters used in the simulation for GaN and AlInN. These parameters were chosen to match the v–E curve with the results of Ref. [25], as per Eq. (6). Donor type traps are introduced at the Al_2O_3/AlInN interface to evaluate the effects of the interface states[9], with the energy of the trap level defined as $E_{c,\,min}$ (AlInN) minus E_T. The $E_C - E_T = 0.9$ eV and a trap density N_T of 6×10^{12} cm^2 were used to match the simulated and experimental transfer characteristics, see Fig. 2. The effects of a non-uniform distribution of trapped electrons in a direction parallel to the interface are also considered in the simulation, as the current continuity equation and Poisson equation are solved self-consistently.

$$v(E) = \frac{\mu_{low}E}{\left[1 + \left(\frac{\mu_{low}E}{v_{sat}}\right)^{\beta}\right]^{\frac{1}{\beta}}}. \quad (6)$$

The simulated transfer characteristics of the device (Fig. 3)

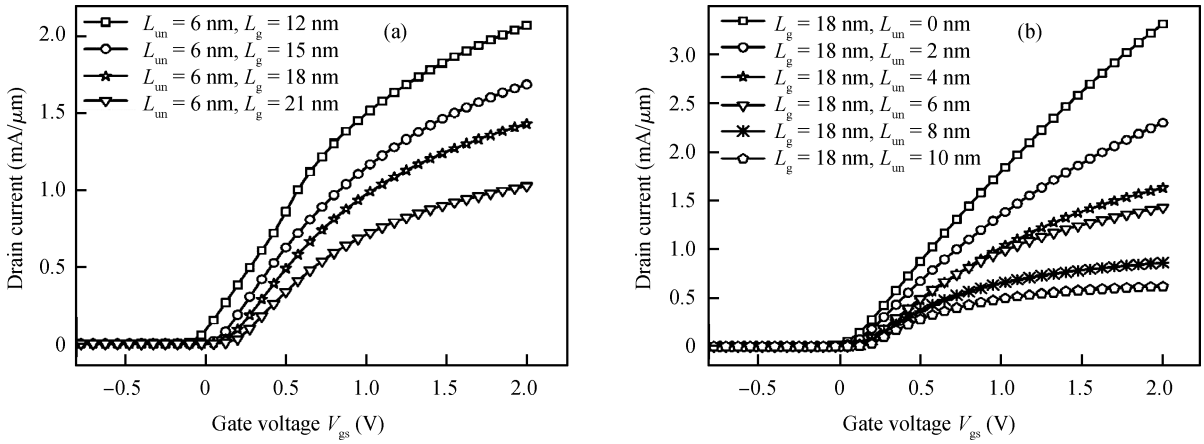

Fig. 4. I_D versus V_g characteristics for applied drain voltage is $V_d = 1$ V for both devices. (a) L_g varied from 12 to 21 nm with $L_{un} = 6$ nm. (b) L_{un} varied from 0 to 10 nm with constant $L_g = 18$ nm.

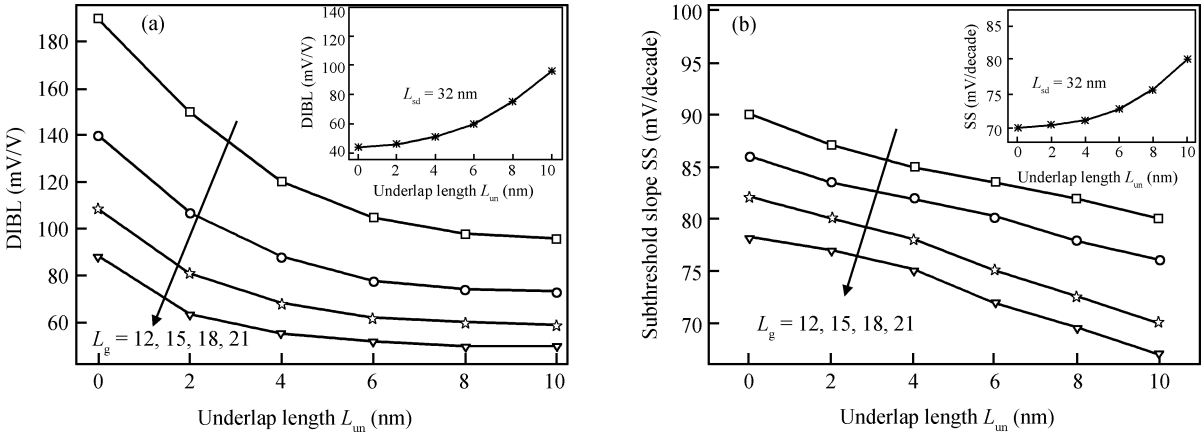

Fig. 5. (a) Variation of DIBL with L_{un}. L_g is varied from 12 to 21 nm in steps of 3 nm. L_{un} is varied from 0 to 10 nm in steps of 2 nm. (b) Dependence of SS on L_{un} for $L_g = 12$, 15, 18 and 21 nm. Insets show the DIBL and SS variation with L_{un} for constant $L_{sd} = 32$ nm.

shows very good agreement between the experimental results, thus validating our approximation of the carrier transport model and other model parameters. As the model is validated, extensive simulations of the underlap DG MOSFET device have been performed for changing gate and underlap lengths.

4. Results and discussion

The transfer characteristics of the AlInN/GaN MOS-HEMT device for variable gate length (Fig. 4(a)) and variable underlap length (Fig. 4(b)) depicts a very high drain current density ($\sim$3.6 mA/μm for $L_g = 18$, $L_{un} = 0$ nm), arising from the high mobility and velocity of 2DEG in the buried channel. Furthermore, there is a high current density (2DEG) by virtue of high spontaneous polarization. We observe good drain current saturation arising from a considerably lower EOT, with the double gate providing much better channel control[18]. For lower bias, the drain current (linear drive current) is proportional to the conductivity of the channel, and for higher bias the drain current (saturated drive current) is proportional to the carrier density and injection velocity. The carrier injection velocity in turn is a function of low-field carrier mobility and effective mass m_e[19].

An important parameter describing the electrostatic integrity of MOSFETs is DIBL, which can be expressed as the shift of threshold voltage caused by a change in the drain voltage (Eq. (7)). Figure 5(a) shows DIBL for varying L_{un} and L_g. As L_{un} increases from 0 nm (no underlap) to 10 nm (large underlap), the drain region moves away from the gate and the effect of drain potential on channel decreases. As the drain region moves apart, barrier lowering caused by the drain decreases, and thus DIBL decreases. DIBL dependence on L_{un} is more for shorter lengths (0 to 5 nm) and is less for longer length (5 to 10 nm). DIBL for $L_g = 18$ nm device decreases from 110 mV/V ($L_{ud} = 0$ nm) to 59 mV/V ($L_{ud} = 10$ nm). Similarly, as the gate length increases from 12 to 21 nm for a constant underlap of 6 nm, the DIBL drops from 105 to 52 mV/V. For symmetrical underlap devices, the effective gate length is the distance between the source and drain ends (L_{sd}), which can be given as $L_{sd} = L_g + 2L_{un}$. For the case of constant $L_{sd} = 32$ nm, as L_{un} increases from 0 to 10 nm, there is a decrease in L_g from 32 nm (for $L_{un} = 0$ nm) to 12 nm (for $L_{un} = 10$). Inset of Fig. 5(a) shows the variation of DIBL with L_{un} for constant $L_{sd} = 32$ nm and an increase in DIBL with L_{un}. The increase in DIBL is due to the mixed effect of a decrease in L_g and an increase in L_{un}, with decreasing L_g having a more pronounced

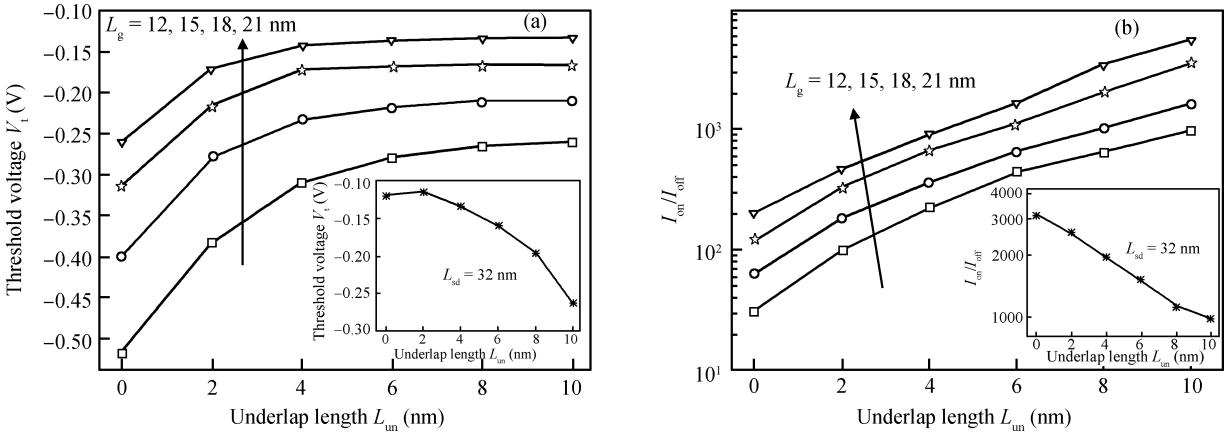

Fig. 6. (a) Variation of V_t with L_{un}. L_g is varied from 12 to 21 nm in steps of 3 nm. L_{un} is varied from 0 to 10 nm in steps of 2 nm. (b) Variation of I_{on}/I_{off} ratio on L_{un} for L_g = 12 nm, 15 nm, 18 nm and 21 nm. Insets shows the V_t and I_{on}/I_{off} ratio variation with L_{un} for constant L_{sd} = 32 nm.

effect than increasing L_{un}.

Figure 5(b) shows the variation in SS with L_g and L_{un}. The insertion of a barrier layer causes the channel to move away from the gate dielectric interface, reducing the electrostatic control and thus degrading the SS. Materials with higher mobility and high permittivity have generally shown higher short channel effects[26]. An SS is observed to decrease linearly with an increase in both L_{un} and L_g. The observed SS vales are higher than the ideal 60 mV/decade value. The inset of Fig. 5(b) shows an increasing SS with L_{un} for constant L_{sd} = 32 nm. An increase in SS is due to a decrease in L_g, leading to a higher short channel effect.

$$\mathrm{DIBL} = \frac{\Delta V_{th}}{\Delta V_{ds}} = \left[\frac{(V_{th1} - V_{th2})}{(V_{ds1} - V_{ds2})}\right], \tag{7}$$

where V_{th1} is threshold voltages extracted at a drain bias of V_{ds1} = 50 mV, and V_{th2} are the threshold voltages extracted at a drain bias of V_{ds2} = 1.0 V.

$$\mathrm{SS} = \frac{\Delta V_g}{\Delta (\log I_d)}. \tag{8}$$

Figure 6(a) shows the impact of underlap length on the device threshold voltage. The variation in L_{un} results in modulation of the device effective channel length ($L_{eff} = L_g + 2L_{un}$). Larger values of L_{un} result in a longer effective gate length, leading to increase in threshold voltage. Underlap is found to be very effective in increasing V_t for shorter underlap L_{ud} (up to 6 nm) and is ineffective for a longer underlap L_{ud} (6 to 10 nm), where V_t remains almost constant. V_t increases from –0.314 to –0.167 V for L_{ud} variation from 0 to 10 nm for an 18 nm gate length device. Another common figure of merit for a CMOS is the I_{on}/I_{off} ratio. This ratio has a significant impact on the static power consumption in low standby power applications and higher values of I_{on}/I_{off} ratio are desirable. Figure 6(b) shows I_{on}/I_{off} ratio variation with L_{un} for multiple gate length devices. The I_{on}/I_{off} ratio for this device is not very impressive due to higher I_{off}, which in turn is attributed to a higher leakage current. The maximum attainable I_{on}/I_{off} ratio value is 5.4 × 10^3 for L_g = 21 nm and L_{un} = 10 nm. In case of constant L_{sd} = 32 nm (insets of Figs. 6(a) and 6(b)), the V_t and the I_{on}/I_{off} ratio are observed to decrease with underlap. This is due to a decrease in L_g from 32 nm (for L_{un} = 0 nm) to 12 nm (for L_{un} = 10 nm).

For CMOS, the most important figure of merit is intrinsic device delay (τ) because it determines the device switching speed. Intrinsic delay is given by $\tau = CV/I$, where C is the total gate capacitance per micron transistor width, V is the power-supply voltage (V_{dd}), and I is the saturation drive current per micron transistor width (I_{dsat}). Drain current (I_{dsat}) in AlInN/GaN and other MOS HEMT devices depends on the mobility and injection velocities of carriers, which are high in case of III–V materials. Due to higher I_{dsat}, the intrinsic delay will be very low and fast device switching can be achieved. The distance between channel and gate metal is more in MOS HEMT because the channel is buried away at the interface of the AlInN/GaN layer. MOS-HEMT devices will therefore have much lower gate capacitance, leading to a further reduction of delay. As underlap length increases, the gate capacitance decreases[27], which results in a reduction of device delay. The variation in delay is almost linear with respect to L_{un} (Fig. 7(a)). Extremely low device delay (∼0.003 ps) can be achieved with a L_g = 21 nm device at L_{un} = 10 nm. Figure 7(b) shows the variation of energy delay product as a function of L_{un}. The AlInN/GaN MOS HEMT shows a considerably lower energy delay product value (∼2.53 × 10^{-31} Js/μm). A lower energy delay product is highly desirable for low power and high-performance logic applications. Reduction in energy delay product ceases beyond 6 nm underlap, and is almost constant from 6 to 10 nm underlap. In the case of constant L_{sd} = 32 nm (insets of Figs. 7(a) and 7(b)), the delay and the energy delay product are observed to increase with L_{un}, due to a decrease in L_g.

5. Conclusion

A performance investigation of AlInN/GaN heterostructure underlap DG MOSFETs is done for major device metrics like DIBL, SS, I_{on}/I_{off}, V_t, delay, and energy delay product, for a wide range of underlap and gate lengths. Lattice matched $Al_{0.83}In_{0.17}N$ and GaN have much larger conduction band discontinuity and also stronger spontaneous polarization

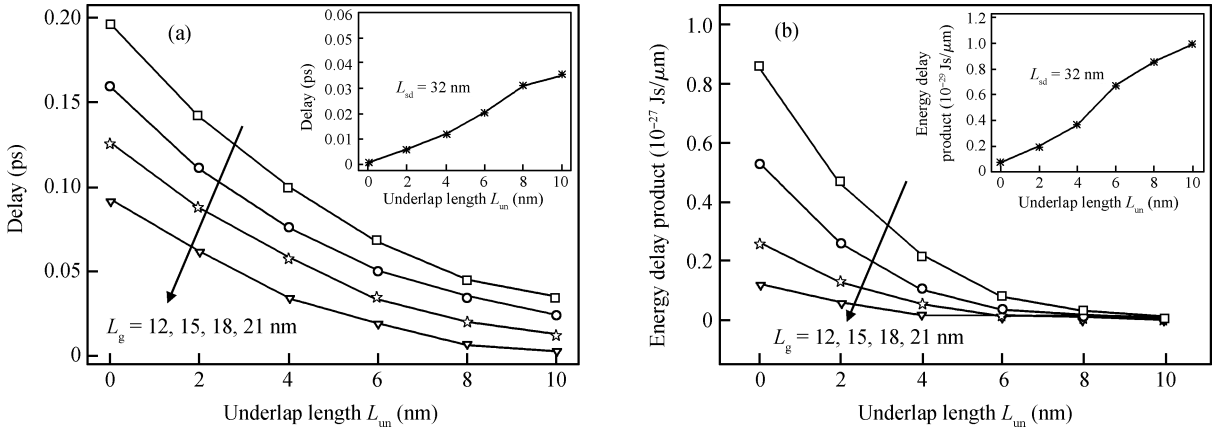

Fig. 7. (a) Variation of intrinsic device delay with underlap length L_{un}. L_g is varied from 12 to 21 nm in steps of 3 nm. L_{un} is varied from 0 to 10 nm in steps of 2 nm. Delay $= C_{gg}V_d/I_d$ measured at $V_d = 1$ V. (b) Energy delay product versus L_{un} for $L_g = 12$, 15, 18 and 21 nm. Energy delay product $= (C_{gg}V_d/I_d)(C_{gg}V_d^2)$ measured at $V_d = 1$ V. Insets shows the delay and energy delay product variation with L_{un} for constant $L_{sd} = 32$ nm.

effects, giving higher 2DEG charge density. The AlInN/GaN heterostructure interface provides high carrier velocity and mobility. An impressive drain current density of $\sim$3.6 mA/μm is obtained for the device with a gate length of 18 nm and underlap length 0 nm. DIBL dependence on L_{un} is more up to 5 nm and becomes less for a longer underlap. The SS performance is degraded because the buried channel is away from the gate dielectric interface. Furthermore, underlap is found to be very effective in increasing V_t for shorter underlap (up to 6 nm). Despite the higher I_{on}, the I_{on}/I_{off} ratio is low due to higher I_{off} (due to high leakage). Extremely low intrinsic delay ($\sim$0.003 ps) and energy delay product ($\sim 2.53 \times 10^{-31}$ Js/μm) are achieved, due to higher mobility and velocity of the carrier in the buried channel. The results show that there is a need to optimize the I_{off} and SS values for specific logic design. The AlInN/GaN heterostructure underlap DG MOSFET shows excellent promise as one of the candidates to substitute present MOSFETs for future high-speed applications.

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