A micro-power LDO with piecewise voltage foldback current limit protection*

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Abstract: To achieve a constant current limit, low power consumption and high driving capability, a micro-power LDO with a piecewise voltage-foldback current-limit circuit is presented. The current-limit threshold is dynamically adjusted to achieve a maximum driving capability and lower quiescent current of only 300 nA. To increase the loop stability of the proposed LDO, a high impedance transconductance buffer under a micro quiescent current is designed for splitting the pole that exists at the gate of the pass transistor to the dominant pole, and a zero is designed for the purpose of the second pole phase compensation. The proposed LDO is fabricated in a BiCMOS process. The measurement results show that the short-circuit current of the LDO is 190 mA, the constant limit current under a high drop-out voltage is 440 mA, and the maximum load current under a low drop-out voltage is up to 800 mA. In addition, the quiescent current of the LDO is only 7 μA, the load regulation is about 0.56% on full scale, the line regulation is about 0.012%/V, the PSRR at 120 Hz is 58 dB and the drop-out voltage is only 70 mV when the load current is 250 mA.

Key words: power protection; voltage foldback; current limit; micro-power; LDO
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1. Introduction

Switching noise propagation and signal crosstalk among digital and RF systems may take place via the power lines, owing to the low-noise and ripple-free characteristics, and the low-dropout regulator (LDO) is utilized widely. For these applications, LDOs should have a constant current-limit protection function and high loop stability with a wide output current range. Moreover, high efficient power management circuits are becoming more and more important to the battery in portable devices. Therefore, techniques to improve the micro quiescent current LDO[1, 2] are being investigated more and more.

Current limit circuits are extensively used in LDO circuits, which prevent the device failure when load currents exceed the safe region. The classical current limit circuit[3] limits the load current by using a current mirror. Recently reported foldback current limit circuits[4, 5] constrain the load current using two current mirrors, which are used for constant current limiting and short circuit current limiting, respectively. However, these current limit circuits are not appropriate for low-power LDOs because of complex topology or a more quiescent current. To deal with this problem, a piecewise voltage foldback current limit circuit with an ultra-low quiescent current is presented in this paper, which limits the output current to a specific level under a different output voltage, namely, a short circuit, high drop-out and low drop-out voltage.

Another problem with the wide current-range is loop stability[6, 7]. The wide current range makes the dominant pole of the LDO change dramatically. The requirement of increasing the load current and a lower drop-out voltage result in enlarging the pass transistor and considerate parasitic capacitance, which pushes the pole present at the gate of the pass transistor toward lower frequencies. So the loop stability is a challenge in LDO design. Unfortunately, the specified micro quiescent current increases the output impedance of the buffer and further lowers the pole, which deteriorates the LDO stability[8, 9]. To deal with this issue, there are three main methods: (1) output capacitor equivalent series resistance (ESR) zero frequency compensation[5], which will increase the output overshoot and reduce the input noise suppression. In addition, the selection of the output capacitor is notorious. (2) The Miller capacitance technique[10], which will reduce the loop bandwidth. (3) The internal zero canceling pole technique[11], which makes matching difficult, but the LDO will have the advantages of low output noise and high response speed. In the proposed LDO, a zero to compensate the second pole phase lag and a buffer with a high transconductance bipolar device to achieve impedance transformation under a micro quiescent current are designed to stabilize the closed loop.

2. The traditional foldback limit circuit

Figure 1 shows the traditional foldback current limit protection circuit[5] and MP is the pass transistor. This circuit limits the load current using two current mirrors, which are used for constant current limiting and short-circuit current limiting, respectively.

If V_{OUT} is low (short-circuit current), M8 will mirror I_{OUT} proportionally. When I_{OUT} increases so that the voltage drop on R_3 exceeding $|V_{TP}|$ (V_{TP} is the PMOS threshold), M1 will turn on. Then I_{OUT} will be limited on a predefined current by V_{TP} and R_3. In the same way, if V_{OUT} is high (constant current limit), M3 will mirror I_{OUT} proportionally. When I_{OUT} increases so that the voltage drop on R_1 exceeds V_{REF}, M2 will turn on. Thus I_{OUT} will be limited on another predefined current by V_{REF} and R_1.

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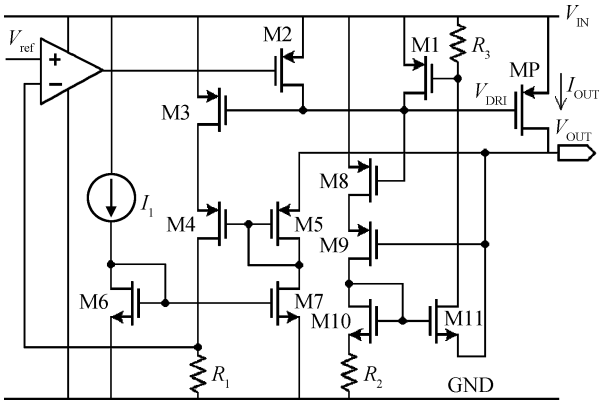

Fig. 1. The traditional foldback current limit circuit.

The purpose of current limiting is to prevent the LDO from overheating damage caused by exceeding the power consumption. For a general LDO, the quiescent current is very small and the main power consumption comes from the pass transistor.

$$P_{\mathrm{D}} = (V_{\mathrm{IN}} - V_{\mathrm{OUT}})I_{\mathrm{OUT}}. \quad (1)$$

For the specific power, the load current will increase as the drop-out voltage decreases. To maximize the driving capability under a specific power, the load current is commonly piecewisely limited according to the drop-out voltage. The traditional circuit in Fig. 1 has constant and short circuit current limiting. However, the constant current limiting restricts the maximum current under a low dropout voltage due to not differentiating the high drop-out voltage from the low drop-out voltage. Moreover, M3, M5, M6, M8 and the auxiliary amplifier all require a bias current, so the circuit will consume much quiescent current. Unfortunately, the quiescent current will increase with the output current I_{OUT} since the branch currents through M3 and M8 increase.

In addition, the circuit contains an auxiliary amplifier and the topology is complex.

3. The proposed piecewise voltage foldback current limit circuit

The proposed current limit circuit is shown in Fig. 2 and MP is the pass transistor. The current limiting is divided into three steps according to V_{OUT}. Those are the short-circuit current limit when $V_{\mathrm{OUT}} \leqslant V_{\mathrm{TN}}$ (V_{TN} is the NMOS threshold), the constant limit current when $V_{\mathrm{TN}} \leqslant V_{\mathrm{OUT}} \leqslant V_{\mathrm{IN}} - |V_{\mathrm{TP}}|$ and the maximum load current when $V_{\mathrm{IN}} - |V_{\mathrm{TP}}| \leqslant V_{\mathrm{OUT}} \leqslant V_{\mathrm{IN}}$, respectively.

When $V_{\mathrm{OUT}} \leqslant V_{\mathrm{TN}}$, M2 is in the linear region, M1 is the cutoff, which pushes M4 into the linear region. Thus, M3 and M5 are in parallel and the operating point is determined by M3 since the W/L of M5 is much smaller than the W/L of M3. As a result, $V_{\mathrm{A}} = V_{\mathrm{IN}} - V_{\mathrm{GS\text{-}M3}} - V_{\mathrm{GS\text{-}M6}}$. After two stage buffers of Q1 and Q2, $V_{\mathrm{B}} \geqslant V_{\mathrm{IN}} - V_{\mathrm{GS\text{-}M3}} - V_{\mathrm{GS\text{-}M6}} + V_{\mathrm{EB\text{-}Q1}} - V_{\mathrm{BE\text{-}Q2}}$. Assuming that PNP and NPN have the same V_{BE}, V_{B} can be simplified to $V_{\mathrm{B}} \geqslant V_{\mathrm{IN}} - V_{\mathrm{GS\text{-}M3}} - V_{\mathrm{GS\text{-}M6}}$. The voltage is passed through the buffer to the gate of the MP. Due to V_{OUT} being low, the pass transistor is in the saturated region. Thus, the maximum load current can be derived.

$$I_{\mathrm{O-S}} = K_{\mathrm{P}}\left(\frac{W}{L}\right)_{\mathrm{MP}}(V_{\mathrm{GS\text{-}M3}} + V_{\mathrm{GS\text{-}M6}} - |V_{\mathrm{TP}}|)^2, \quad (2)$$

where K_{P} is the transconductance coefficient of PMOS.

When $V_{\mathrm{TN}} \leqslant V_{\mathrm{OUT}} \leqslant V_{\mathrm{IN}} - |V_{\mathrm{TP}}|$, both M1 and M2 are in the linear region and M4 is the cutoff. Thus, $V_{\mathrm{A}} = V_{\mathrm{IN}} - V_{\mathrm{GS\text{-}M5}} - V_{\mathrm{GS\text{-}M6}}$. Similarly, $V_{\mathrm{GS\text{-}MP}}$ is no less than $V_{\mathrm{IN}} - V_{\mathrm{GS\text{-}M5}} - V_{\mathrm{GS\text{-}M6}}$. Due to the pass transistor being in the saturated region, the maximum load current can be derived as

$$I_{\mathrm{O-H}} = K_{\mathrm{P}}\left(\frac{W}{L}\right)_{\mathrm{MP}}(V_{\mathrm{GS\text{-}M5}} + V_{\mathrm{GS\text{-}M6}} - |V_{\mathrm{TP}}|)^2. \quad (3)$$

$I_{\mathrm{O-S}}$ is less than $I_{\mathrm{O-H}}$ since W/L of M5 is smaller than W/L of M3.

When $V_{\mathrm{IN}} - |V_{\mathrm{TP}}| \leqslant V_{\mathrm{OUT}} \leqslant V_{\mathrm{IN}}$, M2 is the cutoff and $V_{\mathrm{A}} \approx 0$ V. In this case, V_{B} is only determined by the input stage and is not affected by the current limit circuit. Thus, MP is in the linear region and V_{GS} is about equal to V_{IN} .

$$I_{\mathrm{O-L}} = K_{\mathrm{P}}\left(\frac{W}{L}\right)_{\mathrm{MP}}(V_{\mathrm{IN}} - |V_{\mathrm{TP}}|)V_{\mathrm{DS\text{-}MP}}. \quad (4)$$

The maximum load current under a low drop-out voltage is determined by V_{IN}, V_{TP} and $V_{\mathrm{DS\text{-}MP}}$.

For the specific power, the maximum load current under a high drop-out voltage should be smaller than that under a low drop-out voltage. However, the constant current limiting of the previous circuit restricts the maximum load current under a low drop-out voltage. Fortunately, the proposed circuit overcomes the issue by distinguishing the low drop-out voltage from the high drop-out voltage. It not only achieves a current limit for the high drop-out voltage but also maximizes the load current under the low drop-out voltage. The previous circuit requires much quiescent current to stabilize the operation point. The proposed circuit is a digital circuit which requires little current, the quiescent current is as low as 0.3 μA.

4. Loop stability improvement

The proposed LDO loop is composed of the input stage (OTA), the buffer and the output stage. The input stage has a high gain. The buffer is used to separate the OTA with a high output impedance from the gate of the MP with a large parasitic capacitance. Therefore, the response speed and stability of the loop is improved.

The OTA is composed of M7–M10 and R_5. There is a pole at the output (the node B) of the OTA.

$$A_1 = r_{\mathrm{O1}}/R_5, \quad (5)$$

$$P_2 = \frac{1}{2\pi r_{\mathrm{O1}}(C_{\mathrm{GD\text{-}M8}} + C_{\mathrm{GD\text{-}M10}} + C_1)}, \quad (6)$$

where A_1 is the gain of the input stage, r_{O1} is the output impedance of the OTA and the input impedance of the buffer stage in parallel.

The buffer is composed of Q3–Q6. Due to the base current compensation between Q3 and Q4, the buffer has a high input impedance matching the high output impedance of the

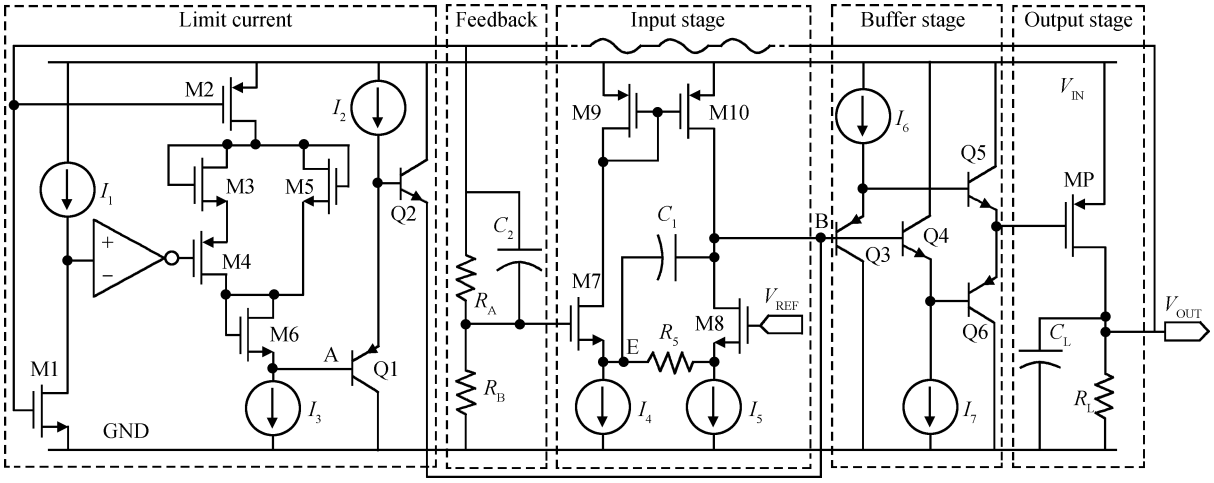

Fig. 2. The proposed LDO with a piecewis voltage foldback current limit.

OTA. The source follower push–pull output of the buffer, comprised by Q5 and Q6, not only reduces the output impedance but achieves no crossover distortion and bilaterally symmetrical driving MP, which is prone to improve the loop response speed. The bipolar transconductance is higher than the MOS transconductance under the same bias current. Therefore, the bipolar buffer achieves a higher impedance transformation under the micro quiescent current. In addition, selecting the V_{BE} of an NPN smaller than the $|V_{TP}|$ of the MP, the minimum load current can be less than μA order of magnitude. Thus, a common issue that the minimum load current is too large is settled. The buffer gain of A2 is at about the unity gain because of the source follower.

The output stage of the LDO is composed of the MP, C_L and R_L. The MP and R_L determine the gain, R_L and C_L determine the dominant pole.

$$A_3 = g_{m_{MP}} \frac{R_L r_{O3}}{R_L + r_{O3}}, \tag{7}$$

$$P_1 = \frac{1}{2\pi \dfrac{R_L r_{O3}}{R_L + r_{O3}} C_L} \approx \frac{1}{2\pi R_L C_L}$$

$$= \frac{I_{OUT}}{2\pi V_{OUT} C_L}, \tag{8}$$

where r_{O3} is the dynamic impedance of the MP.

In order to achieve a low drop-out voltage, the W/L of the MP is quite large ($W/L = 160000$), and $C_{GS\text{-}MP}$ and $C_{GD\text{-}MP}$ are also quite large. Therefore, there is another low frequency pole at the MPgate.

$$P_3 = \frac{1}{2\pi r_{O2}(C_{GS\text{-}MP} + A_3 C_{GD\text{-}MP})}, \tag{9}$$

where r_{O2} is the output impedance of the buffer.

In order to ensure the stability of the LDO, Z_1 for phase compensation is introduced by C_1 at node E.

$$Z_1 = \frac{1}{2\pi R_5 A_1 C_1}. \tag{10}$$

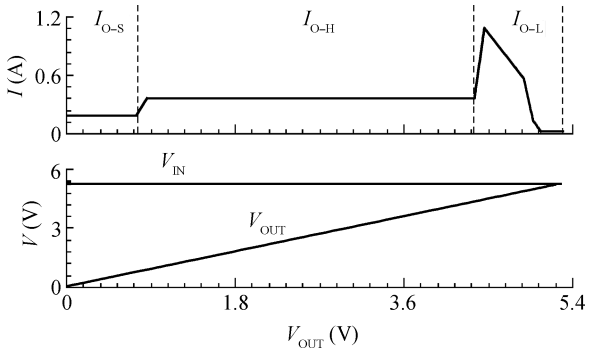

Fig. 3. Simulated results of current limiting.

An appropriate C_1 allows Z_1 to be located between P_2 and P_3, so the phase lag caused by P_2 will be compensated.

The zero Z_2, is beyond the unity-gain bandwidth introduced by C_2 in the feedback network, which can improve the transient response speed.

$$Z_2 = \frac{1}{2\pi \dfrac{R_A R_B}{R_A + R_B} C_2}. \tag{11}$$

5. Experimental results and discussion

The proposed LDO is verified by the Bsim3V3 model of the BiCMOS process, the I_{OUT} simulation versus V_{OUT} under the condition $V_{IN} = 5.2$ V is shown in Fig. 3. When $V_{OUT} \leqslant 0.84$ V, the LDO is in short-circuit mode and I_{O-S} is about 190 mA. When $0.84\text{ V} \leqslant V_{OUT} \leqslant 4.4$ V, the LDO is in constant current limit mode and I_{O-H} is about 430 mA. When $4.4\text{ V} \leqslant V_{OUT} \leqslant V_{IN}$, the LDO is in low drop-out voltage state and I_{OUT} steps up to 0.9 A at first, which is because MP is in the linear region, and R_{ON} is very small as V_{GS-MP} is close to V_{IN}. Hereafter, I_{OUT} decreases as the drop-out voltage declines.

Simulation of loop frequency characteristics are shown in Fig. 4. Under a heavy load current, the DC gain is about 60 dB, the –3 dB and unity-gain bandwidth are 170 Hz and 33 kHz, respectively, and the phase margin is about 50°. The amplitude–frequency and phase–frequency characteristic curves un-

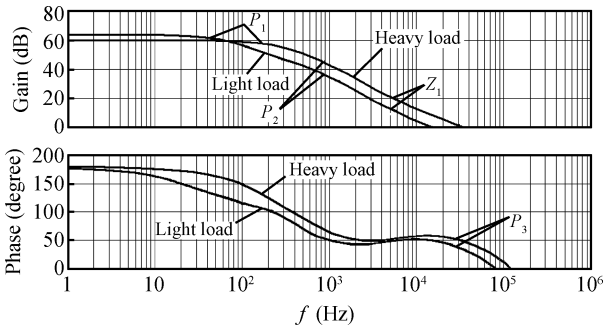

Fig. 4. Simulated results of the loop stability.

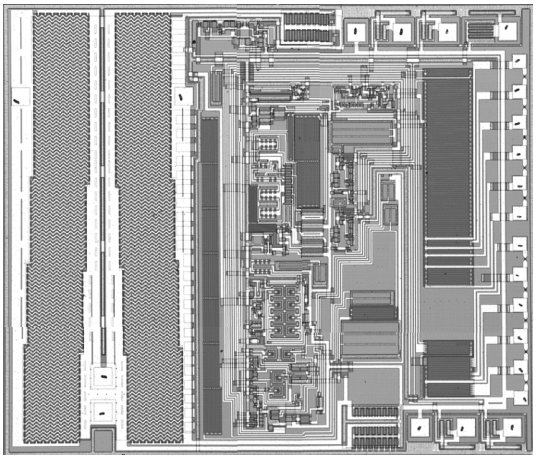

Fig. 5. Micrograph of the proposed LDO.

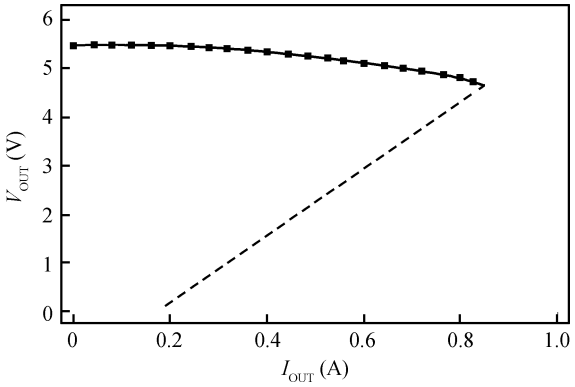

Fig. 6. Measured results of I_{OUT} versus V_{OUT}.

der a light load current both shift left slightly to those under a heavy load current, because the P_1 frequency is lower. In addition, the loop DC gain under a light load current is slightly higher than that under a heavy load current, which is because there is a slight increase in A_3.

Micrograph of the proposed LDO is shown in Fig. 5, the chip size is only 1.5×1.9 mm^2.

The measured result of I_{OUT} versus V_{OUT} under the condition $V_{IN} = 5.5$ V is shown in Fig. 6. When I_{OUT} is small, V_{OUT} is almost unchanged. When I_{OUT} exceeds 200 mA, V_{OUT} decreases with I_{OUT} increasing. When I_{OUT} is added to about 840 mA, V_{OUT} suddenly drops from 4.6 V or so to about 0 V, while I_{OUT} also declines to about 170 mA, which is because the

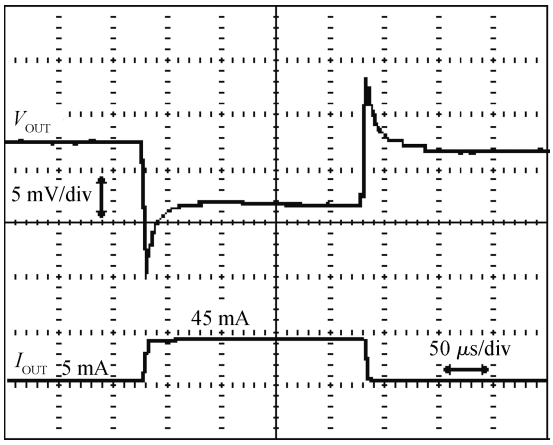

Fig. 7. Measured results of the load transient response.

Table 1. Comparison of the proposed LDO performances.

Parameter	Ref. [12]	Ref. [10]	Ref. [13]	Ref. [14]	This work
V_{IN} (V)	1.2	2.2–5.5	0.95–14	2.5–4	2.7–9
V_{OUT} (V)	1	1.6	0.7–1.2	N/A	1.2–8.5
Drop-out voltage (V)	0.2	0.2	0.2	0.15	0.07
I_{Load} (max) (mA)	100	200	100	100	250
$I_Q(\mu A)$ @ no load	100	23	43	8	7
$I_Q(\mu A)$ @ full load	100	180	N/A	N/A	7.7

LDO comes into the current limit mode induced by the drop-out voltage being lower than $|V_{TP}|$. The reason for I_{OUT} declining to 170 mA is that the LDO enters into the short circuit mode at that time.

The measured load transient response is shown in Fig. 7. When I_{OUT} steps from 5 to 45 mA, there is a 7 mV undershoot and V_{OUT} drops by about 5 mV after the LDO was stabilized, when I_{OUT} steps from 45 to 5 mA. Similarly, there is a 7 mV overshoot and V_{OUT} rises by about 5 mV after the LDO was stabilized. In addition, the settling time of the LDO is about 50 μs.

According to the test results, the total V_{OUT} variation is 28 mV within the I_{OUT} range from 0 to 250 mA when V_{OUT} is set to 5 V, the load regulation is about 0.56% on full scale. The V_{OUT} variation is 2 mV within the V_{IN} range from 5.5 to 9 V when V_{OUT} is set to 5 V and $I_{OUT} = 100$ mA, and the line regulation is about 0.012%/V. The drop-out voltage is only 70 mV when $I_{OUT} = 250$ mA. The PSRR at 120 Hz is 58 dB. In addition, the quiescent current of the LDO is only 7 μA under no load. Despite being on full load the quiescent current is only 7.7 μA.

Table 1 shows a performance comparison of some previously reported LDO with the proposed LDO. It is noticeable that the proposed LDO has the lowest quiescent current and the largest input range within the same driving capacity.

6. Conclusions

A micro-power LDO with a piecewise voltage foldback current limit circuit is presented in this paper, the current limit corresponds to a short circuit, high drop-out voltage and low drop-out voltage, respectively, and the limit current is increasing step by step. Thus, power protection and the maximum driving capability are achieved. For low power and loop stability, the buffer designed with a high transconductance bipolar device achieves the separation of the pole at the gate of the pass transistor from the dominant pole, and Z_1 is designed to compensate the second pole phase lag. The measurement results show that the short circuit current of the LDO is 190 mA, the constant limit current is 440 mA and the maximum load current under a low drop-out voltage is up to 800 mA. The total $V_{\rm OUT}$ variation is 28 mV within an $I_{\rm OUT}$ range from 0 to 250 mA and the load regulation is about 0.56% on a full scale. The $V_{\rm OUT}$ variation is 2 mV within the $V_{\rm IN}$ range from 5.5 to 9 V when $V_{\rm OUT}$ is set to 5 V and $I_{\rm OUT} = 100$ mA, the power regulation is about 0.012%/V. The drop-out voltage is only 70 mV when $I_{\rm OUT} = 250$ mA. The PSRR at 120 Hz is 58 dB. In addition, the quiescent current of the LDO is only 7 μA.

Experimental results show that the proposed LDO achieves a piecewise foldback current limit, fast transient response, excellent line and load regulations, as well as an ultra low quiescent current. The proposed LDO is suitable for a low voltage, micro-power consumption, battery powered system and SoC applications.

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