A pixel circuit with reduced switching leakage for an organic light-emitting diode

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Abstract: This paper presents a pixel circuit with reduced switching leakage for OLED microdisplays. A self-referenced feedback loop is designed to track the node voltages for leakage reduction during the holding period. A longer holding time using a smaller storage capacitor can be achieved using the leakage reduction technique. An experimental system based on a 60 × 80 pixel matrix is fabricated in a 0.35-μm CMOS process. The area of the pixel circuit is only 15 × 15 μm^2. According to the measured results, the pixel circuit achieves a holding time of longer than 500 ms and the system exhibits a satisfied accuracy and linearity within a pixel current range from 100 pA to 3 nA.

Key words: pixel; OLED; leakage; CMOS
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1. Introduction

Since the first observation of light emission in 1987, organic light-emitting diodes (OLEDs) have been proved to be a suitable light source for next generation displays. Compared with other competing technologies, an OLED has the advantages of smaller dimensions, lower power consumption, a wider viewing angle, shorter response time, excellent contrast ratio, larger dynamic range, etc. Combined with commercially available MOS technology, an OLED can be implemented with a complex process circuit on a silicon substrate through hybrid integration. Such an OLED-on-silicon can provide a higher optical performance at a lower power consumption, which is particularly adept for micro-displays[1].

With the rapid increase of pixel scale, the pixel area is required to be less than 100 μm^2 with a pixel current range from hundreds of pA (10^{-10}) to tens of nA (10^{-8})[2]. With the limitation of driving current, the voltage driving mechanism is more appropriate for the pixel circuit than traditional current driving. The driving voltage should be stored on a capacitor during the holding time, which is approximately 20 ms at a frame rate of 50 Hz. Unfortunately, the leakage of the MOS transistor will cause an undesired variation of the voltage, resulting in influences on the resolution and uniformity of OLED displays. Furthermore, the area of the capacitor is restricted by the pixel pitch, which makes the problem more serious. Some research results have been reported on a thin-film transistor (TFT) pixel driving circuit for active matrix organic light emitting diode (AMOLED) displays[3, 4]. But these approaches are still not enough for OLED micro-displays driven by MOS transistors because of a smaller pixel pitch and lower driving current.

This paper presents the leakage mechanisms in deep-submicrometer MOS technology and its influence on pixel circuit for OLED micro-displays. Then, the leakage reduction technique is discussed and a novel circuit structure is proposed to suppress the leakage. Finally, an experimental chip is implemented and the measured results are presented.

2. Leakages of the pixel circuit

In a traditional pixel circuit as shown in Fig. 1, the data voltage is sampled through switching transistor T1 when the address scanning voltage V_{scan} is low. After a short sampling period, V_{scan} changes to be high and the data voltage is stored in capacitor C_S. The value of this stored voltage determines the level of the output current I_{OUT}. During the holding period, the voltage stored in C_S will rise due to the leakage of the switching transistor T1, as shown in Fig. 2. Such variation will lead to serious problems for the resolution and uniformity of OLED displays.

The considerable leakages of the pixel circuit include a PN junction reverse-bias current and off-state channel current, marked as I_1 and I_2 in Fig. 1, respectively. I_1 comes from the reverse-biased diode D_{sub} between the drain and substrate N-well. The current density can be given by[5]

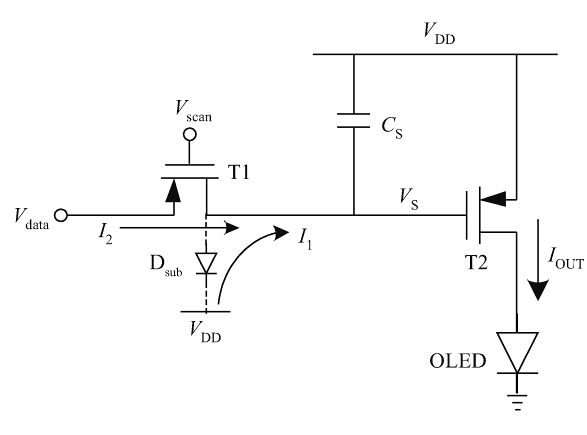

Fig. 1. Traditional pixel circuit.

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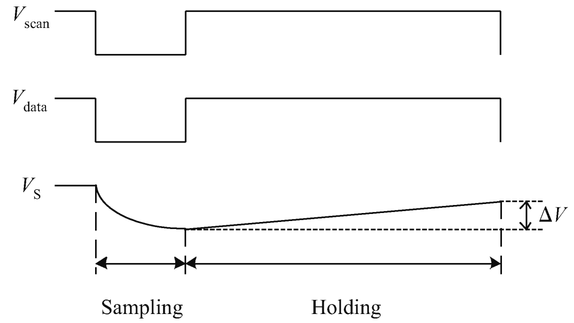

Fig. 2. Waveforms of the pixel circuit in Fig. 1.

$$J_{\mathrm{b-b}} = A\frac{EV_{\mathrm{app}}}{E_{\mathrm{g}}^{1/2}}\exp\left(-B\frac{E_{\mathrm{g}}^{3/2}}{E}\right),$$

$$A = \frac{\sqrt{2m}q^3}{4\pi^3h^2}, \quad B = \frac{4\sqrt{2m}}{3qh}, \quad (1)$$

where m is effective mass of the electron; E_{g} is the energy-band gap; V_{app} is the applied reverse bias; E is the electric field at the junction; q is the electronic charge; and h is $1/(2\pi)$ times Planck's constant. The electric field of a step junction is given by

$$E = \sqrt{\frac{2qN_{\mathrm{a}}N_{\mathrm{d}}(V_{\mathrm{app}} + V_{\mathrm{bi}})}{\varepsilon_{\mathrm{si}}(N_{\mathrm{a}} + N_{\mathrm{d}})}}, \quad (2)$$

where N_{a} and N_{d} are the doping in the p and n side, respectively; $\varepsilon_{\mathrm{si}}$ is the permittivity of silicon; and V_{bi} is the built-in voltage across the junction.

So, the PN junction reverse-bias current I_1 increases with the rise of the reverse bias V_{app}, as illustrated in Eqs. (1) and (2). On the other hand, I_1 can be reduced to zero on the condition that V_{app} is zero. This conclusion is one of the theoretical foundations for leakage reduction approaches.

A MOS transistor works in a weak inversion condition if the gate–source voltage is below threshold voltage V_{th}. The sub-threshold current between the source and drain, I_2 in Fig. 1, is given by[5]

$$I_{\mathrm{ds}} = \mu_0 C_{\mathrm{ox}}\frac{W}{L}(m-1)(V_{\mathrm{T}})^2\mathrm{e}^{(v_{\mathrm{GS}}-V_{\mathrm{th}})/(mV_{\mathrm{T}})}(1-\mathrm{e}^{-v_{\mathrm{DS}}/V_{\mathrm{T}}}), \quad (3)$$

where

$$m = 1 + \frac{C_{\mathrm{dm}}}{C_{\mathrm{ox}}} = 1 + \frac{\varepsilon_{\mathrm{si}}}{W_{\mathrm{dm}}}\Big/\frac{\varepsilon_{\mathrm{ox}}}{t_{\mathrm{ox}}} = 1 + \frac{3t_{\mathrm{ox}}}{W_{\mathrm{dm}}}, \quad (4)$$

where V_{th} is the threshold voltage, and V_{T} is the thermal voltage; C_{ox} is the gate oxide capacitance; μ_0 is the zero bias mobility; m is the body effect coefficient. W_{dm} is the maximum depletion layer width, and t_{ox} is the gate oxide thickness. C_{dm} is the capacitance of the depletion layer. The expression in Eq. (3) is similar to that of the BSIM MOS transistor model, which is expressed as[6]

$$I_{\mathrm{ds}} = \mu_0 C_{\mathrm{ox}}\frac{W}{L}\mathrm{e}^{1.8}(V_{\mathrm{T}})^2\mathrm{e}^{(v_{\mathrm{GS}}-V_{\mathrm{th}})/(mV_{\mathrm{T}})}(1-\mathrm{e}^{-v_{\mathrm{DS}}/V_{\mathrm{T}}}). \quad (5)$$

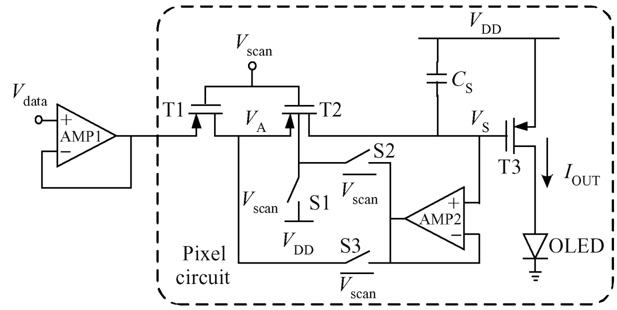

Fig. 3. A simplified schematic of the improved pixel circuit.

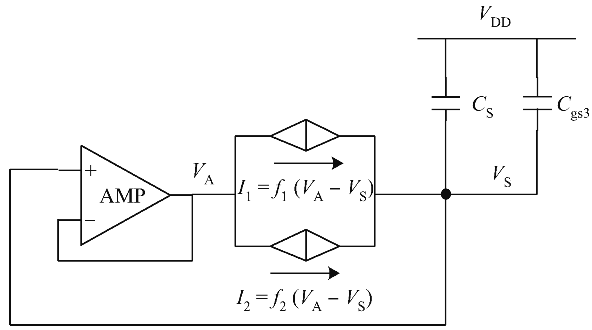

Fig. 4. Equivalent circuit of a pixel circuit during the holding period.

Both Equations (3) and (5) indicate that the off-state current ($v_{\mathrm{GS}} = 0$) is zero as long as the voltage v_{DS} can be guaranteed to be zero. This is the other theoretical foundation for leakage reduction.

3. Circuit design

According to the analysis above, the voltage v_{DS} and the PN junction reverse bias V_{app} of the switching transistor T1 in Fig. 1 should be controlled and adjusted to be zero. Thus, the voltages of input terminal and the substrate of transistor T1 have to follow V_{S} dynamically. In order to implement such a controlling, an improved pixel circuit with switching leakage reduction is proposed in Fig. 3. An amplifier with low power consumption is introduced to achieve the required voltage. Three switches, S1–S3, are designed to be on and off alternately to make it possible to control the voltages of v_{DS} and V_{app}. An additional switching transistor T1 in Fig. 3 is adopted to isolate the input terminal and the source of T2. During the sampling period, V_{scan} is low, S1 is on while S2 and S3 are off. The input data drives the storage capacitor C_{S} through the amplifier to make voltage V_{S} equal to V_{data}. During the holding period, V_{scan} is high, S1 is off while S2 and S3 are on. The output of the amplifier is connected with both the source and the substrate of T2 to establish a feedback loop without any input. Such a self-referenced loop makes it possible for both V_{A} and the substrate voltage of T2 to track V_{S} automatically, guaranteeing v_{DS} and V_{app} of T2 to be approximately zero. So the leakage of T2 is reduced and the stored voltage V_{S} maintains fixed resulting in constant I_{OUT}.

The equivalent circuit of the pixel circuit during the holding period is presented in Fig. 4, which is simplified to a closed loop. Two kinds of leakages of the off-state transistor T_2 are

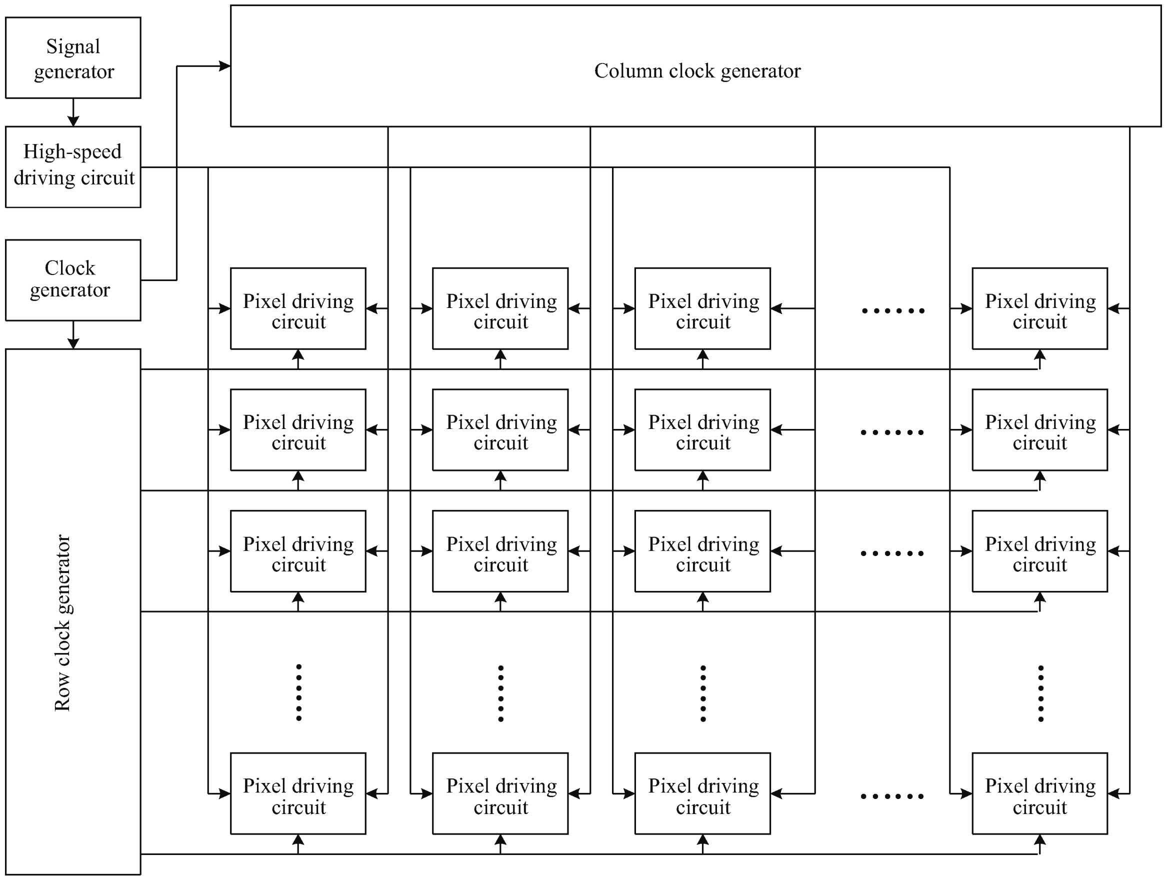

Fig. 5. Block diagram of the measurement system.

represented by voltage-controlled current sources (VCCS) I_1 and I_2, respectively. The functions f_1 and f_2 are defined in Eqs. (1) and (3). The variation of V_S due to leakages can be given by

$$\Delta V_S = \frac{1}{C_S}(I_1 + I_2)t. \tag{6}$$

This expression implies the neglectable variation of V_S on condition that I_1 and I_2 are small enough. As illustrated in Section 2, I_1 and I_2 are dominated by the voltage difference between V_A and V_S in Fig. 4, which can be expressed as

$$V_S - V_A = \frac{V_A - V_{AOP}}{A}, \tag{7}$$

where V_{AOP} is the operating point of the amplifier's output and A is the gain of the amplifier. Regardless of the mismatch, such a voltage difference approximates to zero if A is sufficient and V_A shifts around V_{AOP} just within a small range. So, a careful design can avoid the influences of switching leakages in theory and guarantee the accuracy of the voltage stored in C_S during a long period. In addition, capacitor C_S can be reduced effectively benefitting from the small switching leakages, which is very important for the limited dimension.

To evaluate the stability of the loop, the transfer function of the open-loop should be deduced from the small signal equivalent circuit of the loop. Opened at the input of the amplifier, the transfer function can be written by

$$H(s) \approx \frac{1}{\left(1 + \frac{s}{A\omega_p}\right)\left[1 + s\frac{1}{g_{m1} + g_{m2}}(C_S + C_{gs3})\right]}, \tag{8}$$

where ω_p is the main pole of the amplifier simplified as a single-pole system. g_{m1} and g_{m2} are the equivalent transconductance of the voltage-controlled current sources in Fig. 4. The equation above indicates that the loop is stable because of the low open-loop gain.

In order to prove the functions of the proposed pixel circuit, a system including a 60 × 80 pixel matrix and controlling circuits is also presented, as shown in Fig. 5. For the accuracy of the measurement, the system clock is designed according to a 600 × 800 pixel matrix, as well as the parasitic parameters. The system drives the pixel matrix point by point. Thus the maximal setup time of every pixel is approximately 40 ns with a rate of 50 frames per second.

4. Measured results

The system mentioned above is fabricated in a Chartered 0.35-μm CMOS mixed signal process. Figure 6 shows the photograph of the chip. The dimension of the pixel is 15 × 15 μm^2 and the whole chip occupies an area of 2.5 × 1.3 mm^2 including a 60 × 80 pixel matrix, clock generator, current signal generator, high speed driving circuit, output buffer, etc. The chip is measured on board with a supply from 3 to 5.5 V.

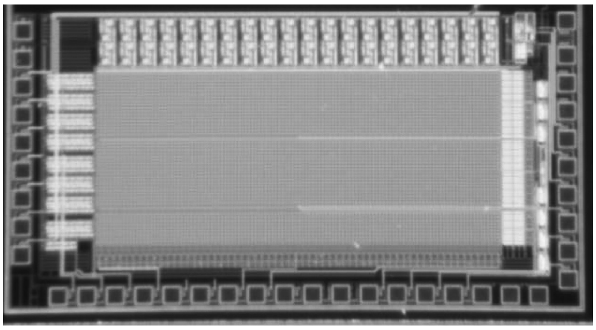

Fig. 6. Chip photograph.

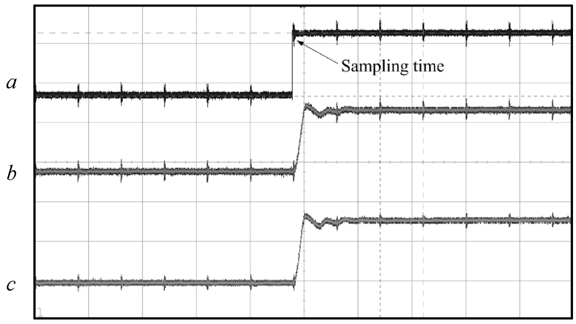

Fig. 7. Setup time of the voltage V_S, 500 mV/div, 5 μs/div. (*a*) Input step signal. (*b*) Traditional pixel circuit. (*c*) Improved pixel circuit.

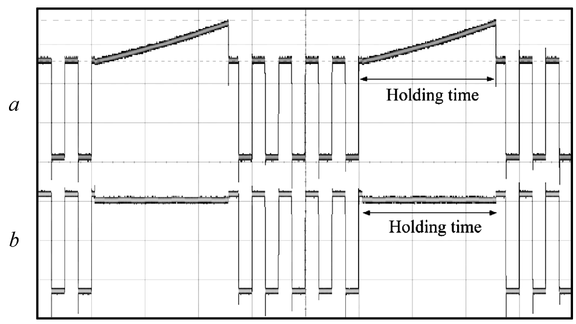

Fig. 8. Holding time of the voltage on capacitor C_S, 200 mV/div, 200 ms/div. (*a*) Traditional pixel circuit. (*b*) Improved pixel circuit.

For comparison, the traditional pixel circuit and the improved circuit have been implemented simultaneously, as shown in Figs. 1 and 3, respectively. The setup time of voltage V_S during the sampling period is presented in Fig. 7, which implies both kinds of pixel circuits can be driven within 40 ns for an 800 mV step. Figure 8 shows the holding time of the voltage on capacitor C_S. According to the results, the signal voltage on capacitor C_S of the traditional pixel circuit rises to about 210 mV within 500 ms, while that of the improved one holds fixed. Both circuits occupy the same silicon area of 15 × 15 μm^2 and the capacitor area of the traditional pixel circuit is three times that of the improved one.

The signal generator sets the output current of the pixel as

$$I_{OUT} = \frac{1}{10000}\frac{V_{in}}{R_{set}}, \tag{9}$$

where V_{in} is the input voltage and R_{set} is the setting resistor off-chip. In order to measure the output current conveniently, the

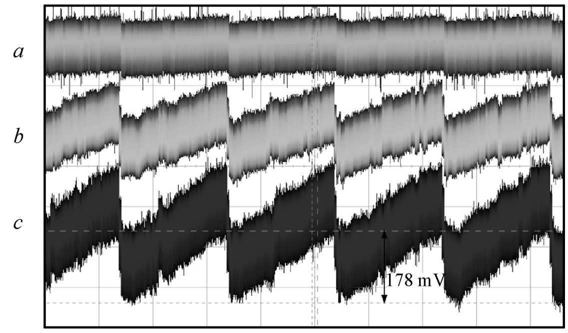

Fig. 9. Output voltage of multi-pixels. R_{set} = 1 MΩ, 100 mV/div, 500 ms/div. (*a*) 1 row. (*b*) 5 rows. (*c*) 10 rows.

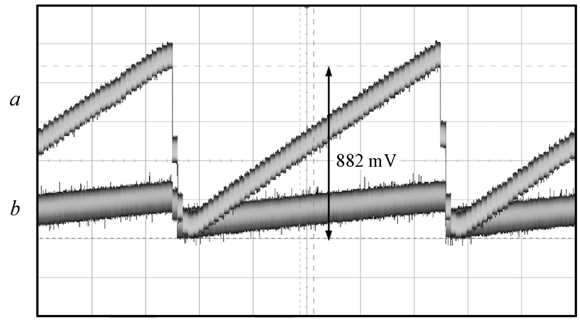

Fig. 10. Output voltage of multi-pixels. R_{set} = 100 kΩ, 200 mV/div, 200 ms/div. (*a*) 1 row. (*b*) 5 rows.

output terminals of many pixels are connected together through an off-chip 1-MΩ resistor to achieve I–V conversion. When R_{set} in Eq. (9) is 1 MΩ and V_{in} is a 1 Hz sawtooth wave from 1 to 3 V, the measured output voltages of 1 row, 5 rows and 10 rows are shown in Fig. 9. One row means 80 pixels. Similar results, only changing R_{set} to 100 kΩ are shown in Fig. 10. The results show a satisfied accuracy and linearity within the measured current range from 100 pA to 3 nA. Compared to the calculated value, the measured current error is approximately 10%, suffering from the mismatch of a large mirror ratio in micro-current condition. The pixel can work at a wider current range, but is not presented here.

5. Conclusion

An improved pixel circuit with a reduced switching leakage for an OLED micro-display has been implemented in 0.35-μm CMOS technology. The measured results show the neglectable switching leakage and the ability of long-time holding, of more than 500 ms. The improved pixel circuit exhibits satisfied accuracy and linearity in micro-current conditions proved by a scaled down system based on a 60 × 80 pixel matrix. The measured results indicate that the pixel circuit proposed in this paper is suitable for a large scale OLED micro-display with low power consumption.

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