Design and analysis of a bang–bang PLL for 6.25 Gbps SerDes*

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Abstract: An analysis illustrates the loop nonlinear performance in a bang–bang PLL. A third-order equivalent model is deduced to give an approximate evaluation of the loop parameters. The architecture of the proposed phase detector is composed of four master-slave DFFs and two XORs based on the current mode logic circuit. A no-load architecture is introduced in the XOR design. The oscillator is designed with an LC VCO implementation for the jitter requirement. A simple voltage-to-current converter is proposed to drive the loop filter. The loop filter design is described in detail, which is important to ensure the nonlinear loop stability. The chip is fabricated in a 0.18 μm CMOS technology. The experimental results show that it can achieve the frequency range of 2.995 to 3.35 GHz, and a phase noise of –118.38 dBc/Hz at 1 MHz offset. The frequency to voltage gain is 270 MHz/V. The chip consumes less than 81 mW with 1.8 V supply voltage, and it occupies a 0.5 mm^2 area.

Key words: PLL; bang-bang PD; LC VCO

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1. Introduction

The backplane communication plays a major role in determining the overall speed of modern data transmission systems. A Serializer/Desterilizer (SerDes) is used between line cards to form the high-speed data channel. OIF-CEI-02.0, which was created by the Optical Internetworking Forum (OIF), is one of the emerging SerDes standards, approved in February 2005[1−4]. This standard specifies the transceiver and the interconnect channel associated with 6 Gbps interfaces for application in high-speed backplanes, chip-to-chip interconnects, and optical modules. To provide a 3.125 GHz clock for the 6.25 Gbps SerDes core in Fig. 1[5], a clock recovery circuit is adopted, which recovers the clock from the data series after the half-rate decision feedback equalizer (DFE).

The clock recovery circuit involving a bang–bang phase detector (BB PD) has become a common design choice for high-speed applications since Gondi used a bang–bang clock recovery circuit in Ref. [6]. However, the nonlinear behavior of the bang–bang PLL is difficult to model as a traditional linear phase-lock loop (PLL) and so many studies on this topic have been performed. Walker[7] analyzed and modeled the bang–bang clock recovery circuit in his paper as a second-order system. Lee[8] considered the distinction between the linear and the saturated regions based on Ref. [7]. But the analyses given above are limited to the 2nd-order loop. Wang[9] has presented the impact of the 3rd-order pole. In this paper, a third-order behavior model is derived to evaluate the CR performance of the loop stability. The transistor level design and the test results are also described.

2. Theoretical analysis

A great deal of research on bang–bang PLL modeling has been done. In the Walker model[7], the circuits between the phase detector and VCO are modeled as two branches: the proportional branch and the integral branch. As shown in Fig. 2(a), $V_{\rm PD}$ is the output voltage of the PD and $V_{\rm ctrl}$ is the control voltage of the VCO. $K_{\rm p}$ is the coefficient of the proportional branch, $K_{\rm I}$ is the coefficient of the integral branch, and $k_{\rm v}$ is the VCO gain.

To ensure PLL loop stability, the phase variation due to the proportion branch should be larger than the variation due to the integral branch. The phase change in one update time due to the proportional connection is $\Delta\theta_{\rm bb}$, as shown in Eq. (1), here $t_{\rm update}$ is the period of the VCO. The phase change in one update time due to the integral branch is $\Delta\theta_{\rm int}$, as shown in Eq. (2). The loop stability factor ξ can be expressed as the ratio of $\Delta\theta_{\rm bb}$ to $\Delta\theta_{\rm int}$, as shown in Eq. (3). $\Delta F_{\rm bb}$ is the VCO frequency step shown in Eq. (4).

$$\Delta\theta_{\rm bb} = K_{\rm p}V_{\rm PD}K_{\rm v}t_{\rm update}, \tag{1}$$

$$\Delta\theta_{\rm int} = \frac{V_{\rm PD}k_{\rm v}K_{\rm I}t_{\rm update}^2}{2}, \tag{2}$$

$$\xi = \frac{2K_{\rm p}}{K_{\rm I}t_{\rm update}}, \tag{3}$$

$$\Delta F_{\rm bb} = V_{\rm PD}K_{\rm p}K_{\rm vco}. \tag{4}$$

The circuit between the PD and the loop filter is the charge pump, or the voltage to current converter (V/I) is shown in Fig. 1. Actually, the charge pump or V/I can be equivalent to a resistor R shown in Fig. 2(b). The $V_{\rm PD}$ is the input voltage and $V_{\rm ctrl}$ is the output voltage, the transfer function can be expressed as Eq. (5). The transfer function between the PD and the VCO in Fig. 2(a) is Eq. (6). Equations (7) and (8) can be obtained by

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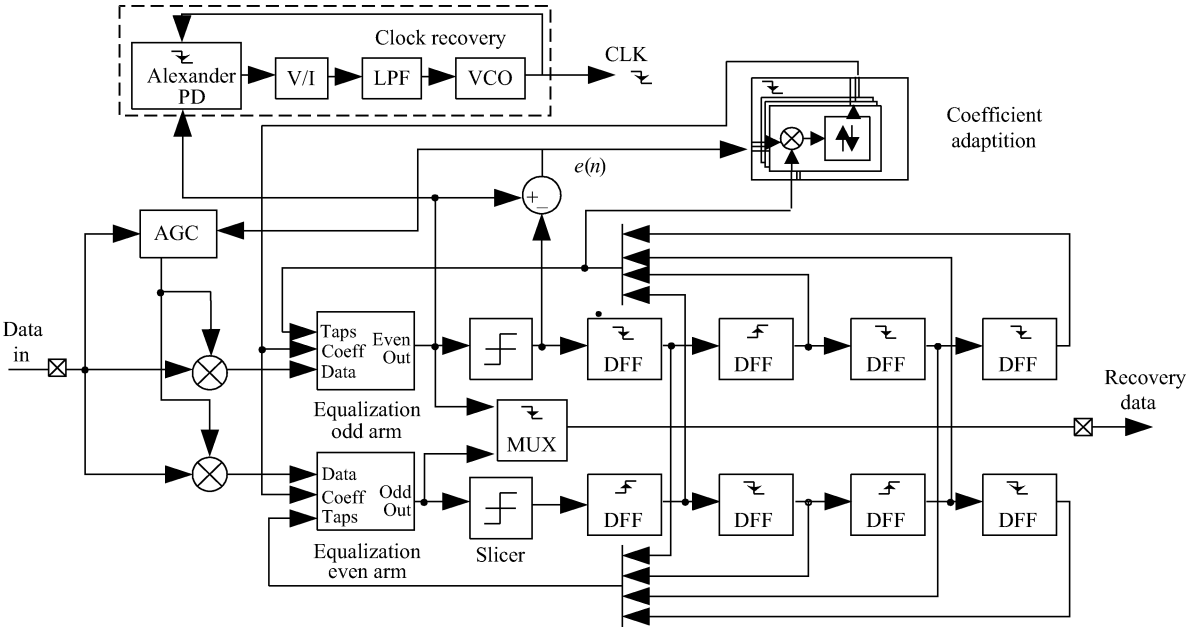

Fig. 1. The SerDes core with a clock recovery.

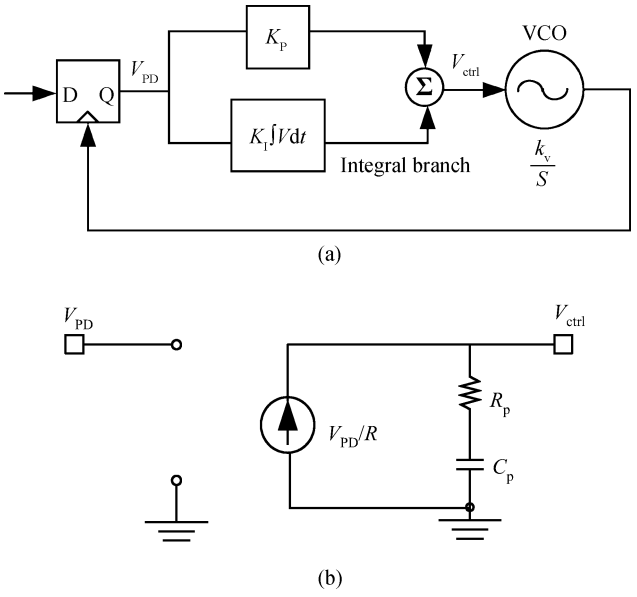

Fig. 2. (a) The two-order bang–bang PLL. (b) The nonlinear equivalent model.

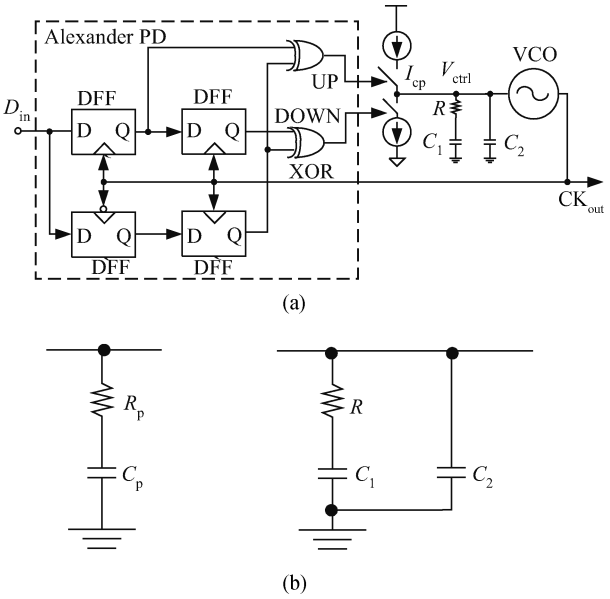

Fig. 3. (a) The third-order bang–bang PLL diagram. (b) The equivalence between the 1st-order filter and the 2nd-order filter.

comparing Eqs. (5) and (6). According to Eqs. (7), (8) and (3), the loop stability factor ξ can be expressed as Eq. (9).

$$F(s) = \frac{1 + sR_pC_p}{sRC_p}, \tag{5}$$

$$F(s) = K_p + \frac{K_I}{s}, \tag{6}$$

$$K_p = \frac{R_p}{R}, \tag{7}$$

$$K_I = \frac{1}{RC_p}, \tag{8}$$

$$\xi_{2nd} = \frac{2R_pC_p}{UI}. \tag{9}$$

When the loop filter is integrated on the chip, because the varactor and the parasitic capacitance of the VCO, the 2nd-order loop presents a 3rd-order character. As shown in Fig. 3(a), C_2 is the bypass capacitance. To reuse the nonlinear model of the 2nd-order loop, the 2nd-order loop filter is equivalent to the 1st-order filter shown in Fig. 3(b)[10]. According to the impedance expression of the 1st-order filter in Eq. (10) and the 2nd-order filter in Eq. (11), the relationships are given in Eqs. (12), (13) and (14). The stability factor of the 3rd-order loop is Eq. (15), and the VCO frequency step ΔF_{bb} is Eq. (16).

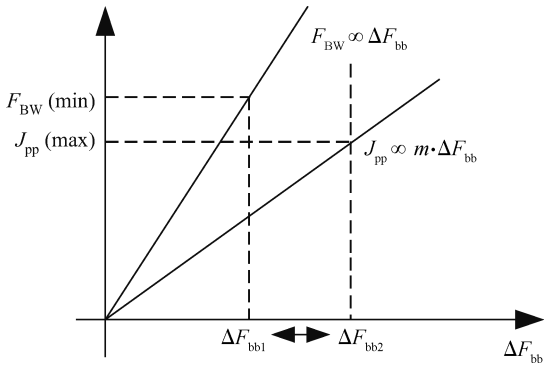

Fig. 4. The range of the ΔF_{bb}.

$$Z = R_p + \frac{1}{j\omega C_p}, \tag{10}$$

$$Z = \left(R + \frac{1}{j\omega C_1}\right) // \frac{1}{j\omega C_2}, \tag{11}$$

$$R_P = \frac{R_1 C_1^2}{\omega^2 R_1^2 C_1^2 C_2^2 + (C_2 + C_1)^2}, \tag{12}$$

$$C_P = \frac{\omega^2 R_1^2 C_1^2 C_2^2 + (C_2 + C_1)^2}{\omega^2 R_1^2 C_1^2 C_2 + C_2 + C_1}, \tag{13}$$

$$R_P C_P = \frac{R_1 C_1^2}{\omega^2 R_1^2 C_1^2 C_2 + C_2 + C_1}, \tag{14}$$

$$\xi_{3nd} = \frac{2R_1 C_1^2 \cdot UI}{4\pi^2 R_1^2 C_1^2 C_2 + (C_2 + C_1) \cdot UI^2}, \tag{15}$$

$$\Delta F_{bb} = \frac{V_{PD} K_{VCO}}{R} \frac{R_1 C_1^2 \cdot UI}{4\pi^2 R_1^2 C_1^2 C_2 + (C_2 + C_1) \cdot UI^2}. \tag{16}$$

The relationship between the VCO frequency step ΔF_{bb} and the jitter peak J_{pp} is given in Eq. (17). So the maximum value of ΔF_{bb} can be expressed as Eq. (18), here the J_{pp}(max) is the maximum value of the jitter peak or the jitter generation of the loop. The relationship between the VCO frequency step ΔF_{bb} and the jitter tolerance $F_{BW}(J_{pp})$ is given in Eq. (19), therefore, the minimum value of ΔF_{bb} is deduced as Eq. (20). To satisfy the requirement of the system in the jitter peak J_{pp} and the jitter tolerance $F_{BW}(J_{pp})$, the VCO frequency step ΔF_{bb} should be selected in the range between the range ΔF_{bb1} and ΔF_{bb2}, as shown in Fig. 4.

$$J_{pp} = \Delta F_{bb} \cdot UI^2, \tag{17}$$

$$\Delta F_{bb} \leqslant \frac{J_{pp}(max)}{UI^2}, \tag{18}$$

$$F_{BW}(J_{pp}) = \frac{1}{2} DF \cdot \frac{\Delta F_{bb} \cdot UI}{J_{pp}}, \tag{19}$$

$$\Delta F_{bb} \geqslant \frac{2F_{BW}(J_{pp}) J_{pp}}{DF \cdot UI}. \tag{20}$$

3. Transistor-level design

This work employs a full-rate CR architecture consisting of an Alexander phase detector (PD) and an LC voltage-controlled oscillator (VCO), as shown in Fig. 3(a). While operating as a bang–bang circuit and exhibiting a high gain, the Alexander PD produces no output in the absence of data transitions, thus leaving the V_{ctrl} signal undisturbed. The high gain of the PD obviates a charge pump, and permits the use of a simple voltage-to-current (V/I) converter to drive the loop filter. The output of the PD need not provide a high bandwidth as only their average voltages are sensed by the V/I converter; that is an important advantage of this realization over those using charge pumps. The speed, jitter, and driving capability required of the oscillator point to the use of an LC implementation.

A negative-resistance oscillator is used as the VCO, as shown in Fig. 5(a). The negative resistance adopts the CMOS architecture, because the phase noise of the CMOS architecture is lower than that of the NMOS architecture. The phase noise drops with an increase in current and a decrease in power supply[11]. The output clock signal is symmetrical about the common mode voltage by using the inverter as the negative-resistance circuit. The elimination of the noise caused by the tail current resource is an advantage, but the power-supply rejection ratio is depressed.

The output common mode voltage is set to $V_{DD}/2$ to enlarge the output frequency range of the VCO by maximizing the regulation range of the varactor. To satisfy the output requirement of high frequency, an N poly/N well varactor is used for its minor capacitance. The parallel connection of the varactor P_{var1} and the capacitance C_{fix} decreases the frequency gain, which is of benefit to the loop stability. The buffer including PM0 and NM0 isolates the VCO with the capacitance of the PD, and realizes the wave shaping function.

The proposed Alexander PD is composed of four DFFs and two XORs circuits, as shown in Fig. 3(a).The DFF (master-slave DFF) based on the current mode logic (CML) circuit is composed of two identical D-latches, which are shown in Fig. 5(b)[12]. It operates by sampling the input data with the recovered clock. The channel length of the current mirror transistor is selected to be long enough to guarantee the stability of the current supply.

The XOR circuit based on the CML is shown in Fig. 5(b). The proposed XOR circuit on the right adopts a no-load architecture, compared with the XOR in the left used in Ref. [6], which had the load resister R_L. The circuit consists of two similar sections: NM1–NM3 and NM4–NM6. The resistance R_1, R_2 and the capacitance C_0 compose the common mode feedback. When the A and B inputs are high, the NMOS NM1 is on and NM2 is cut off. The current flows through NM1 to the tail current resource I_1. When the A and B are low, the NM6 is switched on and NM5 is turned off. The current flows through NM6 to the tail current resource I_2. Therefore, there is no current flowing through the PMOS PM1, and the output V_{out} is high. When the input A is high and the input B is low, NM1 and NM2 are switched on; NM5 and NM6 are turned off. Then the current through PM1 is equal to the tail current, so the output voltage V_{out} is low. Because the load is PMOS, the low output of the circuit is high in logic and the high output of the circuit is low in logic. So the output is equal to A⊕B.

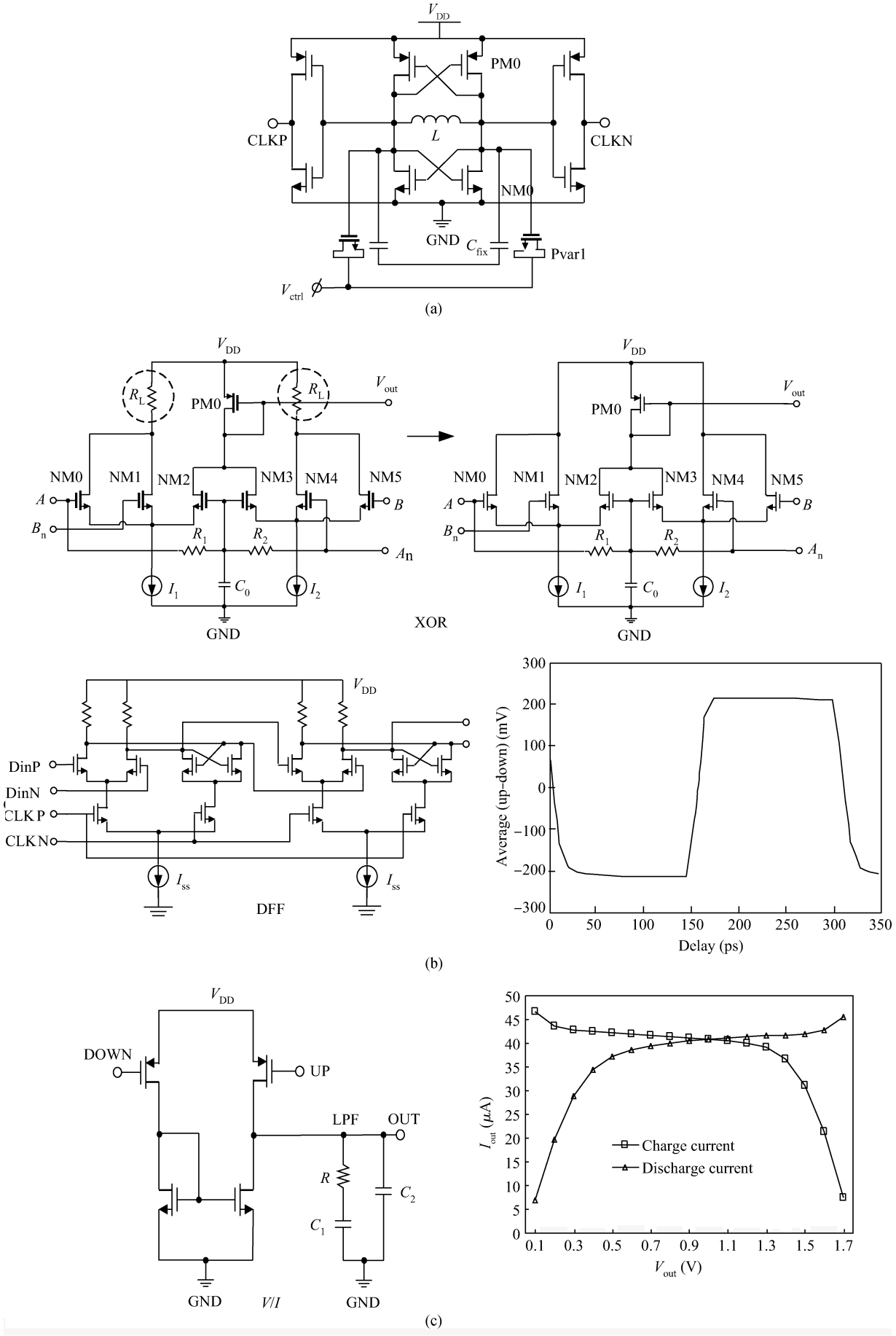

Fig. 5. Circuit diagram of the clock recovery. (a) VCO. (b) PD. (c) V/I and LPF.

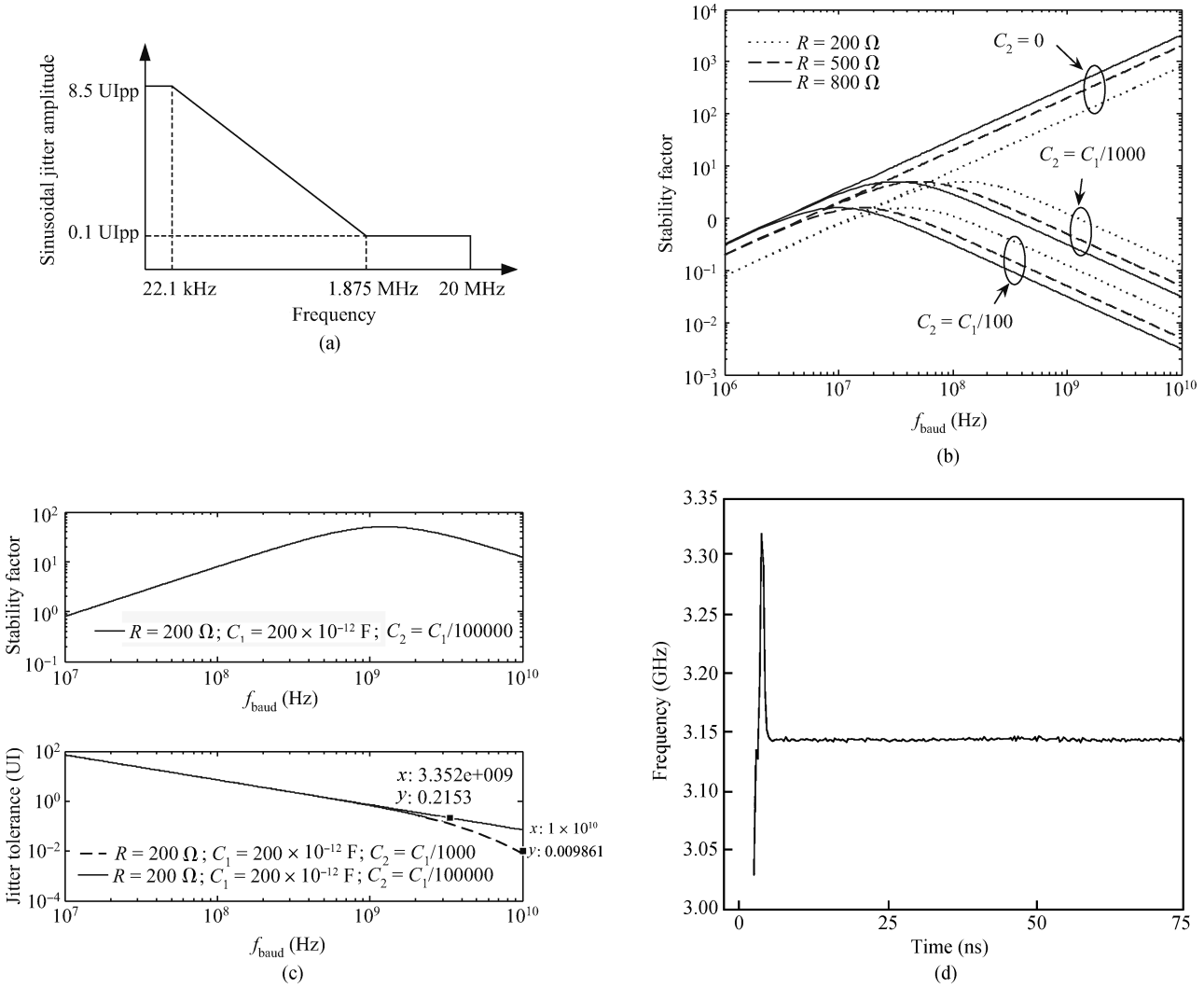

Fig. 6. The loop filter design. (a) Single tone sinusoidal jitter mask. (b) The stability factor versus R and C_2. (c) The jitter tolerance versus C_2. (d) The convergence curve of the frequency.

Figure 5(b) plots the simulated variation on average voltage of up minus down as a function of the variable phase delay. The figure illustrates that when the phase delay between the CLK and the input data is (π, 0), the average voltage is down to reduce the frequency of the VCO. When the phase delay is between (0, $-\pi$), the average voltage is up to increase the frequency of the VCO.

The V/I circuit in Fig. 5(c) is proposed to provide a 40 μA current to charge or discharge the low pass filter. The channel length of the MOS transistor has been selected to be large enough to ensure the stability of the current mirror. Furthermore, to reduce the influence of the mismatch between input transistors, a symmetrical layout has been adopted. Figure 6(c) shows the result: the charge current and the discharge match in the voltage range from 0.4 to 1.5 V, and the mismatch current is less than 8 μA.

The 2nd-order low filter is realized by the component out of the chip in favor of the regulation of the PLL performance. In XAUI standard, the requirement in the peak of the jitter transfer JG_{pp} is 10 ps, and the $F_{BW}(\text{Jitter}_{pp}) \times \text{Jitter}_{pp}$ is 0.1 $\text{UI}_{pp} \times 1.875$ MHz shown in Fig. 6(a). Using Eqs. (18) and (20), the range of the ΔF_{bb} can be determined as (0.75 MHz, 97 MHz). When the output voltage of the PD V_{PD} and the K_{vco} is constant, the value of the K_p can be selected according to Eq. (4). To ensure loop stability, the stability factor ξ should be greater than one, therefore the value of the K_I can be selected according to Eq. (3). From Eqs. (7) and (8), the range of the value of R_p and C_p can be obtained. Then the values of R, C_1 and C_2 are given by Eqs. (12) and (13). As shown in Fig. 6(b), C_2 degrades the loop stability. As the data rate increases, ξ changes from proportional-to-R to inverse ratio to R. As shown in Fig. 6(c), when R is 200 Ω, C_1 is 200 pF, and C_2 is $C_1/1000$, the jitter tolerance is less than 0.1 UI at 10 GHz; when C_2 is selected as $C_1/100000$, the stability factor ξ is larger than one and the jitter tolerance is 0.2 UI at 3.125 GHz. By simulation in cadence, the PLL loop converges after 10 ns and the convergence curve of the frequency is shown in Fig. 6(d).

The proposed current reference circuit is shown in Fig. 7(a). To drive the current reference circuit toward the desired stable state values, a start-up circuit composed of PM4, PM5, PM6 and PM7 is adopted. The circuit, in effect, is disconnected from the circuit in steady-state operation. When the supply voltage V_{DD} rises from zero to 5 V, the voltage at point

X is zero, thus, the PMOS PM4 is switched on. This action causes the current to flow into the NMOS NM8. The mirror effect in the current mirror circuit also causes the current to flow into NM7. Therefore the PTAT circuit starts to work. The diode-connected PM6 and PM7 operate as small-signal resistors. By selecting a proper size, the series resistors of PM6 and PM7 can be much larger than the drain–source resistor of PM5. As a result, the voltage at point X goes up to 5 V, and PM4 is off. Then the start-up circuit will not affect the steady-state current values.

In the input impedance-matching and common-model bias circuit of Fig. 7(b), the resistances R_3 and R_4 of the high resistance element produce the common-mode bias voltage. The resistances R_5 and R_6 match the impedance of the signal source and the connecting cable. The output buffer of Fig. 7(c) is composed of three common source amplifiers[13], and the output amplitude is 500 mV, as shown in Fig. 7(d).

4. Measurement

The bang–bang PLL was implemented in a 0.18 μm CMOS process. The chip photomicrograph has been shown in Fig. 8(a), which occupies 0.5 mm^2 of area and consumes less than 81 mW for a 1.8 V supply. The pad INPUTN and INPUTP are the input of the PRBS, the recovery clock output pads are CLKN and CLKP, and the PD output are observed by UP and DOWN. The offset between the test value and the simulation value of the bias voltage in clock buffer tail current is 26 mV. The test value of the tail current bias voltage in the PD is 26 mV higher than the simulation value. The input common mode voltages of the signal UP and DOWN are all 0.771 mV, which is 78 mV lower than the simulation. The common mode bias of the PRBS input is 1.384 V, which is 14 mV lower than the simulation value. There are 39 mV mismatches in the common-mode voltage between the clock phase and reversed phase output; they are 21 mV lower than the value in after layout simulation. The charge and discharge current of the V/I is 41 μA in simulation; correspondingly, the charge current is 53.2 μA and the discharge current is 56.3 μA in test. There is a 3 μA mismatch in the charge and discharge current of the V/I.

The test phase noise of the VCO shown in Fig. 8(b) is –118.38 dBc/Hz @ 1 MHz, although the value is –121 dBc/Hz @ 1 MHz in pre-layout simulation and –120.7 dBc/Hz @ 1 MHz in post-layout simulation. The VCO frequency voltage control characteristic is shown in Fig. 8(c), including the result of the chip test, the schematic simulation, and the post-layout simulation. In the pre-layout simulation, the frequency regulation range is 2.92 to 3.3 GHz and the frequency gain is about 272 MHz/V. In the post-layout simulation, the frequency regulation range is 2.89 to 3.25 GHz and the frequency gain is 280 MHz/V. The frequency regulation range is 2.995 to 3.355 GHz and the frequency gain is 270 MHz/V by test on chip. The 100 MHz frequency deviation between the test and the simulation is caused mostly by the fabrication process and the accuracy of the inductor spectre model. The recovered clock from the input PRBS is shown in Fig. 8(d), the value of the jitter p–p in the falling edge is 21.33 ps, as shown in Fig. 8(e).

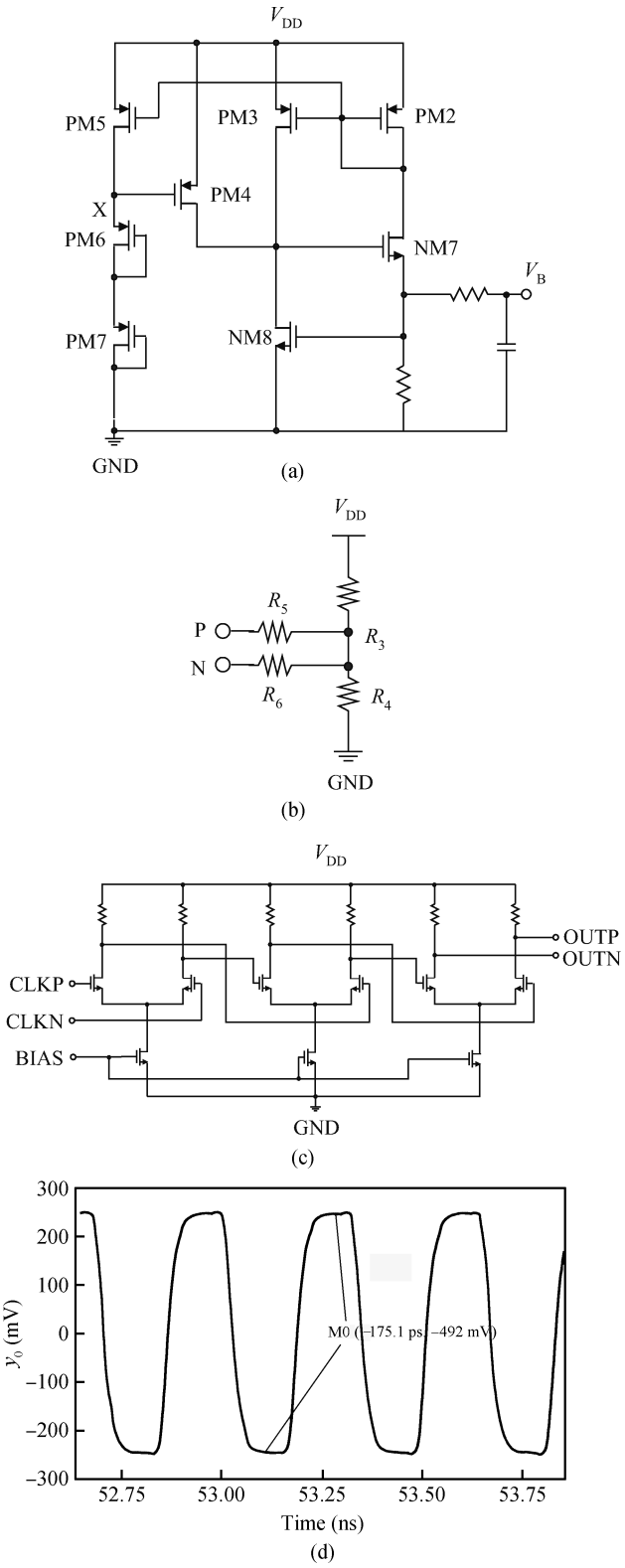

Fig. 7. Circuit diagram of the current resource and buffer. (a) The schematic of the current source. (b) The input buffer and impedance-matching circuit. (c) The schematic of the data-out buffer. (d) Output amplitude.

5. Conclusion

A 3.125 GHz clock recovery circuit is realized in a 0.18-μm CMOS technology for 6.25 Gbps backplane communica-

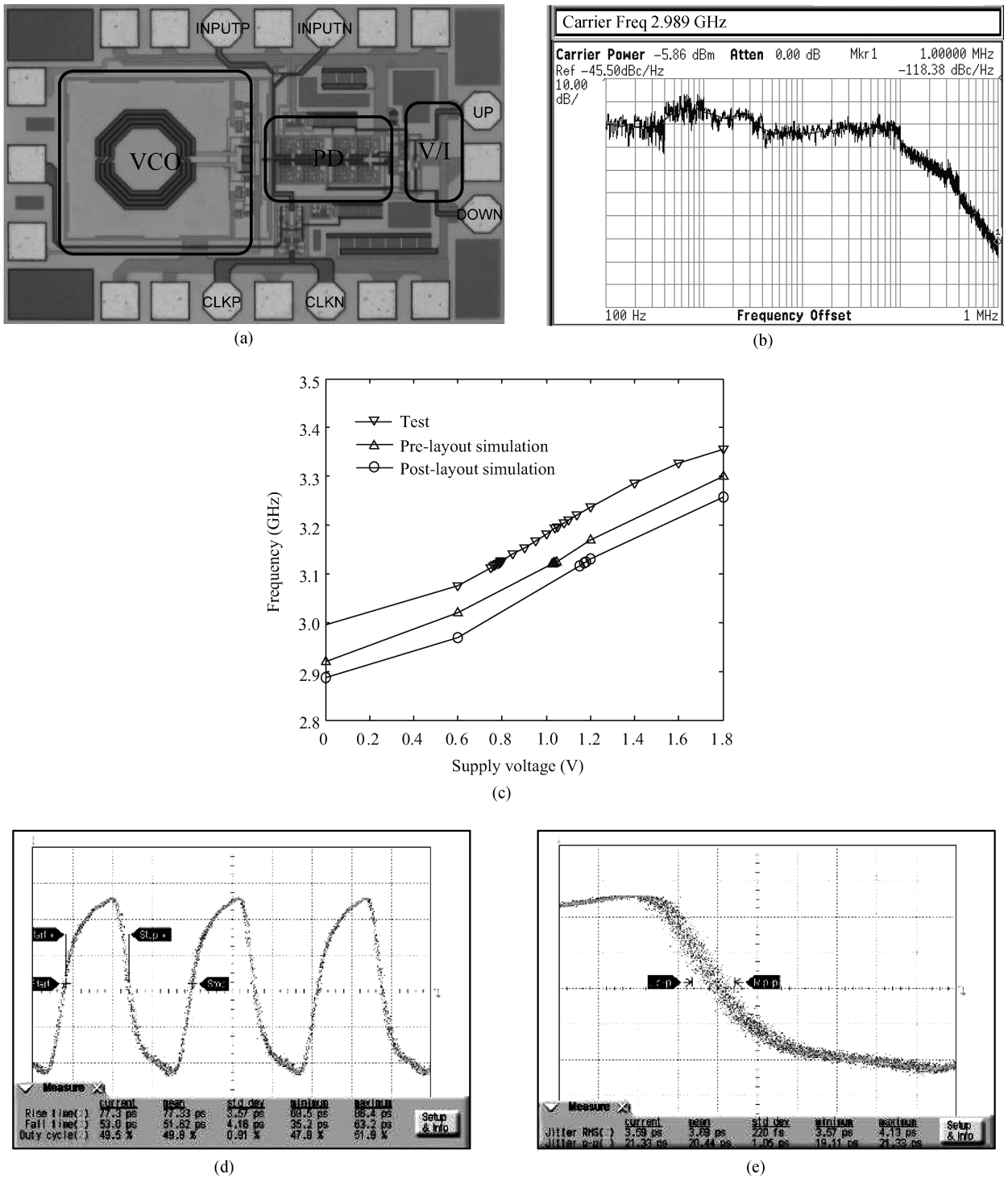

Fig. 8. The test results. (a) The chip photomicrograph. (b) The phase noise curve. (c) The VCO frequency voltage control curves. (d) The clock signal recovered. (e) the jitter in the falling edge.

tion application, which increases the circuit speed by using bang–bang PLL architecture. The nonlinear behavior model of the 3rd-order bang–bang PLL is derived in order to analyze the loop characteristics. The test result indicates that the circuit has provided a reliable clock recovery function.

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