Patterned Dual pn Junctions Restraining Substrate Loss of an On-Chip Inductor *

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Abstract: Dual pn junctions in lateral and vertical directions are formed by diffusing the p^+ on the patterned n-well in standard CMOS technology, which are inserted under the inductor in order to reduce the currents in the substrate induced by the electromagnetic field from the inductor. The thickness of high resistance is not equivalent to the width of the depletion region of the vertical pn junctions, but the depth of the bottom pn junction in the substrate are both proposed and validated. For the first time, through the grounded p^+-diffusion layer shielding the substrate from the electric field of the inductor, the width of the depletion regions of the lateral and vertical pn junctions are changed by increasing the voltage applied to the n-wells. The quality factor is improved or reduced with the thickness of high resistance by 19%. This phenomenon validates the theory that the pn junction substrate isolation can reduce the loss caused by the currents in the substrate induced by the electromagnetic field from the inductor.

Key words: on-chip inductor; patterned dual pn junctions; eddy current; substrate loss
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1 Introduction

Monolithic inductors are important components in highly integrated radio frequency circuits for wireless communication systems such as a low-noise amplifier, a voltage-controlled oscillator, and an impedance matching network. However, on-chip inductors have a low quality factor (Q) due to metal ohmic loss and conductive silicon substrate loss. Many researchers have found several methods to improve the Q of on-chip inductor[1].

The use of a patterned ground shield (PGS)[2] between the inductor metal trace and substrate increases Q by reducing the loss of electric energy due to the current induced in a silicon substrate, while at the same time not reducing the eddy current, which can significantly reduce Q. Increasing the resistance of the substrate[3,4] can reduce the eddy currents in the substrate and increase Q. These methods are not standard technology. The inductor designers aim at realizing a substantially greater quality factor at circuit operation frequency without altering the fabrication process, through such methods as using a symmetric inductor that is excited differentially[5]. Several papers[6~8] have reported the singe pn junction substrate isolation, however, dual pn junction substrate isolation structures without altering the fabrication process have not been reported and the reasons this structure can reduce the substrate loss have not been reliably validated by tape-out experiments. The eddy current would be formed in an n-well that is designed as a whole layer[6], which is larger than the substrate because the resistance of the n-well is less than that of the substrate.

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The *Q* improvement approach reported in this paper is an implementation of the patterned dual pn junctions substrate isolation structures (JSIS) underneath spiral inductors by increasing the effective resistance of the substrate. Reducing substrate losses due to JSIS are reliably validated.

2 On-chip inductor

Several planar inductor structures are possible ,including loop ,meander ,and spiral ,though spirals are preferred because of their large positive mutual inductance. Vertically stacked inductors are also compatible with the IC interconnect scheme.

2.1 Loss mechanism of eddy currents in silicon substrate

The magnetic field of the inductor is vertical to the semiconductor silicon substrate , therefore the eddy current (EC) is formed in the substrate as shown in Fig. 1. The ohmic loss is induced by the EC emitting heat energy. The inductance is reduced because the direction of the magnetic field induced by the EC is reverse to that from the inductor. Series resistance of the inductor is increased due to the transformer effect between the inductor and the substrate. Therefore ,the *Q* will be reduced by the EC in the substrate.

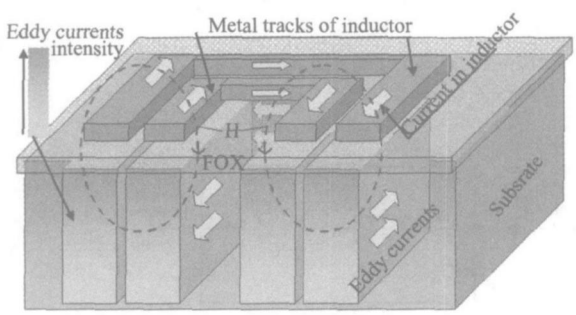

Fig. 1　Schematic of loss mechanism of magnetic energy due to current induced in a silicon substrate

2.2 Q and f_{SR}

If an inductor is modeled by a simple parallel RLC tank ,it can be shown as[2]

$$Q = 2\pi \frac{\text{peak magnetic energy-peak electric energy}}{\text{energy loss in one oscillation cycle}} \quad (1)$$

The self-resonant frequency f_{SR} can be defined as the frequency when *Q* drops to zero.

$$f_{SR} = (2\pi \sqrt{L_{eq} C_{eq}})^{-1} \quad (2)$$

where L_{eq} and C_{eq} represent the series inductance and the total equivalent capacitance of the inductor ,respectively.

3 pn junctions substrate isolation

The substrate loss is primarily caused by the eddy current , which is induced by magnetic coupling to the substrate. To prevent the occurrence of such an energy loss mechanism ,a patterned dual pn junctions structure inserted above or in the substrates is proposed. The objective of the structure is to interrupt the flowing path of the eddy current ,thus reducing energy loss.

3.1 Dual pn junctions substrate isolation

For single well technology ,the dual pn junctions (p^+np) can be formed by diffusing p^+ on the patterned n-well ,as shown in Fig. 2. The depletion region would be formed at the interface between the p^+ diffusion and n-well , which decreases the non-depleted width of the n-wells and reduces the eddy current in the n-wells.

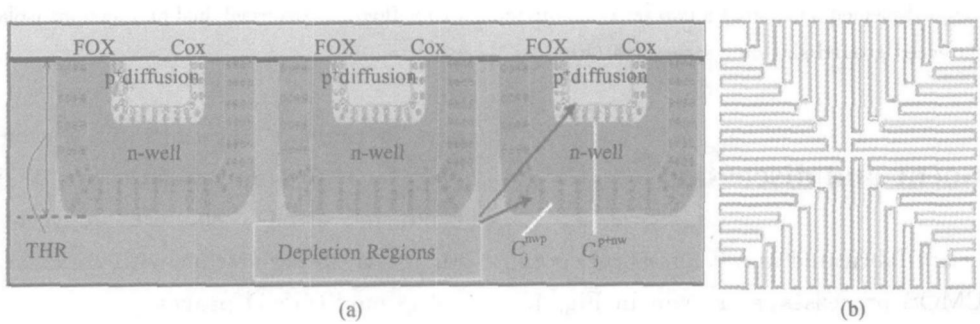

Fig. 2　Cross section (a) and planform (b) of the dual pn junctions substrate isolation

3.2 Depletion regions isolation

Figures 2(a) and (b) are the cross section and planform of the dual pn junctions substrate isolation, respectively. The resistance of the p^+-diffusion or well is less than that of the substrate. The pn junction must be made like a metal ground shielding, again in order to protest the eddy current. Thus, the thickness of high resistance (THR) is equivalent to the depth of the bottom pn junction in the substrate, as shown in Fig. 2(a). Therefore, the CMOS technology with a deep-well is a better choice for a high performance inductor with JSIS. Capacitive coupling substrate current (CCSC) and eddy current (EC) in the substrate are the results of high frequency effects and concentrate on the top of substrate. It is found that 90% of magnetic energy is dissipated within a depth of 10μm below the substrate surface[8]. Thus, depletion layers reduce the CCSC and EC, substrate losses are reduced, and the Q factor of the inductor is improved.

With an approximation of abrupt junction, the corresponding depletion width (W_{di}) is given by

$$W_{di} = \sqrt{\frac{2\varepsilon_{Si}(N_A + N_D)}{qN_A N_D}} \sqrt{V_R + \phi_{bi}} \qquad (3)$$

where N_A, N_D (atoms/cm^3) are the doping densities in the p-type material and n-type material, respectively, ε_{si} is the permittivity of the silicon, ϕ_{bi} is the built-in potential of pn junction, and V_R is the reverse bias across the junction.

The depletion width will increase with reverse bias across the junction.

3.3 Lumped-elements models

Figure 3 is the lumped-elements model of a two-port on-chip inductor for floating patterned dual pn junctions isolation and patterned ground shielding structures. At the series branch of the π-network, model parameters L_S, R_S, and C_S represent the series inductance, series resistance, and inter-turn fringing capacitance of the inductor, respectively. The model parameter C_{m_s} represents coupling-capacitance between the suspended inductor body and the substrate (where C_{ox} is the capacitance of the oxide layer and C_j is the capacitance of the pn junction). C_{sub} and R_{sub} represent the capacitance and resistance of the substrate, respectively. R_{PGS} represents the resistance of the patterned ground-shielding layer in parallel with the substrate.

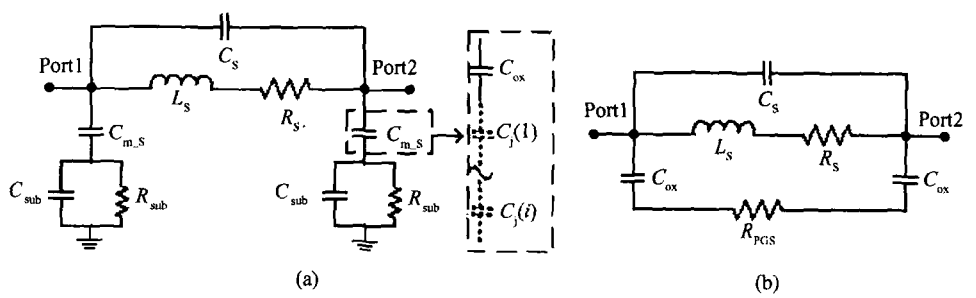

Fig. 3 Lumped-elements model of a two-port on-chip inductor for floating patterned dual pn junctions isolation (a) and for patterned ground shielding structures (b)

4 Experiment and discussion

Inductors are fabricated in a 0.35μm two-poly four-metal CMOS processes, as shown in Fig. 4. The prototype chips also include the de-embed layouts to calibrate the on-wafer testing wiring and pads[10]. On-wafer measurement of inductors is conducted using a network analyzer and cascade microtech probe station with coplanar ground-signal-ground (GSG) probes.

The die photo and layout of the pnp substrate

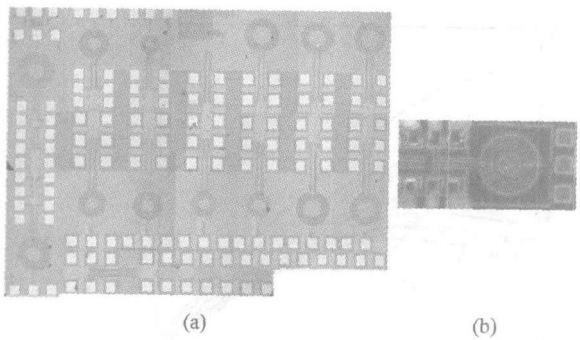

Fig. 4　Die photos of the inductors in 0. 35μm CMOS processes (a) and one inductor with probes (b)

isolation structure are shown in Fig. 5. The space between the adjacent n-well slots is 1. 1μm, which is the minimum space that design rule check permits under a 3. 3V source voltage. The p-substrate and p^+ diffusion layer are connected with the ground while the n-well is connected with the bias voltage (V_R). Thus, the electric fields of the inductor are terminated at the p^+ diffusion layer and the pn junction capacitor does not have an effect on the parasitical capacitance and f_{SR} of the inductor (in order to validate the reduced eddy current due to JSIS). Ohmic loss from the eddy currents is only substrate loss. A lumped-elements model of a two-port on-chip inductor with a grounded p^+ shielding layer is shown in Fig. 3(b).

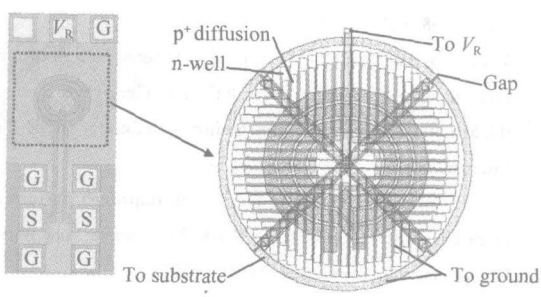

Fig. 5　A single-end spiral inductor with pnp isolation structure

Quality factors and the self-resonant frequency of the inductor with n-well voltages are shown in Fig. 6. Increasing the voltage applied to the n-wells increases the depletion region laterally between them and vertically beneath them. With rising THR, the substrate eddy currents are reduced; therefore, L_s is increased and R_s is decreased, as shown in Fig. 7. Thus, the maximum quality factor is increased with V_R from 0V to 3V by a further 19 %. The frequency of the maximum $Q(f_{MQ})$ and f_{SR} of the inductor are reduced because the reduced quantity of the inductance due to eddy currents is decreased. From 4V V_R the depletion regions of two neighbor n-wells touch. The lateral pn junction dies away at 7V V_R and the THR is not only the depth of the bottom pn junction in the substrate, but also the relatively thinner thickness of the depletion of the vertical pn junction. Thus, increasing V_R from 3V to 7V decreases the maximum quality factor by a further 19 % and the f_{MQ} and f_{SR} of the inductor are increased because the reduced quantity of the inductance due to eddy currents are increased. This phenomenon validates the theory that the JSIS can lower the loss induced by the eddy currents in the substrate. The capacitive coupling substrate current and eddy current in the substrate are the results of high frequency effects and concentrate on the top of the substrate. This result can be safely extended to obtain the conclusion that the JSIS can also reduce the loss caused by the capacitive coupling currents in the substrate.

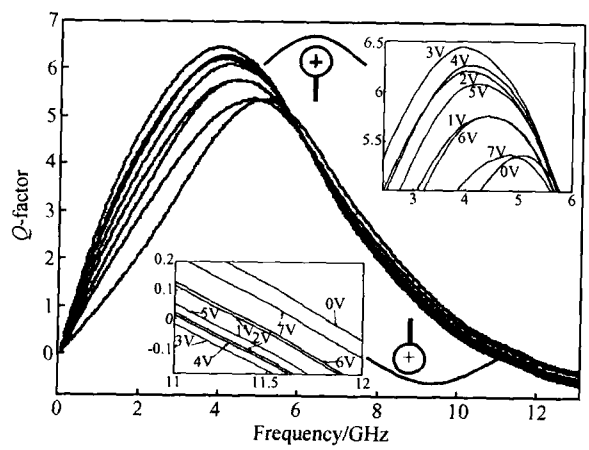

Fig. 6　Quality factors of the inductor with n-well distance 1. 1μm and at n-well different bias voltages

5　Conclusion

The substrate magnetic losses of the CMOS inductor are analyzed in detail and new substrate i-

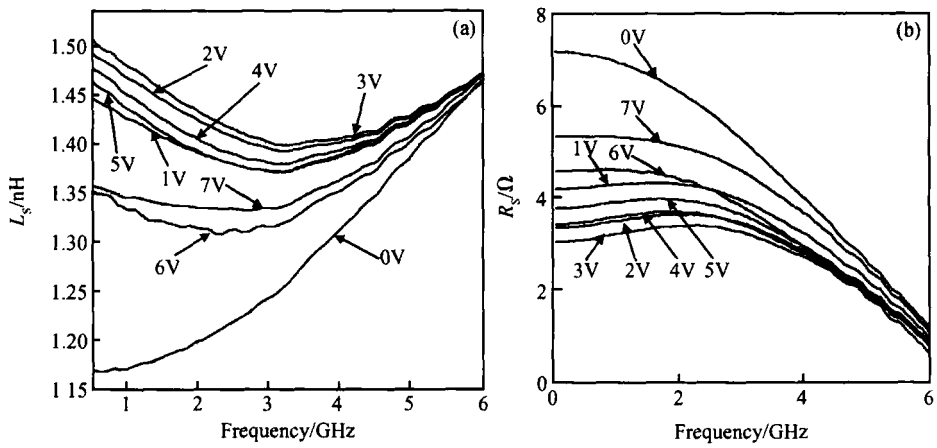

Fig. 7 L_S and R_S of the single-end spiral inductor with PNP isolation structure

solation structures for inductors consisting of alternating patterned dual pn junctions with voltage controlled, variable lateral and vertical depletion regions are presented. The structure covers the whole area underneath an inductor and is compatible with standard digital CMOS process flow. The THR is not equivalent to the thickness of the depletion regions of the vertical pn junction but the depth of the bottom pn junction in the substrate. Applying a voltage to the structure alters depletion regions and the number of free carriers underneath the inductor. The THR is thus increased. The eddy current in the substrate is reduced by the depletion of the pn junction. Therefore, the inductance is increased because the reduced quantity of the inductance due to eddy currents is decreased. For the first time, pn junction substrate isolation that can reduce the substrate loss caused by the eddy currents is reliably validated. The maximum quality factor is increased by 19%, which validates the theory that the pn junction isolation substrates can reduce the substrate loss caused by the eddy currents and capacitive coupling currents in the substrate. Dual pn junctions substrate isolation structure and deep-well technology are better choices for a high performance inductor with JSIS. Using a ground p^+ diffusion layer and patterned dual pn junction with controlled voltage, the electric energy loss and magnetic energy loss in the substrate can be reduced.

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放射状双 pn 结抑制片上电感衬底损耗 *

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摘要: 使用标准 CMOS 工艺 ,在放射状的 n 阱上面扩散 p^+ ,使垂直和水平方向形成双 pn 结 ,将此结放在电感的底部用来抑制衬底损耗. 提出并实验证明了该结构形成的高阻区厚度不是垂直 pn 结耗尽层的厚度 ,而是最低层的 pn 结的深度. 首次通过接地的 p^+ 扩散层屏蔽电感到衬底电场 ,水平和垂直 pn 结耗尽层厚度随着 pn 结反向偏压升高改变衬底有效的高阻区厚度 ,电感品质因数跟随高阻区厚度升降 ,有效地证明了 pn 结衬底隔离可以降低电感的衬底电流造成的损耗.

关键词: 片上电感; 放射状双 pn 结; 涡流; 衬底损耗

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