

VLSI Implementation of a Single-Chip DVB-C Demodulator^{*}

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Abstract: A single-chip DVB-C quadrature amplitude modulation (QAM) demodulator is proposed, which integrates a 3.3V 10bit 40MSPS analog-to-digital converter and a forward error correction decoder. The demodulator chip can support 4~256 QAM with variable bit rate up to 80Mbps. It features a wide carrier offset acquisition range, optimal demodulation algorithm, and small circuit area. The chip is implemented in SMIC 0.25 μ m 1P5M mixed-signal CMOS technology with a die size of 3.5mm \times 3.5mm. The maximum power consumption is 447mW.

Key words: QAM demodulator; VLSI implementation; carrier recovery; blind equalization

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1 Introduction

Quadrature amplitude modulation (QAM) demodulators are widely used in the physical layer interface of digital cable TV and cable modems^[1,2], as well as many other high-speed digital communication transceivers.

According to DVB-C and ITU J83-A specification^[1], it is possible to transmit one HDTV or 2~4 SDTV programs in a single 8MHz/6MHz channel with QAM modulation. For such kinds of wideband applications, it is impractical to implement the demodulation algorithm with general purpose DSPs due to their insufficient performance and high cost. Therefore, dedicated ASIC implementation is the right choice for digital cable TV demodulators.

Several ASIC implementations of QAM demodulators were proposed^[3~9]. A QAM receiver integrated with a 10bit ADC and FEC decoder was

presented in Ref. [3], but it had several shortages, such as lacking the capability to directly sample the signal with 36M/44M IF, a fixed sampling rate with 4x IF frequency, and a low carrier frequency offset acquisition range. Reference [4] introduced a QAM demodulator with a carrier frequency offset range of 80kHz, which had a relatively large area and less integration level. Reference [5] proposed a highly integrated QAM demodulator, but from the architecture of the carrier recovery loop, it can be concluded that the carrier acquisition range is not very large. Reference [6] introduced a VLSI architecture for a blind QAM demodulator which used a normal four-corner carrier recovery algorithm. Reference [7] proposed a 64/256QAM receiver with a symbol rate up to 8Mbaud, but its implementation loss was large. Reference [8] aimed for low power dissipation but it needed a complex architecture of two additional digital to analog converters (DAC). Reference [9] proposed a low-IF QAM transceiver

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but with single mode.

In this paper, we propose a monolithic multi-mode QAM demodulator with an integrated direct IF sampling ADC and FEC decoder. Compared with existing QAM receivers, our demodulator has a large carrier frequency offset correction, robust blind demodulation algorithm and small circuit area.

2 Demodulator architecture

2.1 Principles of QAM demodulation

Figure 1 shows the block diagram of the proposed QAM demodulator.

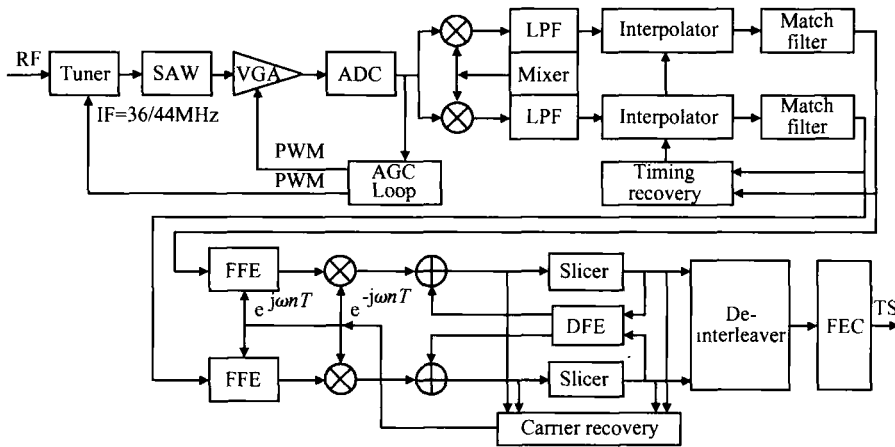


Fig. 1 Block diagram of the proposed QAM demodulator

The modulated QAM RF signal is down-converted to 36/44MHz IF by a TV tuner, then the IF signal is filtered with a band-pass surface acoustic wave (SAW) filter to remove out-of-band noise and interference. The output signal of the SAW is amplified by a voltage controlled variable gain amplifier (VGA) to fully utilize the resolution of the ADC. Tuner, SAW, and VGA are placed in the analog front end as discrete components, which will not be integrated into the QAM demodulator.

A 10bit ADC directly samples the VGA output at a clock frequency of 28MHz or 36MHz (according to the IF frequency). The signal is then down-converted to base-band by a digital mixer^[10] and filtered by a pair of low pass image rejection filters. A timing recovery loop and fully digital interpolator are used to recover the correct sampling frequency/phase of the QAM symbol. Joint carrier recovery and blind equalization cooperate to remove the carrier frequency offset and impairments due to

the channel.

The output of the equalizer is sent to a DVB compliant de-interleaver to improve performance over impulse and burst noise. A (204, 188) Reed-Solomon (RS) decoder is then used to correct up to 8 bytes of error in a 204 bytes MPEG frame.

Finally, the MPEG transport stream (TS) data from the output of the QAM receiver is sent to an MPEG decoder to recover the video and audio signals.

2.2 Timing recovery

In the QAM demodulator, there are four control loops correlated with each other — automatic gain control (AGC), timing recovery, carrier recovery, and equalization. These loops must be locked to their appropriate states before correct demodulation. It is a major issue in a QAM demodulator to make these loops work properly under various channel distortion.

Prior to carrier recovery and equalization ,timing in the demodulator must be synchronized to the received symbols by the timing recovery loop shown in Fig. 2.

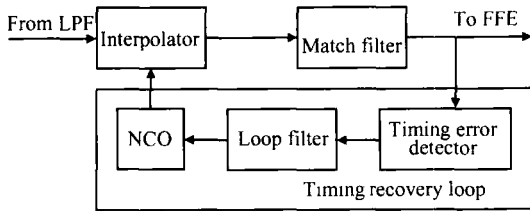


Fig. 2 Timing recovery loop

A polynomial interpolator that supports variable baud rate adjusts the sampling time by a numerically controlled oscillator (NCO). The resulting timing-recovered data stream at the output of the interpolator is then filtered by the match filter , which is implemented using the canonic signed digit (CSD) architecture. The timing recovery loop consists of a timing error detector ,loop filter ,and NCO. The timing error detector calculates timing error from the output of the match filter. NCO employs the filtered timing error signal that passed through the loop filter to produce the variable baud rate clock. When the timing recovery loop has been locked ,the received symbol is sampled with correct frequency and phase.

2.3 Joint carrier recovery and blind equalization

The AGC and timing recovery loops work independently in the first step of demodulation ;however ,carrier recovery and blind equalization must work in cooperation with each other due to the mutual effect between channel distortion and carrier frequency offset.

Figure 3 shows the details of the joint architecture of carrier recovery and blind equalization. The blind equalizer consists of a feed-forward equalizer (FFE) and a decision feedback equalizer (DFE) ,which is coupled with the carrier-recovery loop. The carrier-recovery loop consists of an optimal frequency detector (FD) , a phase detector (PD) ,a loop filter ,and a digital control oscillator

(DCO) .

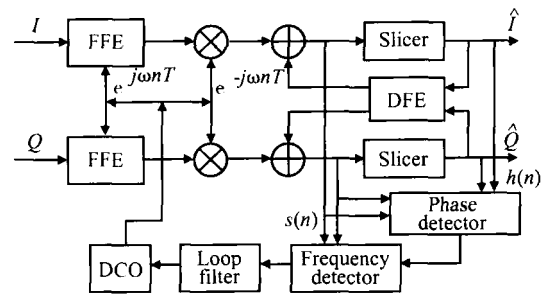


Fig. 3 Joint carrier recovery and blind equalization

The optimal FD receives the soft decision $s(n)$ of the equalizer to improve the performance of frequency offset acquisition , which is the key technique of the joint architecture. The carrier-recovery loop using the conventional decision directed (DD) algorithm^[3,11] is sensitive to channel impairment without the optimal FD. The optimal FD can acquire a large frequency offset quickly ;even the signal noise ratio (SNR) is relatively low. However , the FD cannot acquire a low steady-state jitter. Thus ,in order to lower the steady-state jitter and eliminate the phase offset ,the carrier-recovery loop then switches to phase detecting mode when frequency offset is locked. The phase detecting mode needs the $s(n)$ and hard decision $h(n)$ to track the phase offset ,which uses a normal DD algorithm.

Additionally ,in order to improve the acquisition range of the frequency offset ,we incorporate a frequency sweeping control unit in the carrier-recovery loop. When the FD does not lock at in a certain time ,a sweeping control unit will adjust the frequency of the digital mixer periodically until the FD locks. With the aid of the frequency sweeping , the performance of our carrier recovery loop is better than those in Refs. [11 ,12]. For typical DVB-C applications with 6. 875 MBaud ,our demodulator can acquire a frequency offset up to $\pm 18\%$ baud rate ,i. e. more than 1MHz.

2.4 ISI cancellation and blind equalizer

In high-speed digital communication ,the inter symbol interference (ISI) introduced by the chan-

nel is the main cause for significant performance degradation. A blind equalizer is indispensable for reducing the ISI of digital TVs without training sequences.

VLSI implementation of the blind equalizer is based on an adaptive finite impulse response (FIR) filter or infinite impulse response (IIR) filter, so the circuit area of such equalizers is very large. In order to design an area-efficient QAM receiver, it is

very important to optimize the equalizer.

The intrinsic frequency response of the cable channel, such as ripple and echo, can be modeled as FIR filters, thus we adopt the blind equalizer with an 8-tap FFE and a 16-tap DFE to cancel ISI. The equalizer architecture is shown in Fig. 4, which is implemented in transposed form. The transposed filter has a constant critical path delay and good timing stability.

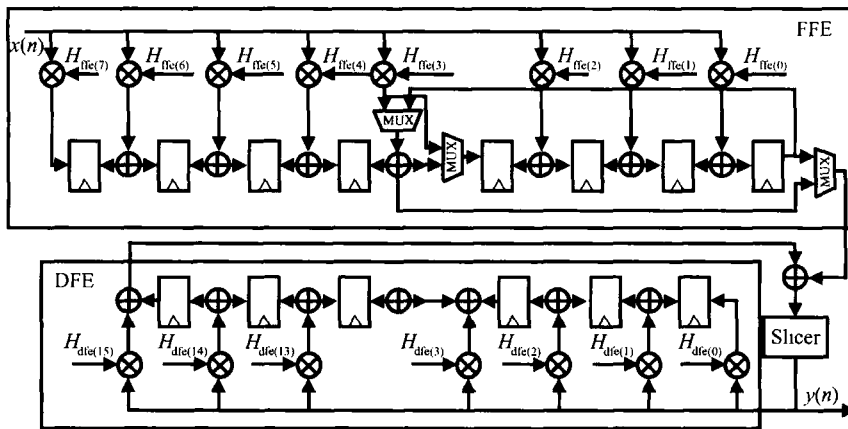


Fig. 4 Equalizer architecture

The FFE, as shown in the upper side of Fig. 4, can be configured as either T -space or $T/2$ -space mode via 3 additional MUXs. The input rate and output rate are both $1/T$ in T -space mode; however, the input rate and output rate are $2/T$ and $1/T$, respectively, in $T/2$ -space mode. The MUXs can control the output with the rate of $1/T$ in both modes. The improved structure reduces area cost compared to the normal fractionally spaced equalizer (FSE). The lower part of Fig. 4 is the DFE. The FFE and DFE are used to cancel the pre-cursor and post-cursor ISIs, respectively.

The equalizer uses a dual-mode of the constant modulus algorithm (CMA) and least mean square (LMS) algorithm to update the tap coefficients, i. e. $H_{ffe(0)} \sim H_{ffe(7)}$ and $H_{dfe(0)} \sim H_{dfe(15)}$. CMA only concerns the power of QAM signals, which is insensitive to the carrier frequency offset. Therefore CMA is used prior to the carrier recovery when QAM signals are severely distorted by cable

channel. But CMA cannot compensate for the channel distortion completely, so LMS is then used to get global convergence with perfect properties once frequency and phase offset have been eliminated.

2.5 Other channel impairments and solutions

Besides the carrier frequency offset and ISI described above, channel impairments include (1) AM and FM hum modulation, which are amplitude modulation and frequency modulation, respectively, caused by coupling of low frequency AC power; (2) thermal noise, which is modeled as white Gaussian noise; (3) impulsive and burst noise, which are determined by the surroundings.

Dual analog AGCs are used to compensate for the amplitude attenuation of cable plant response, one is for tuner gain control (the other is for IF amplifier control). Compared with single AGCs^[3-5], dual AGCs have larger dynamic range and less distortion.

AM modulation is compensated for by a digital AGC placed after the match filter.

A RS decoder, together with a convolutional de-interleaver with an interleaving depth of 12, is used to resist white noise and burst noise.

3 Chip implementation methodology

3.1 Design flow

Design of a high performance QAM demodulator chip is a challenging task. Particularly the all-digital QAM demodulator with integrated 10bit ADC needs a mixed-signal design flow.

Firstly, a detailed functional specification of the QAM demodulator is specified which defines the baud rate, mode of QAM constellation, clock frequency, etc. Table 1 is a brief of this demodulator.

Table 1 Functional specification of the demodulator

QAM mode	4/ 16/ 32/ 128/ 256QAM
Baud rate	1 ~ 10M
Carrier offset	$\pm 18\%$ baud rate
Baud rate offset	± 400 ppm
AGC	Dual PWM output
ADC	10bit, 40MSPS
RS decoder	(204, 188)
Interleaver	Convolutional interleaver, depth = 12
Output interface	DVB common interface
Clock frequency	56/ 72MHz

Secondly, we use C and Matlab to describe functional models of the QAM demodulator. Both floating point and fixed-point models are developed. After extensive algorithm and architecture exploration, we shall get a robust QAM demodulation algorithm suitable for chip implementation.

Thirdly, we define the detailed VLSI architecture such as module partition, system control interface, clock strategies and so on. After evaluating the pros and cons of different architectures, optimized chip architecture is validated.

Finally, we implement the chip according to the optimized architecture. The digital circuits are designed with Verilog HDL while the analog circuits are designed at the transistor level with sche-

matic entry. Verification of the digital and analog circuits adopts advanced mixed-signal methodology.

3.2 Clock strategies

Clock strategies are very important for reliable chip design. We divide the demodulator into two clock domains: system clock domain (clk_sys) and 4 × baud rate clock domain (clk_b4). The clk_b4 is derived from clk_sys using a NCO. The rising edge of clk_b4 is synchronized with the falling edge of clk_sys, which ensures reliable data transfer between the two clock domains.

Compared with the clock strategies in Ref. [3], our method is more reliable and greatly facilitates the clock tree generation during logic synthesis and layout design.

The system clock is generated by an on-chip PLL with low phase noise (-120 dBc/Hz @ 100kHz). The PLL is programmable to output a 56MHz or 72MHz clock according to different IF frequencies.

3.3 Area reduction techniques

Several area reduction techniques are adopted in this demodulator.

Due to the nearly identical function of the in-phase and quadrature-phase branches of the QAM demodulator, interleaving is used to reuse the computation units in both branches. This technique is adopted in modules such as image rejection low pass filters, interpolator and match filters.

The complex equalizer occupies a large proportion of the area in a whole chip; therefore, we use a multiplier-sharing technique to reduce the number of multipliers from 4 per tap to only 1 per tap.

4 Experimental results

Figure 5 describes the locking process of a 256QAM under severe channel distortion and frequency offset. Fig. 5(a) shows the constellation after CMA equalization; we cannot really identify the

QAM constellation due to frequency offset. Fig. 5 (b) shows the constellation after frequency offset recovery. The constellation does not rotate anymore, but does still have a certain phase offset. After phase recovery, the QAM constellation has the right position, which is shown in Fig. 5 (c). Due to

the property of the CMA algorithm, the residual noise is still very large. After switching from CMA to LMS mode, the SNR of the QAM constellation is greatly improved, which can be found in Fig. 5 (d).

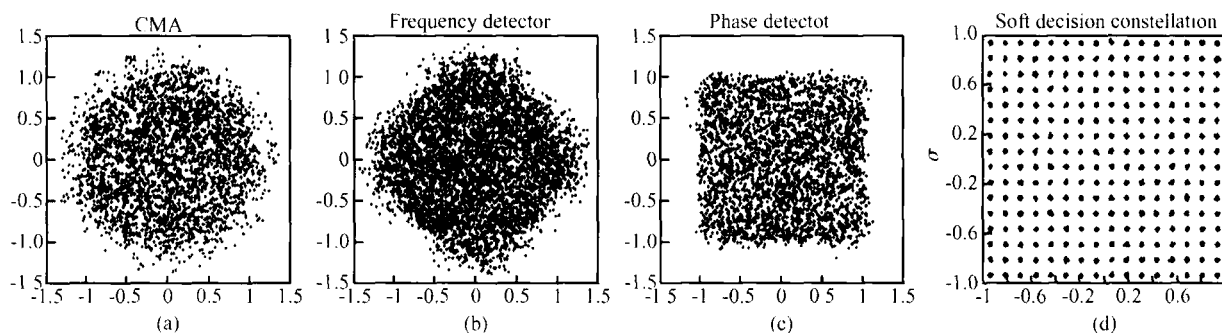


Fig. 5 256QAM with frequency offset locked

Figure 6 shows the bit error rate (BER) performance before the FEC decoder. The measured BER performance is very close to the theoretical estimation. Its implementation loss is less than 0.5dB under 256QAM @BER = 1×10^{-4} (uncoded).

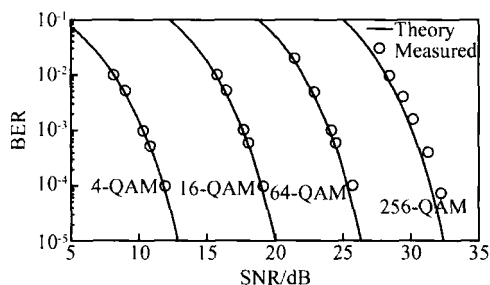


Fig. 6 BER performance of proposed QAM demodulator

The ASIC chip is fabricated in SMIC 0.25 μ m 1P5M mixed signal CMOS technology. The core area of the chip is 3mm \times 3mm and the die size is 3.5mm \times 3.5mm. The total transistor number is 6.4×10^5 K. The chip is packaged in a 128-pin QFP. The supply voltage of the analog circuit and digital circuit are 3.3V and 2.5V, respectively. The maximum power dissipation is 447mW at 6Mbaud.

The die microphotograph of the chip is shown

in Fig. 7. In the figure, ADC and PLL are located in the upper right corner of the chip. The remaining area is the digital logic circuit and memory unit.

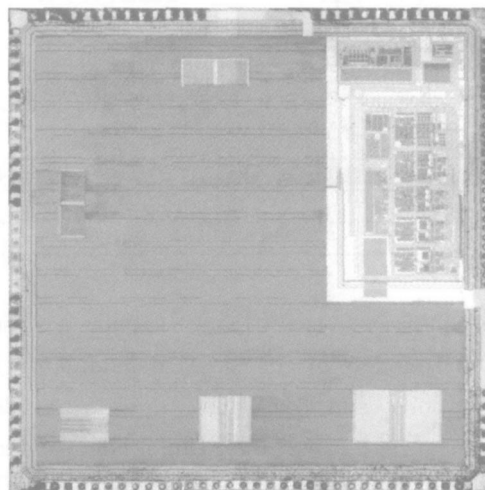


Fig. 7 QAM demodulator die microphotograph

We test the chip in a digital cable TV system, which consists of transmitter, receiver and cable channel. The transmitter comprises a DVD player, DVB-C compliant encoder, and QAM modulator. The receiver includes the analog front end (tuner, SAW filter and IF amplifier), the proposed QAM demodulator, a MPEG decoder, and a TV monitor. From Fig. 8 the oscilloscope shows the correct

MPEG TS signals labeled Syn , Error and Valid , etc. The video of high quality (BER 1×10^{-12}) shown in Fig.9 further demonstrates the robust-

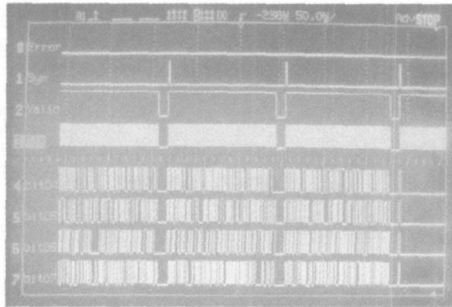


Fig. 8 MPEG TS signals



Fig. 9 Test system for QAM demodulator

ness of the proposed demodulation algorithm and its VLSI implementation.

5 Conclusion

An area efficient high performance 4 ~ 256QAM demodulator chip has been designed with a maximum bit rate of 80Mbps and a frequency offset acquisition of $\pm 18\%$ baud rate. The demodulator IC integrates high precision analog functions such as a 10bit A/D converter and PLL for an on-chip clock generation referenced to an off-chip crystal. The QAM demodulator meets all the requirements of DVB-C/ ITU J83-A.

Table 2 shows the comparison results of other reported QAM demodulators. The advantages of our demodulator are obvious. It features a larger maximum baud rate ,wider carrier offset acquisition range ,high integration level ,and low circuit complexity.

Table 2 Comparison of existing QAM demodulators

	Tan ^[3]	Yamanaka ^[4]	D Luna ^[5]	Zhang ^[6]	Shin ^[7]	Fukuoka ^[8]	Chang ^[9]	This work
QAM mode	4 ~ 1024	16/ 64/ 256	4 ~ 256	64	64/ 256	4/ 16/ 32/ 64	64	4 ~ 256
Baud rate	1 ~ 7M	< 8.25M	1 ~ 7M	0.875 ~ 7M	< 8M	7M	5.38M	1 ~ 10M
Carrier offset	N/ A	± 80 kHz	N/ A	N/ A	N/ A	± 200 kHz	± 100 KHz	± 1.8 MHz
Baud rate offset	N/ A	N/ A	N/ A	N/ A	N/ A	± 60 ppm	± 200 ppm	± 400 ppm
AGC	1 * PWM	1 * PWM	1 * PWM	N/ A	N/ A	8-bit DAC	N/ A	2 * PWM
ADC	10bit	-	10bit	-	10bit	8bit	-	10bit
PLL	Y	-	Y	-	-	-	-	Y
RS decoder	(204 ,188)	-	(204 ,188)	-	-	(204 ,188)	-	(204 ,188)
Interleaver	Y	-	Y	-	-	Y	-	Y
Technology	0.5 μ m	0.5 μ m	0.35 μ m	-	0.35 μ m	0.35 μ m	0.35 μ m	0.25 μ m
Chip area	7mm \times 6.7mm	12.87mm \times 12.49mm	8mm \times 8mm	-	-	N/ A	5.5mm \times 5.5mm	3.5mm \times 3.5mm
Tran number	650 K	880 K	2.3M	-	210 K gates	640 K	280 K gates	640 K

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一种单芯片 DVB-C 解调器的 VLSI 实现*

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摘要: 设计了一个单芯片实现的用于 DVB-C 的 QAM 解调器. 片上集成有 3.3V 10 位精度的 40MSPS 模数转换器及 FEC 前向纠错解码器. 该芯片支持 4~256QAM 多种模式, 最高码率达 80Mbps, 具有宽的载波频偏捕获范围. 采用改进的算法及 VLSI 实现结构, 性能稳定, 面积优化. 采用 SMIC 0.25 μ m 1P5M 混合信号 CMOS 工艺制造, 面积为 3.5mm \times 3.5mm, 最大功耗为 447mW.

关键词: QAM 解调器; VLSI 实现; 载波恢复; 盲均衡

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