A 59mW 10b 40Msample/ s Pipelined ADC *

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Abstract : This paper describes a 3. 0V ,10b ,40Msample/ s analog-to-digital converter (ADC) fabricated in a 0. 25μm CMOS technology. Through the sharing an amplifier between two successive pipeline stages ,the converter is realized using just four amplifiers with a separate sample-and-hold block. It employs two key techniques : a high bandwidth low-power gain-boosting telescopic amplifiers technique and a low power low offset dynamic comparators technique. The ADC achieves a 8. 1 effective number of bits ,a maximum differential nonlinearity of a 0. 85 least significant bit (LSB) , and maximum integral nonlinearity of 2. 2LSB for a 0. 5MHz input at full sampling rate. It occupies 1. 24mm^2 ,which also includes a bandgap and a voltage reference circuit and dissipates only 59mW.

Key words : analog-to-digital converter ; low power ; OPAMP sharing technique ; gain-boosting technique
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1 Introduction

High-speed ,high-resolution A/ D conversion is important in a wide variety of commercial applications , such as data communication and storage. These applications often use complex modulation and detection schemes such as quadrature amplitude modulation (QAM) , which usually requires extensive digital signal processing at the receiver. Thus , the front end of such a receiver typically needs a high-speed A/ D converter (ADC) . Many of these applications make use of 10bit analog-to-digital converters (ADC's) sampling at around 40MHz[1] . And ,in most applications , the reduction of power consumption is one key design issue.

The ADC described in this paper has been designed to meet the 10bit 40Msample/ s requirements and also features a low power consumption. The power reduction is achieved by using power efficient pipeline architecture , sharing an amplifier between two successive stages in the pipelined ADC ,employing high bandwidth low-power gain-boosting telescopic amplifiers and low-power low-offset dynamic comparators ,as well as using a capacitor size scaling down scheme. The measured results are much better than those of Refs. [9～11] which concern state-of-art AD converters. The power efficiency of this work is excellent ,even in real world situations.

2 ADC architecture

In general ,pipelined ADCs have been proven to be power efficient architectures. In pipeline converters ,power consumption can be optimized by an

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appropriate selection of bits/stage[2] and capacitor scaling down the pipeline[3]. Furthermore, using the amplifier sharing technique to share an opamp between two consecutive stages in the pipeline causes a further significant power reduction in a pipelined ADC[4]. An attractive method of realizing a high-speed ADC is to use a pipeline architecture where each stage has a resolution of 1.5b[5]. This 1.5bits/stage architecture has two benefits. The first is to maximize the bandwidth of the SC (switched-capacitor) circuit. With such a resolution, the closed-loop gain equals 2, which allows for low load capacitance and a large feedback factor. As a result, a large interstage amplifier bandwidth can be achieved. The second benefit is that it allows for a large correction range for comparator offsets in the flash ADC, where only two comparators are required for every stage. Thus comparator offsets up to $\pm V_{ref}/4$ can be tolerated.

Consequently, a 1.5bits/stage pipeline with amplifier sharing topology is adopted for the converter. Figure 1 presents the architecture of the converter.

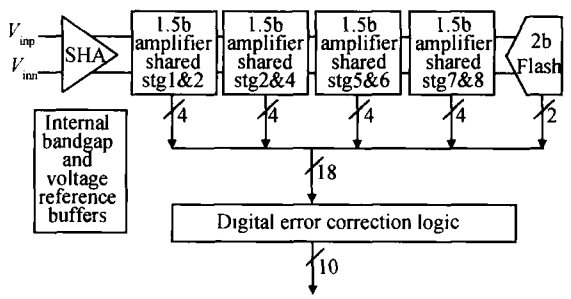

Fig. 1 Block diagram of the ADC

2.1 Sample and hold amplifier circuit

The implementation of the sample and hold amplifier (SHA) is shown in Fig. 2. The SHA is capable of dealing with high-frequency inputs with low distortion by using constant V_{GS} sampling switches, which use a bootstrapping circuit and are designed to observe device reliability considerations. The input voltage is sampled on capacitors C_{in} at the end of the sample phase ϕ_{1p}. During the hold phase ϕ_2, the charge from C_{in} is transferred to feedback capacitors C_f such that the output is

$$V_{out} = \frac{C_{in}}{C_f} V_{in} \quad (1)$$

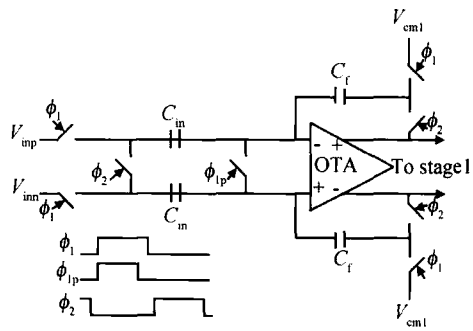

Fig. 2 SHA circuit

2.2 Amplifier sharing blocks

Each amplifier sharing block is made up of two consecutive stages sharing one amplifier and one clock generator. Each sharing block (actually equivalent to two conventional 1.5bits stages) provides four bits of digital output. The four bits from the four sharing blocks and the two bits from the flash are transferred to the digital error correction logic block and, in the end, provide ten bits of digital output.

The implementation of each sharing stage is shown in Fig. 3. Here, for simplicity, a single-ended configuration is shown, though the actual implementation is fully differential.

Amplifier sharing is based on the fact that, in switched-capacitor architecture, the amplifier is used for only one half of a clock cycle, which is during the amplification phase.

The operation of the sharing stage can be briefly described as follows. There are two switched-capacitor networks operating on opposite clock phases with the opamp alternating between them. During phase 1, $C_s(n)$ and $C_f(n)$ sample $V_{RES}(n-1)$. During phase 2, the residue $V_{RES}(n)$ is produced by $C_s(n)$, $C_f(n)$, and A1 operating under the control of the digital input D_{n-1}. This is sampled by $C_s(n+1)$ and $C_f(n+1)$ and is simultaneously processed by the decision circuit n to generate the digital signal D_n. During phase 1 of the next

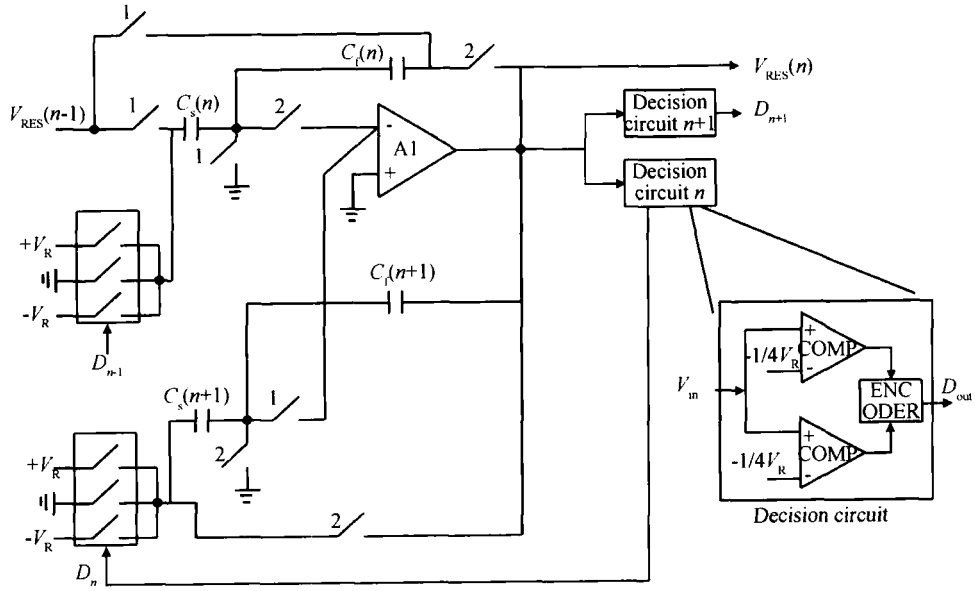

Fig. 3　Amplifier shared stage

clock interval , C_s (n + 1) , C_f (n + 1) ,and A1 combine to generate the analog residue V_{RES} (n + 1) under the control of D_n. This is processed by the decision circuit n + 1 to generate the digital output D_{n+1}.

Amplifier sharing introduces two possible drawbacks[4]. Firstly , the additional switches that are used to implement amplifier sharing introduce series resistances ,which will affect the settling behavior of the stage. The switch resistances can be reduced by using large switches at the expense of a potential increase in offsets due to charge feed through. Secondly ,the nonzero input voltage of the amplifier is never resetted. Thus ,every input sample is affected by the finite-gain error components from the previous sample. However ,increasing the gain of the opamp could make the finite gain error negligible.

Also ,in order to reduce power consumption , the scaling technique for the opamps and capacitors is applied. The value of the sampling capacitor of the SHA , C_s , should be obtained from noise and matching constraints. In this design C_s is limited by matching rather than noise.

3　Circuit techniques

There are mainly two key techniques for the ADC , i. e. low-power high-bandwidth gain-boosting opamp technique and low-power low-offset dynamic comparator technique.

3. 1　Low-power high-bandwidth gain-boosting opamp

The amplifiers adopted in the SHA and other ADC stages are based on a fully differential gain-boosting telescopic architecture (shown in Fig. 4) to get a high open-loop gain and excellent bandwidth with less power consumption ,at the cost of a reduced signal swing range. In this implementation , the telescopic amplifier also exploits a wide-swing gain-boosting technique in order to alleviate the problem of the reduced signal swing range. The gain-boosting technique improves the cascoding effect of a single MOS transistor by using local negative feedback.

Assume ,for simplicity ,that the two additional gain-boosting amplifiers have the same DC gain A_{add} ,and the upper part of the circuit has the same output impedance as the lower part. Then the output impedance of the circuit is increased by the gain of the additional gain-stage A_{add} :

$$R_{out} = \frac{1}{2}((g_{m3} r_{o3} (A_{add} + 1) + 1) r_{o1} + r_{o3}) \quad (2)$$

where g_{m3} is the transconductance of transistor

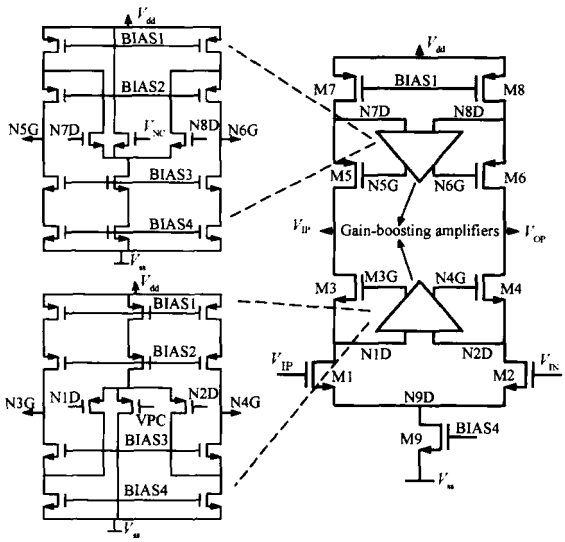

Fig. 4 Low-power high-bandwidth gain-boosting opamp

$M3$, r_{o1} and r_{o3} are the output resistance of transistors M1 and M3, respectively. Hence, the total DC-gain becomes

$$A_{o,tot} = \frac{1}{2} g_{m1} r_{o1} (g_{m3} r_{o3} (A_{add} + 1) + 1) \quad (3)$$

where g_{m1} is the transconductance of the transistor M1.

From Eq. (2), it can be seen that the gain-enhancement technique increases the output impedance by a factor approximately equal to $A_{add} + 1$. But the gain of the additional stage, A_{add} decreases for frequencies above the - 3dB bandwidth of the gain-boosting amplifier with a slope of - 20dB/decade. For frequencies above unity-gain bandwidth of the gain-boosting amplifier, A_{add} is less than one, and the normal output impedance of a cascade stage without gain-enhancement remains. This could introduce a doublet in the plot of the total output impedance.

Non-complete doublet cancellation can seriously degrade the settling behaviour of an opamp. In order to overcome this drawback, the unity-gain frequency of the added gain boosting circuit should be higher than the - 3dB bandwidth of the circuit, which is the closed-loop bandwidth of an SC circuit which uses the main amplifier, and must be lower than the second-pole frequency of the main amplifier for reasons concerning stability. This way, the circuit could have a single-pole settling behavior. The gain-bandwidth product (GBW) could be expressed as

$$\mathrm{GBW} = \frac{g_m}{C_{load}} \quad (4)$$

where g_m is the input transconductance and C_{load} is the load capacitor connected at the output of the amplifier. The amplifier also uses a switched-capacitor common-mode feedback circuit[6], which is not shown in Fig. 4.

Figure 5 shows the simulated gain and phase of the gain-boosting opamp used in SHA. The main simulated characteristics of the opamp are summarized in Table 1.

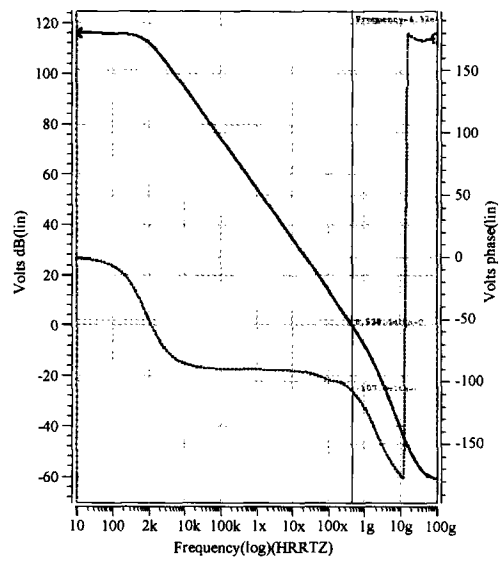

Fig. 5 Simulated gain and phase of the gain-boosting opamp

Table 1 Main characteristics of the opamp

Characteristics	Value
DC gain	118dB
Unity-gain freqency	432MHz
Load capacitor	5pF
Phase margin	73°
Power consume	18mW
Output swing	2.1V
Supply voltage	3.0V

3.2 Dynamic comparator

As previously discussed, the 1.5bits/stage architecture relaxes the requirements for comparator

offsets. This allows the use of dynamic latch-type comparators without any preamplifier to cancel the offset voltage. In order to reduce power consumption ,a low offset dynamic comparator ,as shown in Fig. 6 ,is adopted in the ADC[7].

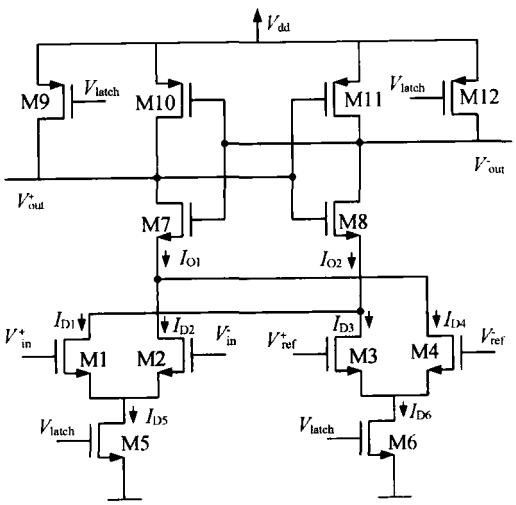

Fig. 6　Dynamic comparator

The operation of the comparator can be briefly described as follows. When the latch signal V_{latch} is at 0V the comparator is inactive , transistors M5 and M6 are switched off and there is no current path between the supply voltages. The transistors M9 and M12 reset the outputs to V_{dd}. The transistors M7 and M8 of the latch conduct and pull the drains of the transistors M1～M4 to V_{dd} ,while the drain voltage of M5 and M6 are dependent on the comparator input voltages. When V_{latch} is raised to V_{dd} ,the comparator is active ,the outputs are disconnected from the supply V_{dd} , M5 and M6 turn on ,and M1～M4 compare V^+_{in} - V^-_{in} with V^+_{ref} - V^-_{ref}.

The threshold voltage of the comparator is determined by the current division in the differential pairs and between the cross-coupled branches. The transistors M1～M4 follow the large signal current equations ($W_1 = W_2$, $W_3 = W_4$) :

$$I_{D1} - I_{D2} = \beta_1 V_{in} \sqrt{\frac{2I_{D5}}{\beta_1} - V_{in}^2} \qquad (5)$$

$$I_{D4} - I_{D3} = \beta_3 V_{ref} \sqrt{\frac{2I_{D6}}{\beta_3} - V_{ref}^2} \qquad (6)$$

where $\beta_i = \frac{1}{2}\mu C_{ox}\frac{W_i}{L}$, $V_{in} = V^+_{in} - V^-_{in}$ and $V_{ref} = V^+_{ref} - V^-_{ref}$.

The comparator changes its stage when the currents $I_{O1} = I_{D1} + I_{D3}$ and $I_{O2} = I_{D2} + I_{D4}$ of both the output branches are equal. Assuming the relation of the source-coupled pair bias currents to be $I_{D5} = dI_{D6}$,and by marking the threshold point with a parameter e such that $V_{in} = eV_{ref}$, the resulting condition is thus

$$2de^2 I_{D6}\frac{W_1}{L} - \mu C_{ox} e^4 V_{ref}^2\left(\frac{W_1}{L}\right)^2 = 2I_{D6}\frac{W_3}{L} - \mu C_{ox} V_{ref}^2\left(\frac{W_3}{L}\right)^2 \qquad (7)$$

The parameters d and e are chosen according to the desired trip point of the comparator. The total offset voltage of the comparator consists of the sum of the offsets of both source-coupled pairs. The offset of one differential pair has a well-known dependency on the mismatch of the threshold voltage V_T , load resistance R_L and transistor dimensions $\Delta\beta$ and their corresponding average values V_T , R_L ,and β.

$$V_{OS} = \Delta V_T + \frac{V_{gs} - V_T}{2} \times \left(\frac{\Delta R_L}{R_L} + \frac{\Delta\beta}{\beta}\right) \qquad (8)$$

The offset voltage in this case is dominated by the mismatch of the transistor dimensions $\Delta\beta$, while $V_{gs} - V_T$ is set by the tail currents I_{D5} and I_{D6}. Simulation results show that the offset of this comparator is within 5mV , with a supply voltage range from 2. 6～3. 6V ,a process range from slow to fast ,and temperatures from low to high (- 40～125 °C) , which is much lower than the traditional dynamic comparators in Ref. [9].

3. 3　Other components

The ADC also includes an on-chip precision bandgap reference voltage generator and buffer amplifiers to generate positive and negative reference voltage and the common-level voltage for opamps. The clock generation of the ADC is implemented with five local clock generators driven by a single master clock to coincide between stages in order to avoid any loss of clock period due to skews related

to the layout.

4 Experimental results

The ADC has been fabricated in a 0.25μm single-poly five-metal DGO CMOS process with an MiM capacitor. The die photograph is shown in Fig. 7. The upper side shows the bandgap and the reference buffer opamps, while the center side shows the SHA and the four opamp sharing blocks, and the bottom shows the digital error correction logic block. The total active area is about 1.24mm^2, with a core area, excluding the bandgap and buffer amplifiers, of about 1mm^2. The measured output fast Fourier transform (FFT) spectrum with a 0.5MHz input frequency at 40MS/s is shown in Fig. 8. The measured nonlinearity of the ADC is shown in Fig. 9. The summary of the ADC's overall performance is given in Table 2.

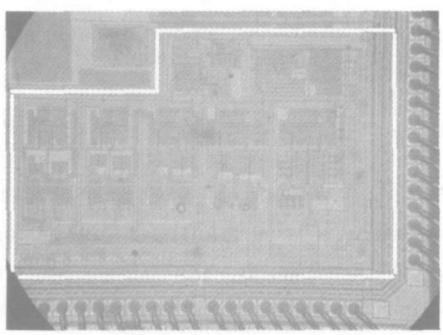

Fig. 7 Die photograph

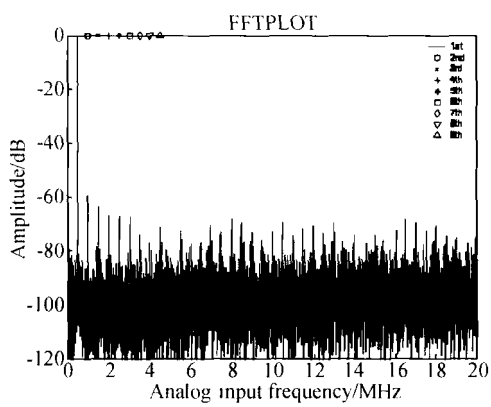

Fig. 8 Measured FFT spectrum

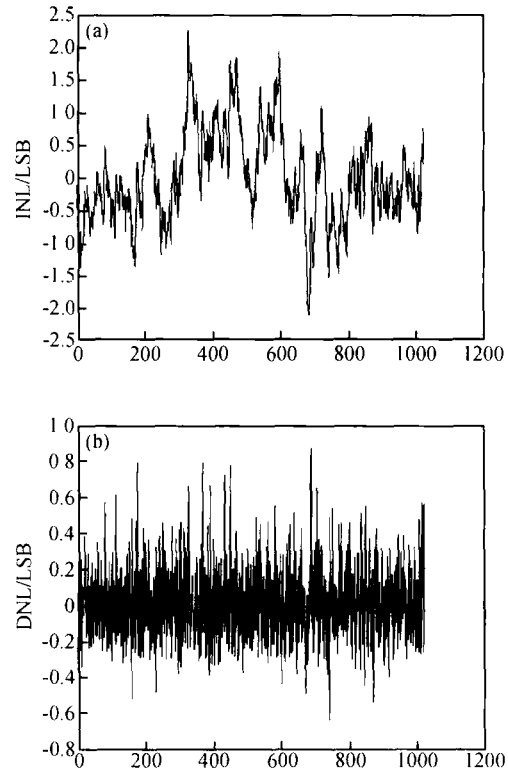

Fig. 9 Measured nonlinearity 40Ms/s, f_{in} = 500kHz

Table 2 Performance summary

Resolution	10bit
Conversion rate	40MS/s
Process	0.25μm single-poly five-metal DGO CMOS process with MiM capacitor
Power supply	3.0V
Total power	59mW@3.0V
SNR *	51dB
SFDR *	59dB
THD *	57dB
ENOB *	8.1bit
Peak INL *	2.2LSB
Peak DNL *	0.85LSB

* Measured at f_{in} = 0.5MHz, f_{clk} = 40MHz

5 Conclusion

A 10bit 40MS/s ADC has been described. By sharing an amplifier between two successive pipeline stages, significant power reduction has been achieved. The converter also employs high bandwidth low-power gain-boosting telescopic amplifiers and low power low offset dynamic comparators in order to save power and provide high performance. The ADC, which occupies 1.24mm^2 and

consumes only 59mW (including a bandgap and a reference circuit) at 40MS/ s ,has been implemented in a 0. 25μm DGO CMOS process technology.

When quantifying the power efficiency of the A/ D converter implementations ,the resolution and sample rate should also be considered. The most widely accepted measure of the effectiveness of design is the energy per conversion step[8] ,defined as

$$E_{\mathrm{conv}} = \frac{P_{\mathrm{D}}}{2^{N} f_{\mathrm{s}}} \tag{9}$$

where P_{D} is the power dissipation , N is the resolution ,and f_{s} is the sample rate. Using the above equation ,power efficiency comparison with those reported in Refs. [1 ,3～5 ,9～12] is given in Table 3.

Table 3　Power efficiency comparison

	Resolution / bit	Sample rate / (Msample ·s^{-1})	Power dissipation / mW	Energy per conversion step / pJ
This work	10	40	59	1. 4
Ref. [1]	10	40	65	1. 6
Ref. [3]	13	5	166	4. 1
Ref. [4]	8	52	250	18. 7
Ref. [5]	10	20	240	11. 7
Ref. [9]	10	20	65	3. 2
Ref. [10]	8	200	177	3. 4
Ref. [11]	8	125	71	2. 2
Ref. [12]	12	20	254	3. 1

As can be seen from the table ,the power efficiency of this work is much higher than those of Refs. [9～11] which are published state-of the art performances in domestic journals. Although the power efficiency of Ref. [1] is comparable with this work ,it was implemented in a BiCMOS process , which is more suitable for high performance mixed-signal circuits than a CMOS process.

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一个 59mW 10 位 40MHz 流水线 A/D 转换器*

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摘要: 设计了一个工作在 3.0V 的 10 位 40MHz 流水线 A/D 转换器,采用了时分复用运算放大器,低功耗的增益自举 telescopic 运放,低功耗动态比较器,器件尺寸逐级减小优化功耗. 在 40MHz 的采样时钟,0.5MHz 的输入信号的情况下测试,可获得 8.1 位有效精度,最大积分非线性为 2.2LSB,最大微分非线性为 0.85LSB,电路用 0.25μm CMOS 工艺实现,面积为 1.24mm^2,功耗仅为 59mW,其中同时包括为 A/D 转换器提供基准电压和电流的一个带隙基准源和缓冲电路.

关键词: 模数转换器; 低功耗; 共享运算放大器技术

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