A High Phase Accuracy and Low Amplitude Mismatch Quadrature LO Driver *

Han Shuguang[1] , Chi Baoyong[2] , and Wang Zhihua[2]

(1 *Department of Electronic Engineering , Tsinghua University , Beijing* 100084 , *China*)
(2 *Institute of Microelectronics , Tsinghua University , Beijing* 100084 , *China*)

Abstract : A 1. 1～1. 2GHz CMOS high phase accuracy ,low amplitude mismatch quadrature LO driver is presented , which consists of a high frequency amplifier ,an integrated poly phase filter ,and an I/ Q phase and magnitude calibration circuit (PMCC) . The proposed PMCC uses a feed-forward calibration technique. It improves the phase accuracy and reduces the amplitude mismatch with low power consumption. Simulation results show that phase error with PMCC is reduced to about one half and the amplitude mismatch is reduced to about one tenth ,when compared to the LO driver without PMCC. Moreover ,the calibration circuit also functions as a buffer to drive mixers ,thus no additional buffer is needed in this design. The LO driver is implemented in a TSMC 0. 25μm CMOS process. Experimental results show that the LO driver achieves high quadrature accuracy (< 2°) and low amplitude mismatch (< 0. 1 %) . It has about 5. 25dB gain and dissipates 6mA from the 2. 5V power supply. The size of the die area is only 1. 0mm ×1. 0mm.

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1 Introduction

Many modern transceivers , such as those based on low-IF or zero-IF architecture ,require an in-phase and quadrature (I/ Q) LO signal for image rejection[1] . In these transceiver systems , a major challenge is the generation of high quadrature accuracy and low amplitude mismatch I/ Q LO signals. The I/ Q phase and amplitude error directly effect the performance of the image cancellation and negative frequency rejection of the demodulation. Thus ,to the circuit designers ,there is an unprecedented interest to study the generation and calibration techniques of quadrature LO signals.

At present ,there are three popular methods to generate quadrature signals[2～5] : combination of a VCO and a poly phase-filter ,a VCO at double frequency followed by a divide-by-2 master-slave flip-flop ,and the use of a quadrature VCO. The second method needs a VCO designed at double frequency and the third method offers bad phase accuracy; therefore ,in this design ,the first method is adopted. However ,it is well known that this method is subjected to the component mismatch and parasitic effect. In order to improve phase accuracy , several

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Han Shuguang male ,PhD candidate. His work focuses on analog circuit design and RF front-end circuit design.
Chi Baoyong male ,PhD. His work focuses on the analog circuit design and RF front-end circuit design.
Wang Zhihua male ,professor. His research areas include analog/ mixed-signal/ RF CMOS integrated circuit technologies ,ASIC design for communication systems ,algorithm exploration ,and ASIC design of digital audio/ video signal processing systems ,design of integrated electronic systems and SOC.

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digital methods for compensating the I/Q imbalance using base-band DSP techniques have been demonstrated[6]. An analog approach is desirable because its power dissipation is lower than that of the digital methods[7].

In this paper, a fully integrated quadrature LO driver is presented with high phase accuracy and low amplitude mismatch. In order to improve the phase accuracy of quadrature LO signals, an I/Q phase and magnitude calibration circuit (PMCC) is proposed. In contrast to the traditional feedback calibration methods[6,7], PMCC uses a feed-forward phase and amplitude calibration techniques. In a traditional feedback calibration mechanism, high accuracy quadrature LO signals can be achieved, but there are two unsolved problems that degrade transceiver performances: system rate has to slow down for the large feedback circuit circle, and the transceiver will suffer from instability issues. Moreover, due to the D/A and DSP in feedback calibration systems, more power has to dissipate in feedback calibration circuits. In our proposed PMCC, due to the feed-forward technique used, the feedback technique problems will not show and low power can be achieved.

2 Circuit description and analysis

The architecture of the quadrature LO driver is shown in Fig. 1. Firstly, the differential LO signals VIN + and VIN - are amplified by the high frequency amplifier, which is followed by the second-order poly phase network to produce quadrature signals (VI +, VQ +, VI -, VQ -). The quadrature signals are sent to the proposed PMCC to improve phase accuracy and reduce amplitude mismatch of the adjacent branches. They make the output LO signals (VO1, VO2, VO3, and VO4) show the better quadrature accuracy and low amplitude mismatch.

2.1 High frequency amplifier

Figure 2 shows the schematic diagram of the high frequency amplifier. MA1 and MA2 are the differential pairs to amplify the input signals (the amplitude is - 3dBm). L1 and L2 are the spiral inductors that resonate with parasitic capacitance at 1.15GHz. MB1 ~ MB4 combine the output buffer to drive the first stage of the poly phase filter. Simulation results show that the high frequency amplifier has a gain of about 15dB loaded with the poly phase network.

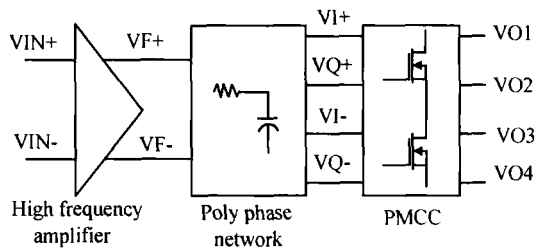

Fig. 1 Architecture of quadrature LO driver

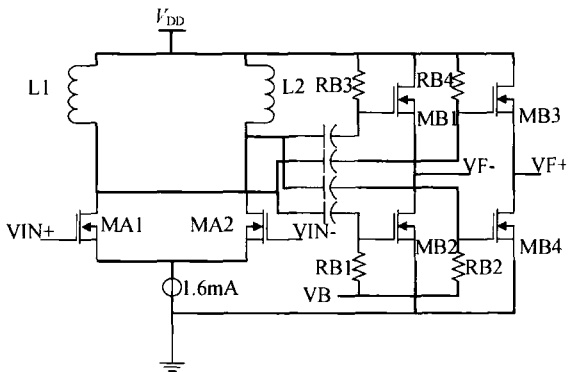

Fig. 2 Schematic of high frequency amplifier

2.2 Second-order poly phase network

Figure 3 is the circuit to generate balanced quadrature signals from differential input signals. In a poly phase network, in order to lower total loss, the impedance of each successive stage is made lager so that it lightly loads the previous stage[3]. Therefore, in this design, the high pole (1.2GHz) consisting of $R_{11} \sim R_{14}$ and $C_{11} \sim C_{14}$ is placed in the first stage, and the low pole (1.1GHz), consisting of $R_{21} \sim R_{24}$ and $C_{21} \sim C_{24}$, is placed in the second stage. Simulation shows the cascaded loss is about 8.5dB. The poly phase network is extremely sensitive to variations in component values; component mismatch will induce I/Q phase error in the poly phase network[3,7]. Thus

phase calibration is necessary with the outputs of the poly phase network.

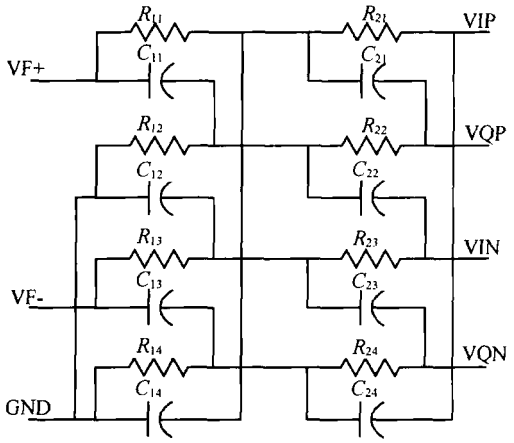

Fig. 3　Schematic of second-order poly phase network

2.3　Proposed I/Q phase and magnitude calibration circuit

Figure 4 shows the core schematic diagram of the proposed PMCC. The same size transistors, M1, M3, M5, and M7 act as source followers with unit gain. M2, M4, M6, and M8 act as common-source amplifiers with the same size and render the gain $\beta = -g_{m2}/g_{m1}$ ($g_{m1} = g_{m3} = g_{m5} = g_{m7}$, $g_{m2} = g_{m4} = g_{m6} = g_{m8}$). According to the superposition principle, VO1 = VIN - β · VIP and VO2 = VIP - β · VIN.

The differential branches VIP and VIN (or VQP and VQN) produced by the poly phase network should be differential theoretically, but their phase difference may not be 180° due to component mismatch. Assuming VIN = $(A + \Delta A)\sin(\omega t + \phi)$ and VIP = $A\sin(\omega t + \pi)$, where ΔA and ϕ denote amplitude mismatch and phase error, respectively, then VO1 and VO2 can be written as

$$\begin{cases} \mathrm{VO1} = (A + \Delta A)\sin(\omega t + \phi) + \beta A\sin(\omega t) \\ \mathrm{VO2} = A\sin(\omega t + \pi) + \beta(A + \Delta A)\sin(\omega t + \phi + \pi) \end{cases} \tag{1}$$

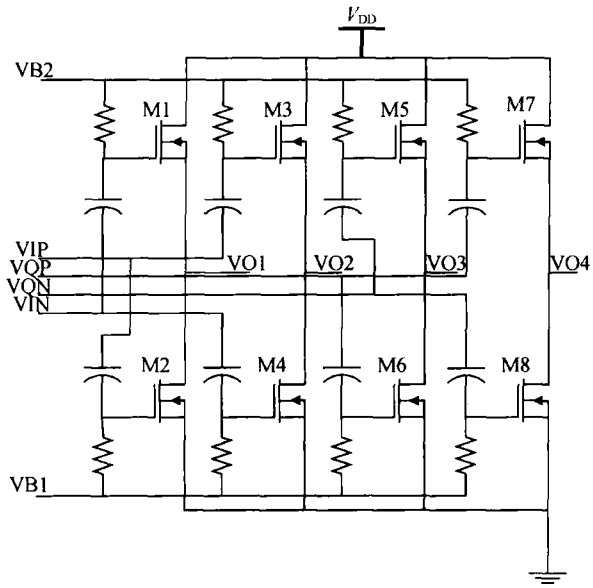

Fig. 4　Core schematic of phase and amplitude calibration circuit

Expanding and simplifying the two equations, VO1 and VO2 can be written as

$$\begin{cases} \mathrm{VO1} = (\beta A + A + \Delta A)\cos(\phi/2)\sin(\omega t + \phi/2) + \\ \qquad (A + \Delta A - \beta A)\sin(\phi/2)\cos(\omega t + \phi/2) \\ \mathrm{VO2} = (\beta A + A + \beta\Delta A)\cos(\phi/2)\sin(\omega t + \phi/2 + \pi) + \\ \qquad (\beta A + \beta\Delta A - A)\sin(\phi/2)\cos(\omega t + \phi/2 + \pi) \end{cases} \tag{2}$$

If $\beta = 1$ and $\Delta A = 0$, VO1 and VO2 can be simplified to $2A\cos(\phi/2)\sin(\omega t + \phi/2)$ and $2A\cos(\phi/2)\sin(\omega t + \phi/2 + \pi)$, respectively. Generally, $\phi \leq 6°$, so $\cos(\phi/2) \approx 1$. In this case, the phase error is reduced to one half and amplitude is doubled.

The amplitude difference in differential branches is analyzed as follows: the amplitude of VO1 and VO2 can be written as

$$\begin{cases} |\mathrm{VO1}| = \sqrt{(\beta A)^2 + (A + \Delta A)^2 + 2\beta A(A + \Delta A)\cos\phi} \\ |\mathrm{VO2}| = \sqrt{(\beta(A + \Delta A))^2 + A^2 + 2\beta A(A + \Delta A)\cos\phi} \end{cases} \tag{3}$$

Defining $\nabla = (|\mathrm{VO1}| - |\mathrm{VO2}|)/|\mathrm{VO2}|$, ∇ denoting the relative amplitude difference with calibration by PMCC, ∇ can be written as

$$\nabla = \frac{\sqrt{\beta^2 + (1 + \frac{\Delta A}{A})^2 + 2\beta(1 + \frac{\Delta A}{A})\cos\phi} - \sqrt{(\beta(1 + \frac{\Delta A}{A}))^2 + 1 + 2\beta(1 + \frac{\Delta A}{A})\cos\phi}}{\sqrt{(\beta(1 + \frac{\Delta A}{A}))^2 + 1 + 2\beta(1 + \frac{\Delta A}{A})\cos\phi}} \tag{4}$$

Figure 5 shows the simulation results of ∇ when $\phi = 5°$. It shows that the relative amplitude difference ∇ is much lower than the original relative amplitude difference $\frac{\Delta A}{A}$. When gain β increases, ∇ will increase. In this design, the parameters of PMCC are regulated to control the gain of the common-source amplifier within the range $1 \leq \beta \leq 2$.

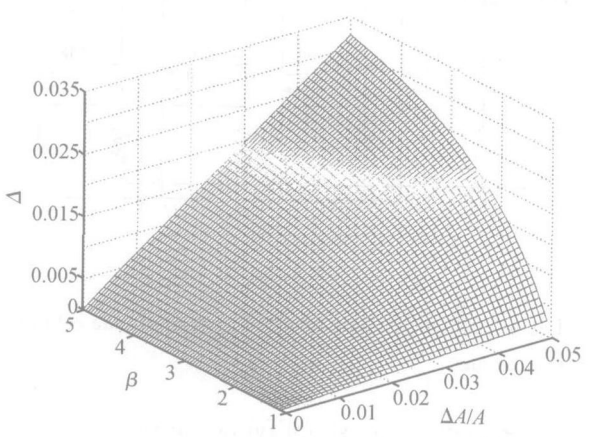

Fig. 5 Simulated relative amplitude difference ∇ with $\phi = 5°$

Defining the additional phase error as Φ, according to the expressions of VO1 and VO2, Φ can be written as

$$\Phi = \tan^{-1}\left(\frac{(\beta + 1 + \frac{\Delta A}{A})\cos(\phi/2)}{\sqrt{\beta + (1+\frac{\Delta A}{A})^2 + 2\beta(1+\frac{\Delta A}{A})\cos\phi}}\right) - \tan^{-1}\left(\frac{(\beta + 1 + \beta\frac{\Delta A}{A})\cos(\phi/2)}{\sqrt{(\beta(1+\frac{\Delta A}{A}))^2 + 1 + 2\beta(1+\frac{\Delta A}{A})\cos\phi}}\right) \quad (5)$$

Figure 6 shows the simulation results of Φ with $\phi = 5°$. It shows that the additional phase error can be negligible.

From the above analysis and simulation, the following conclusions for the PMCC can be drawn.

(1) The amplitude mismatch of differential branches is about one tenth of the original value;

(2) The phase error is about half of the original value;

(3) The induced phase error from PMCC is very small. In the expression of Φ, if $\frac{\Delta A}{A} = 5\%$, $\phi = 5°$ and $\beta = 2$, additional phase error $\Phi \approx 0$; if $\Delta A = 0$, phase difference is absolutely 180° between the differential branches;

(4) In the four branches, if any of the adjacent branch pairs are quadrature after PMCC, then all adjacent branches will be quadrature through the PMCC.

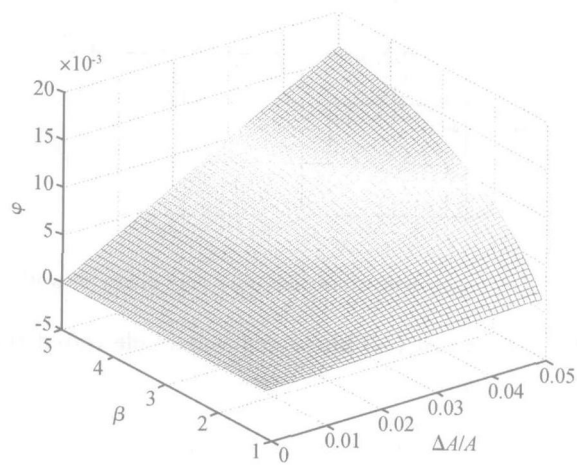

Fig. 6 Simulated additional phase error Φ with $\phi = 5°$

3 Results

A worst case simulation is performed to verify this design. In the worst case analysis, let the component value increase 5% in one of symmetric branches (R_{11}, C_{14}, R_{21} and C_{24} of Fig. 3) and in the others (R_{12}, C_{12}, R_{22} and C_{22} of Fig. 3) decrease 5% (the component values of other symmetric branches change the same as above). Figures 7 and 8 show the amplitude mismatch and phase error curves, respectively. As can be seen, with PMCC, the maximum amplitude difference decrease from 0.217 to 0.0219dB and the maximum phase error decreases from 6.26° to 2.6°.

This design has been implemented in a TSMC 0.25μm CMOS process. The die photograph is shown in Fig. 9. The chip area is about 1mm ×1mm. Figure 10 shows the measured gain curves using Agilent 8753ES network analyzers. The measured maximum gain is about 5.25dB at 1.1267GHz. The measured two adjacent branches output signals are shown in Fig. 11. An overview of the measured circuit performance is summarized in Table 1.

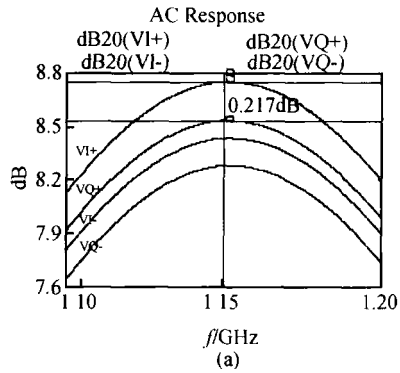

Fig. 7　Simulated amplitude difference without (a) and with PMCC (b) by Spectra RF

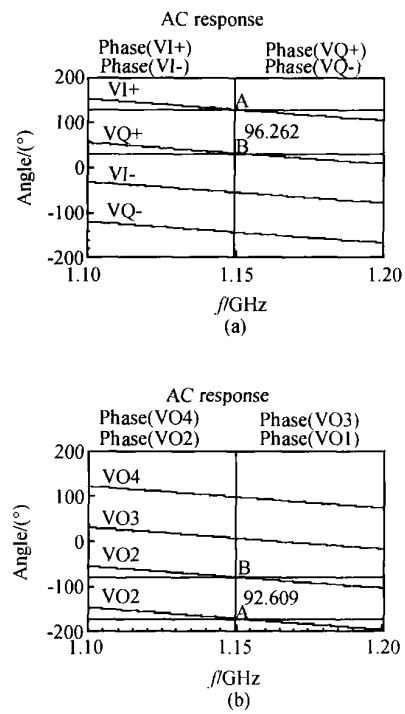

Fig. 8　Simulated phase error without (a) and with PMCC (b) with by Spectra RF

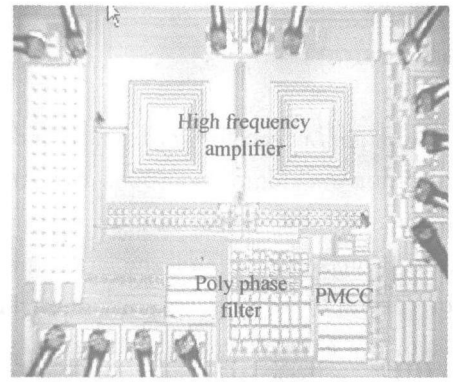

Fig. 9　Die photograph of LO Driver

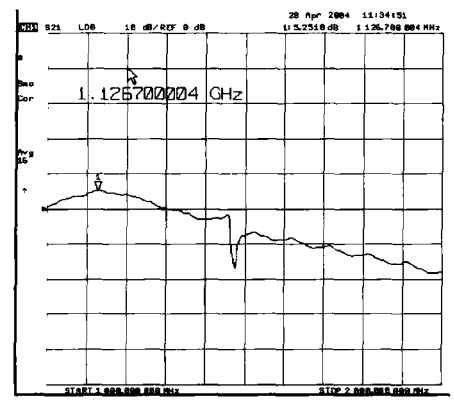

Fig. 10　Measured gain curves

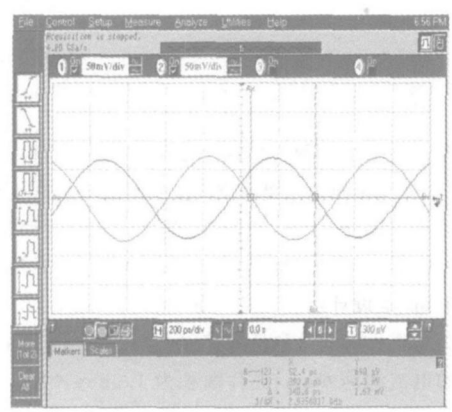

Fig. 11　Measured output signals in two adjacent branches

Table 1　Measured circuit performances

Power supply	2.5V
Frequency range	1.1～1.2GHz
Power consumption	15mW
Power gain	5.25dB @1.126GHz
Phase error	<2°
Amplitude error	<0.1%
Chip size	1mm ×1mm
Technology	0.25μm CMOS

4 Conclusion

In this paper, a feed-forward phase and amplitude calibration technique is proposed, with a circuit implemented and tested. The circuit is used to calibrate the phase error and the amplitude mismatch of the input signals without degrading the system stability and system rate. It has been used in the quadrature LO driver to achieve a higher phase accuracy and lower amplitude mismatch. The simulation and measurement results show that the proposed PMCC could reduce the phase error and the amplitude mismatch of adjacent branches. In addition, the output buffer has been left out for the strong load capability of the PMCC. This design has been used in a DAB receiver. The lower power characteristics of this design open prosperous perspectives towards the integration of this circuit in low power RF transceiver systems.

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一种相位准确度高幅值失配度低的正交 LO 驱动电路*

韩书光[1] 池保勇[2] 王志华[2]

(1 清华大学电子工程系, 100084 北京)

(2 清华大学微电子研究所, 100084 北京)

摘要: 提出了一种工作在 1.1～1.2GHz 的相位准确度高、幅值失配度低的正交 LO 驱动电路. 它主要由高频放大器、二阶的无源多项滤波器、相位和幅度校准电路(PMCC)组成. PMCC 是一种利用前馈技术实现的低功耗电路, 大大提高了正交信号的正交性, 降低了相邻支路信号的幅值误差. 仿真结果表明, 经过 PMCC 校准后, 输出正交信号的相位误差可以降低大约一半, 而幅度误差可以降低到原来的十分之一. PMCC 可直接驱动混频器, 无需额外的驱动电路. 本设计已经用 TSMC 0.25μm CMOS 工艺实现并进行了验证. 测试结果表明本文提出的校准电路能够获得高正交性(<2°)和低幅值误差(<0.1%)的正交信号, 测试的最大功率增益为 5.25dB, 在 2.5V 的电源电压下, 消耗的电流约为 6mA, 芯片面积为 1.0mm×1.0mm.

关键词: CMOS; 正交; 多项滤波器; 相位校准; 幅度校准

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韩书光 男, 博士研究生, 研究方向为模拟电路及射频前端电路设计.

池保勇 男, 博士, 研究方向为模拟电路及射频前端电路设计.

王志华 男, 教授, 研究方向包括 CMOS 模拟、数模混合及射频集成电路技术, 通信专用集成电路技术, 数字音频及视频信号处理及专用集成电路, 电子系统集成及片上系统.

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