A Novel Multi-Functional Leakage Current Protector IC Design *

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Abstract: A novel type of leakage current protector chip, implemented in the mixed-signal 0.6μm CMOS process, is presented. This chip has the advantages of low power dissipation (10mW), accurate protection control based on digital response delay time and integration of multi-functions such as leakage current/over-voltage/over-load detection and protection, auto switch-on and so forth. Additionally, the chip is programmable to suit different three-level protection applications with a high anti-interference ability.

Key words: leakage current protector; IC design; programmable IC
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1 Introduction

While electrical equipment is so very popular in our working and daily life, it is necessary both to avoid getting electrical shocks and to enhance safety of usage. Therefore, leakage current protectors, which are electric devices that cut off power supply automatically in order to protect human bodies and equipment from damages are widely applied.

Most of the leakage current protectors today are made of bipolar IC and need a lot of peripheral discrete devices. In response to the disadvantages caused by bipolar IC, a novel type of specialized leakage current protector IC chip is presented in this paper. It is implemented in a mixed-signal 0.6μm CMOS technology and has the advantages of low power consumption (10mW), high reliability and integration of multi-function suitable for different three-level protection (general-protection, mid-protection and in-door protection) areas.

2 Outline of protectors

The international electro-technical commission (IEC) standard and China design standard of electrical equipment in civil building JTJ/F-6-92 specify the standards of leakage current protection in detail[1,2].

The control part of leakage current protectors is designed to fit the current-mode. The protector detects the leakage current through a magnetic ring of the zero-order current mutual inductor. Magnetic flux, as caused by the leakage current, will be generated inside the magnetic ring of the zero-order current mutual inductor. The secondary coil transfers the inductive voltage generated by the magnetic flux to the controller in the chip, which determines the state of the switch (on or off) according to the intensity and duration of the leakage cur-

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rent ,as illustrated in Fig. 1.

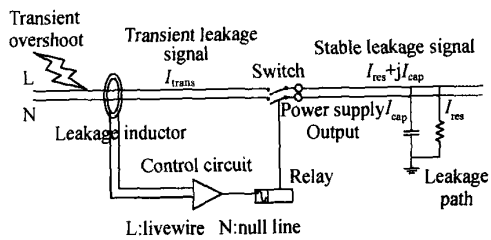

Fig. 1 Working principle of the current-mode leakage protector

Up to now ,traditional application circuits used external resistors and capacitors to control the response time[3,4]. The relationship between the intensity of the leakage signal and the response time of the protector is a "reverse delay" mode ,shown as the solid line in Fig. 2.

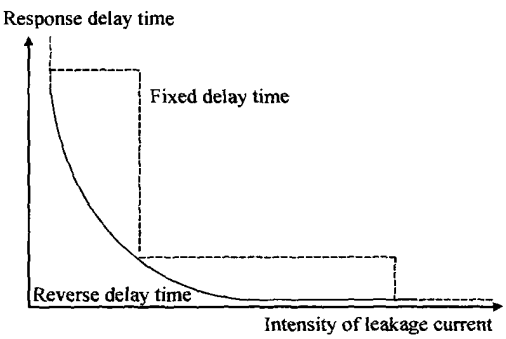

Fig. 2 "Reverse response delay time" and "Fixed response delay time"

The most popular leakage current protector chip ,M54133FP/ GP ,which belongs to Mitsubishi Corp is such a type[5]. Barring the advantage of two active low filters inside through which the negative effect from the high frequency noise and high-order harmonics is avoided, the chip has a high static power consumption at about 200mW and needs more than 10 peripheral discrete resistors and capacitors to achieve the reverse delay time as shown in Fig. 2. This reduces the precision and reliability of the protectors.

3 Novel design of the chip

According to what we have analyzed above, the novel type design of the leakage current protector chip includes the following advanced nature:

(1) The "fixed response time" concept realized by the internal digital circuit is adopted and the traditional "reverse time delay" approach by using external resistors and capacitors is abandoned.

As we well know ,the properties of the peripheral R/ C components are so discrete that the control precision of the delay time is usually low, which will easily cause mistake actions among the three level applications if the gaps among their response curves are not wide enough.

Since the internal integrated digital timer is used ,the novel chip is able to set the response time as "fixed delay" mode ,whose relationship between the intensity of the leakage signal and the response time is shown as the dotted line in Fig. 2. No discrete R/ C is necessary ,therefore not only the self-control precision but also the matching precision among different protection levels is greatly improved because their response curves never cross in any case.

(2) Multi-function integration is implemented in this chip. In addition to the main leakage current protection function ,the functions of over-voltage/ over-load detection and protection ,auto switch-on and so on are all integrated into this chip.

(3) There are two programmable pins in this chip to determine at which protection level the chip works (because different application levels demand different protection reactions). It provides convenience to the customers ,who only need to set the two input pins to "0" or "1" ,and keeps the number and parameters of the periphery components unchanged.

(4) This chip reduces power dissipation dramatically with the advantages of CMOS ICs ,which is only about 10mW instead of the several hundred milli-watts needed by the products in the market

now.

(5) A checking mechanism for the input leakage signal is introduced into this chip, which effectively reduced the protector's mistake actions against an interferential signal, such as a lightening strikes. Thus, the stability of the chip in electromagnetic circumstances is greatly enhanced and the external filter in traditional application circuit, which increases the integration density, is no longer needed.

In a word, the novel leakage current protector can be regarded as a multi-functional, programmable and low power consumption protector.

4 Architecture and specifics of the chip[6~9]

This chip consists of two main functional parts: over-voltage/over-load protection and leakage current protection. The function block diagram is shown in Fig. 3.

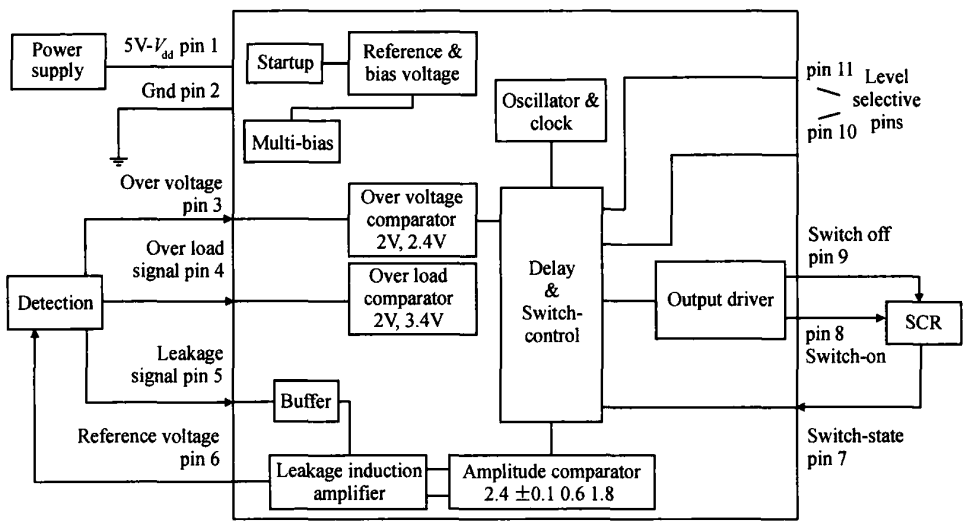

Fig. 3 Function block diagram

When an over-voltage/over-load signal occurs, the corresponding comparator outputs a pulse to the next block, named "delay & switch control".

When a leakage current signal occurs, it is first amplified by the leakage induction amplifier and then enables the amplitude comparator output a pulse to the "delay & switch control" block.

The delay & switch control block in Fig. 3 is a digital circuit shown in Fig. 4. In this block a pulse trigger signal is sent to a finite states machine (FSM) only if a leakage signal, an over-voltage signal or an over-load signal have passed the judgment of continuity and durability (so the transient noise signals and short abnormal leakage (harmless) etc. are filtrated). According to different situations, the output of FSM gives different enable signals in the output wave generator, which forms suitable pulse signals in the special duty cycle and frequency to control the switch on and off.

Pin 10 and pin 11 are designed to be suitable for different levels of protection: general-protection, mid-protection, and in-door protection, which are presented in Table 1.

Table 1

State name	Pin 10/11 value	Levels
HH11	00	In-door protection
HH12	01	Mid-protection
HH13	10	General-protection Ⅰ
HH14	11	General-protection Ⅱ

The mixed-signal design is simulated with the Cadence and Synopsys tools. The power dissipation

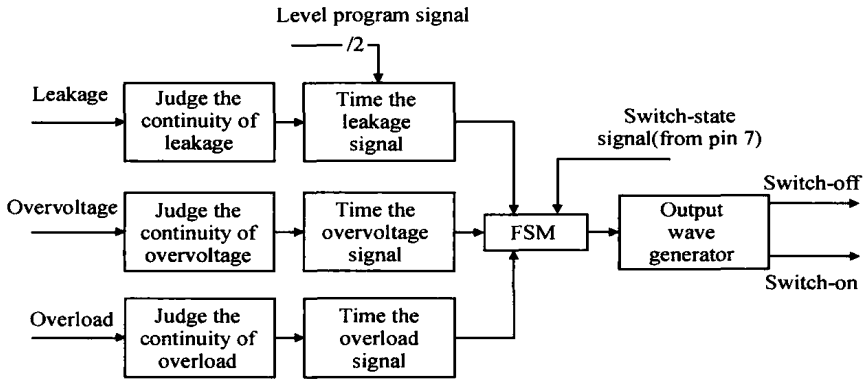

Fig. 4 Delay & switch control block

of the whole circuit is about 10mW under 5V supply, which benefits from the low bias current in the analog blocks and the low frequency of a 100kHz main clock signal in the digital blocks.

In order to reduce the interference from the digital blocks, the MOS transistors in analog blocks are designed to operate in the full swing mode. In the layout, the guard ring and a large gap between the analog and digital circuits are considered.

5 Measured results

The chip was fabricated in 0.6μm CMOS mixed-signal double poly and double metal technology. The die size was 2.1mm^2, including the core and I/O PADs, as shown in Fig. 5.

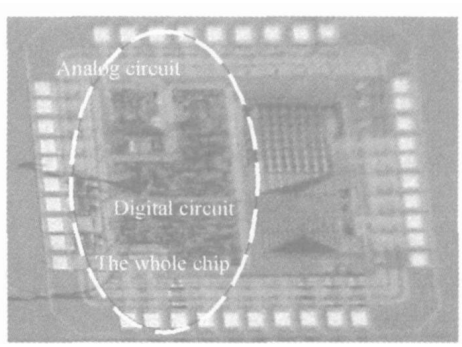

Fig. 5 Micrograph of the chip

The total static working current value of the chip is 1.94mA with a 5V supply. Therefore the power consumption is 9.7mW.

The measured result of digital "fixed delay" time when the value of the pin 10/11 is set to "0/0" and the value of the leakage current is 0.03I_N is shown in Fig. 6. Curve 1 in Fig. 6 is the detected leakage signal, and curve 2 is the output of the pin9, which is to switch-off the SCR. The gap between t_1 and t_2 is the fixed response time value T, which equals 0.26s. The statistic result of fixed response time is shown in Fig. 7, by the same measure method in different conditions, which achieved the specification we have designed. The HH11～HH14 are the state name for different levels presented in Table 1. The test results of the over voltage and overload signals, which also achieved the specification are shown in Table 2. The test result of pin8, which is to switch-on the SCR, achieved the fixed-delay time (60s), 60s later after the pin9 is on (the SCR is switch-off), pin8 is set to switch on the SCR, as well.

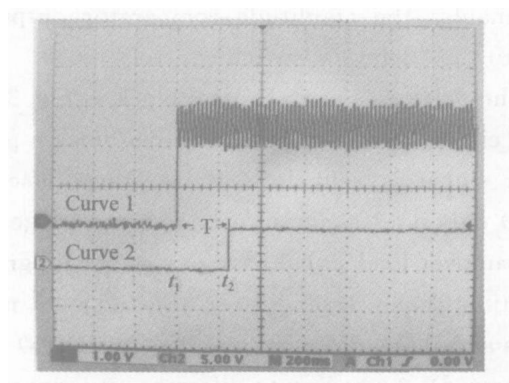

Fig. 6 Test result of fixed response time

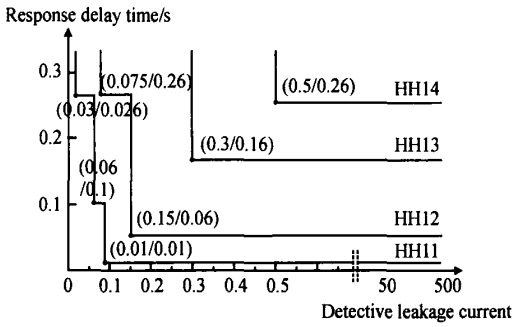

Fig. 7　Fixed response time of different levels

Table 2

	Over voltage		Overload	
Over value	1.36V_N	1.64V_N	1.45I_N	3I_N
Response time/ s	5	0.5	10	0.5

V_N : normal voltage ; I_N : normal current

6　Conclusion

A novel low-power multi-functional leakage current protector IC is developed. Based on mixed signal CMOS technology, this chip possesses the properties of low-power dissipation, high anti-interference ability, and accurate controlled response time. Besides these, multiple functions are integrated, such as over-voltage/over-load detection/protection, auto switching-on after a protection switch-off occurs, etc. This chip is also programmable for different application usages, meaning that it can be generally used in every level of the three different protection states.

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一种新型低功耗多功能漏电保护器芯片的设计*

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摘要: 提出了一种新型漏电保护芯片,使用 0.6μm CMOS 工艺、数模混合信号设计. 与传统的漏电保护芯片相比,该设计功耗低(10mW),数字延时响应确保控制保护的精确性,且实现了多功能集成(如漏电/过压/过流的检测与保护,自动切换). 此外通过可编程端,该芯片可以用在三级保护的不同场合,同时运用数字电路对输入信号的检测,提高了芯片的抗干扰性.

关键词: 漏电保护; 集成电路设计; 可编程芯片

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