Design and Fabrication of a High-Voltage nMOS Device *

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Abstract: High-voltage nMOS devices are fabricated successfully and the key technology parameters of the process are optimized by TCAD software. Experiment results show that the device's breakdown voltage is 114V, the threshold voltage and maximum driven ability are 1.02V and 7.5mA ($W/L = 50$), respectively. Experimental results and simulation ones are compared carefully and a way to improve the breakdown performance is proposed.

Key words: high-voltage nMOS devices; simulation; fabrication
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1 Introduction

High-voltage semiconductor devices have been used in a wide range of applications, such as drivers, actuators, regulators and so on; the devices are also used in switching devices with extremely low voltage drops at on-state, low leakage current at off-state, and fast switching times[1,2]. In order to achieve higher reliability and lower manufacturing cost, there has been growing interest in developing high-voltage devices that can be integrated in low-voltage CMOS circuits[3]. The method of integration provides an excellent way of achieving both high voltage and low voltage functions on the same chip; it reduces the cost of fabrication and reliability of circuit.

This paper presents a feasible method to fabricate high-voltage nMOS devices (HV-nMOS) based on 0.8μm CMOS process. The device can be used in high-voltage integrated circuits such as driver ICs for FED[4].

2 Device simulation

2.1 Device structure

Figure 1 shows the schematic cross-section of an HV-nMOS structure using bulk silicon p-substrate. The high-voltage nMOS device is lateral double-diffusion MOSFET (LDMOS), which can be fabricated in the standard CMOS process by means of adding extra masks and process steps.

As we can see from Fig. 1, L_d is the length of the drift region of HV-nMOS, and its lengthening can lead to the increase of breakdown voltage of HV-nMOS[5]. L_f is the length of the field plate, which can improve the breakdown voltage of HV-nMOS by reducing the surface electrical field[6]. L_c is the channel length of HV-nMOS, which determined by the lateral diffusion of the p well and HV n well.

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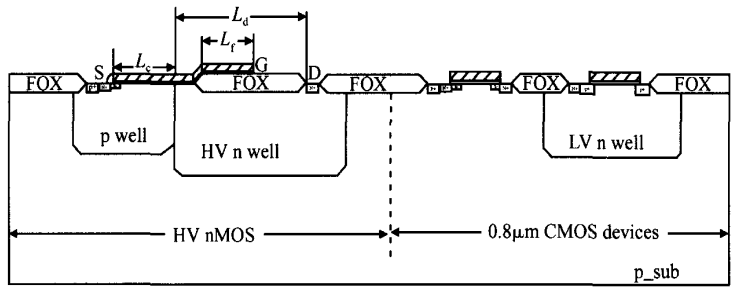


Fig. 1 Schematic cross-section of high-voltage nMOS device

2.2 Technology calibration

The HV n well is the drift region of HV-nMOS. The phosphorus in an HV n well can affect a device's breakdown voltage. The p well is the channel region of HV-nMOS, which can affect the threshold voltage and output current of the device. Thus, the technology parameters to form wells should be carefully designed by TCAD software[8]. In order to guarantee the validity of simulation results, the experiments to fabricate an n well and p well have been designed before the simulation.

From Table 1 and Table 2, we can see that the simulation results using default coefficients cannot match the experiment results. In order to make the simulated results more creditable, it is necessary to calibrate the coefficients of TSUPREM-4[8]. DIX.0 and DIP.0 represent the impurity diffusion coefficient of phosphorus and born in Si and SEG.0 represents the segregation coefficient of born between silicon and SiO_2[8]. Table 3 is the experimental and simulated results of an HV n well with calibrated coefficients.

Table 1 Results of experiment 1

n well	R_s/ (kΩ · □$^{-1}$)	X_j/μm	Coefficient in TSUPREM-4
Experimental results of experiment 1	2	5.3	
Simulated results using default coefficients	2.2	6.27	DIX.0 = 2.31 ×10^{10}
Simulated results using calibrated coefficients	2	5.4	DIX.0 = 1.3 ×10^{10}

Table 2 Results of experiment 2

p well	R_s/ (kΩ · □$^{-1}$)	X_j/μm	Coefficient in TSUPREM-4
Experimental results of experiment 2	3.8	4.81	
Simulated results using default coefficients	2.7	5.58	SEG.0 = 1.13 ×10^{3} DIP.0 = 4.10 ×10^{9}
Simulated results using calibrated coefficients	3.7	4.83	SEG.0 = 5 ×10^{2} DIP.0 = 3 ×10^{9}

Table 3 Simulated and measurement results of HV n well

Parameter	X_j/μm	R_s/ (Ω · □$^{-1}$)	Thickness of SiO_2 after anealling/ nm
Simulation	3.3	4910	378
Measurement	3.34	4829	362.8

2.3 Device simulation

In this paper, the structural parameters of the HV-nMOS are: L_d = 9.5μm, L_f = 7.5μm, L_c varies from 1.5μm to 3μm with the increase of 0.5μm. MEDICI[8] is used to simulate the breakdown char-

acteristic of HV-nMOS (L_c = 2μm). At low phosphorus doses, simulation result indicates surface breakdown around the n^+ drain region. As the implant dose increases to 1.3 ×10^{12}, a maximum bulk RESURF breakdown voltage is achieved; further increasing the implant dose leads to loss of RESURF action and decrease of breakdown voltage[7]. The RESURF technique is based on the total depletion of the HV n well region leading to a spreading of equipotential lines, just as Fig. 2 shows.

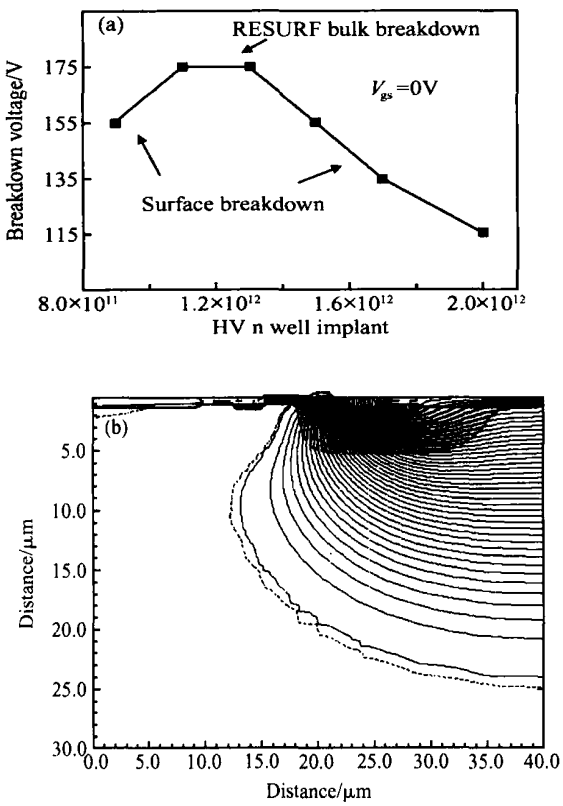


Fig. 2　MEDICI simulation results　(a) Breakdown voltage versus HV n well doping; (b) Equipotential contours of HV-nMOS (V_{gs} = 0V, V_{ds} = 170V)

3 HV-nMOS fabrication

The HV-nMOS is fabricated based on 0.8μm standard CMOS process in IMECAS (Institute of Microelectronics, Chinese Academy of Sciences). The following is the key process flows.

(1) BS p-substrate;

(2) Phosphorus implantation for HV n well;

(3) Boron implantation for p well;

(4) Annealing process to form HV n well and p well;

(5) Field implantation and LOCOS formation;

(6) Channel doping for HV-nMOS;

(7) Channel doping for low-voltage CMOS devices;

(8) Gate oxide formation;

(9) Gate formation;

(10) S/D formation;

(11) Contact and metallization.

The steps of (2～4, 6) are the extra steps to form HV-nMOS while the other steps are the standard CMOS process. In order to be compatible with standard CMOS process, the thickness of the gate oxide is 15nm and the formation of the two wells is assigned at the beginning of the whole process, thus the high-voltage process cannot affect the performance of low-voltage CMOS devices.

4 Results and discussion

The experimental results show that the maximum driven ability and threshold voltage of HV-nMOS (W/L = 100μm/2μm) are 7.5mA and 1.02V, respectively; the breakdown voltage of the device is 114V when V_{gs} = 0V. Table 4 is the comparison with related work[9].

Table 4　Electrical parameters of devices

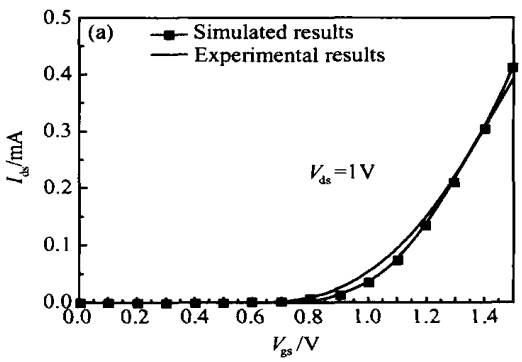
Device	Breakdown voltage (V_{gs} = 0V)	Output current (V_{gs} = 5V)	W/L	I_{ds}/L
HV nMOS	114V	7.5mA	50	7.5 ×10^{-5}A/μm
HV nMOS[9]	100V	7mA	90	5.2 ×10^{-5}A/μm

The comparison between simulated results and experimental results are shown in Fig. 3. The simulated threshold voltage and experimental threshold voltage are 0.84V and 1.02V (Fig. 3(a)). However, we can see that the deviation between simulated results and experimental results of output characteristics becomes obvious as V_{gs} increases, just as Fig. 3(b) shows.

In device simulation ,we do not take the interface states between silicon and silicon dioxide into account. In fact ,the Coulomb scattering mechanism of the interface states and fixed oxide charges is the dominant scattering mechanism as V_{gs} increases. The dependence of mobility on the gate field can be described by an empirical relationship of the following form:

$$\mu_s = \mu_0 \left(\frac{\varepsilon_0}{\varepsilon_{eff}}\right)^{\gamma}$$

where μ_0 is the maximum extracted value of the mobility at a given doping concentration and γ is an empirical constant. An increase of V_{gs} can lead to an increase in ε_{eff} ,which causes carriers to be drawn closer to the interface ,thus increasing surface scattering ,and hence lower mobility[10].



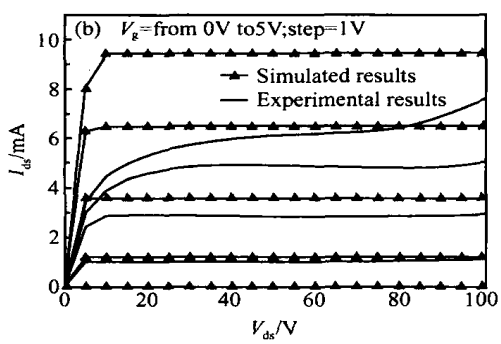


Fig. 3 Simulated results versus experimental results
(a) I_{ds}-V_{gs} characteristics; (b) Output characteristics

The output characteristics of different devices are compared in Fig. 5 ;the channel lengths of four devices are 1. 5 ,2 ,2. 5 ,and 3μm ,respectively. From Fig. 5 we can see that the decrease of channel length can lead to the increase of the device 's driven ability. However ,the short channel length may lead to the reduction of soft breakdown voltage because of punch-through :the breakdown voltage of HV-nMOS (L_c = 1. 5μm) is just 85V when V_{gs} = 5V. On the other hand ,the driven ability of the device is determined by two important factors: the length of drift region (L_d) and channel (L_c)[5]. Thus ,the increase of L_c cannot lead to the rapid decrease of driven ability. The experimental results show that the output current only decreases about 15 % when L_c increases from 1. 5μm to 2μm (Fig. 5) ; therefore , we can conclude that the channel length of HV-nMOS should be designed as 2μm in order to maintain the breakdown voltage of HV-nMOS and get an acceptable output current.

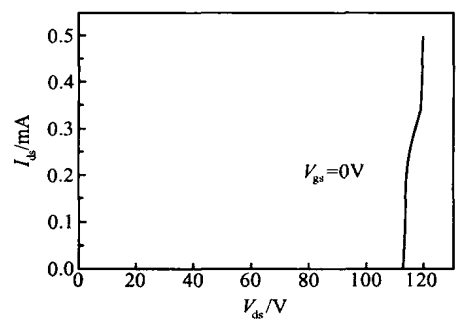


Fig. 4 Breakdown voltage of HV-nMOS devices

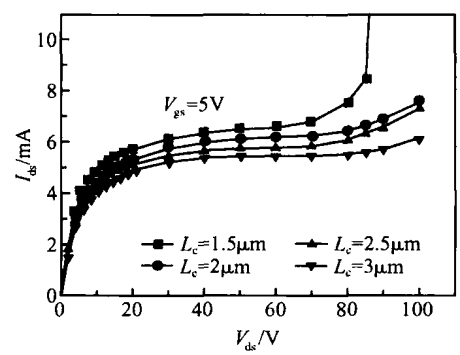


Fig. 5 Output characteristics of different channel

Figure 2 shows that the optimal breakdown voltage of HV-NMOS devices is 170V ,but the experimental result is still 114V. The reason for the discord is the effect of field implantation. In order to avoid parasitic MOSFETs between adjacent devices ,field implants should be done before LOCOS

process ;according to layout design rules of 0. 8μm CMOS process ,the distance of a field layer spaces well layer or active layer (L_1) is 3μm ,just as Fig. 6 shows. Figure 7 is the breakdown potential contours of HV-nMOS when V_{gs} = 0V , V_{ds} = 140V. The simulated results of MEDICI show that the position of the peak electrical field is (34. 75μm , 1. 456μm) and the weak point of breakdown is the p-n junction between the field implant region and the drift region of an HV-nMOS. In order to improve the breakdown performance of an HV-nMOS ,self-enclosed structure of the device can be adopted. Figure 8 shows the cross-section of it. We can see that the drain of HV-nMOS is surrounded by the regions of source and gate , so the breakdown between the field implant region and drift region can be avoided.

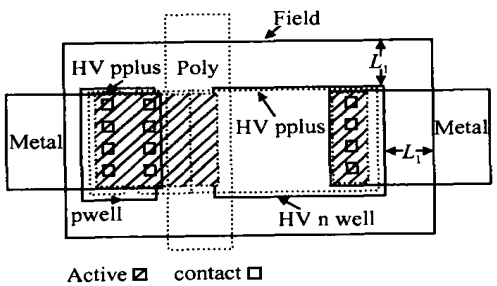


Fig. 6　Layout of HV-nMOS

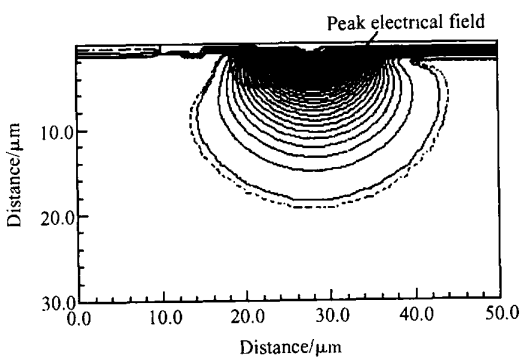


Fig. 7　Equipotential contours of HV-nMOS　V_{gs} = 0V , V_{ds} = 140V , L_1 = 3μm

5　Conclusion

In this paper ,an HV-nMOS has been successfully integrated with standard 0. 8μm CMOS process. Process steps are given in detail after simulation and optimization by TSUPREM-4 and MEDICI. The HV-nMOS has been fabricated in IMECAS and the device exhibits excellent DC characteristics and acceptable breakdown performance. A way to improve the breakdown performance of the device is proposed. The process and the structure of an HV-nMOS are feasible for high-voltage applications.

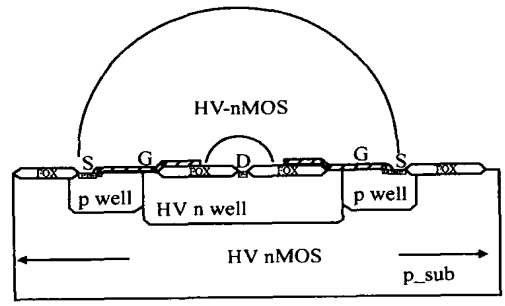


Fig. 8　Self-enclosed HV-nMOS

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高压 nMOS 器件的设计与研制 *

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摘要: 根据 TCAD 软件模拟的最优工艺条件成功研制了高压 nMOS 器件. 测试结果表明器件的击穿电压为 114V , 阈值电压和最大驱动能力分别为 1. 02V 和 7. 5mA ($W/L = 50$) . 详细比较了器件的模拟结果和测试数据 ,并且提出了一种改善其击穿性能的方法.

关键词: 高压 nMOS 器件; 模拟; 制造

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