2. 5Gb/ s Monolithic IC of Clock Recovery ,Data Decision , and 1 ∶4 Demultiplexer *

Chen Yingmei , Wang Zhigong , Xiong Mingzhen , and Zhang Li

(*Institute of RF &OE-ICs , Southeast University , Nanjing* 210096 , *China*)

Abstract : A high integrated monolithic IC ,with functions of clock recovery ,data decision ,and 1 ∶4 demultiplexer ,is implemented in 0. 25μm CMOS process for 2. 5Gb/ s fiber-optic communications. The recovered and frequency divided 625MHz clock has a phase noise of - 106. 26dBc/ Hz at 100kHz offset in response to a 2. 5Gb/ s PRBS input data (2^{31} - 1) . The 2. 5Gb/ s PRBS data are demultiplexed to four 625Mb/ s data. The 0. 97mm ×0. 97mm IC consumes 550mW under a single 3. 3V power supply (not including output buffers) .

Key words : optical transmission systems ; clock recovery circuits ; data decision ; 1 ∶4 demultiplexer ; charge pump phase-locked loops

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1 Introduction

With the explosive development of telecommunication networks , computer networks and internet ,it is time to build up information highways. Optic fiber communications have been widely used in the world because of their many merits ,such as huge capacity ,long distance transmission ,economizing resource ,anti interference and radiation ,etc. Nowadays , synchronous digital hierarchy (SDH) and synchronous optical networks (SONET) based on optical transmission network have been widely constructed and applied in the world.

The clock and data recovery (CDR) circuit is the key component in optical digital transmission systems. Many papers and textbooks covering CDR design have been published[1 ,2] . However ,for commercial application , the optical receiver must be high integrated , insensitive to temperature and component variations and have few external components. This paper adopts the charge pump phase-locked loops (CPPLL) scheme ,the phase detector (PD) in CPPLL , which can detect the phase to generate early-late phase logic , and PD ’s special function ,which is sampling the data to act as a 1 ∶2 demultiplexer. Therefore , three blocks including clock recovery , data decision , and 1 ∶4 demultiplexer of an optical receiver are integrated monolithically.

2 Circuit description

The architecture of a monolithic clock data recovery and 1 ∶4 demultiplexer chip is shown in Fig. 1. In the system , the sampling and early-late phase logic circuits act as a phase detector. In the sampling circuit ,samples of a ,b ,c ,d ,and e are gen-

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Chen Yingmei female , PhD candidate , lecturer. She is working in the field on high-speed/ frequency ICs. Email : njcym @seu. edu. cn

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erated from the input data. These 5 samples carry the time information between the input data and the clock generated by the VCO. The early-late phase logic circuit processes these samples and provides an early-late signal to the charge pump. At the same time ,the sampling circuit acts as a 1 ∶2 demultiplexer.

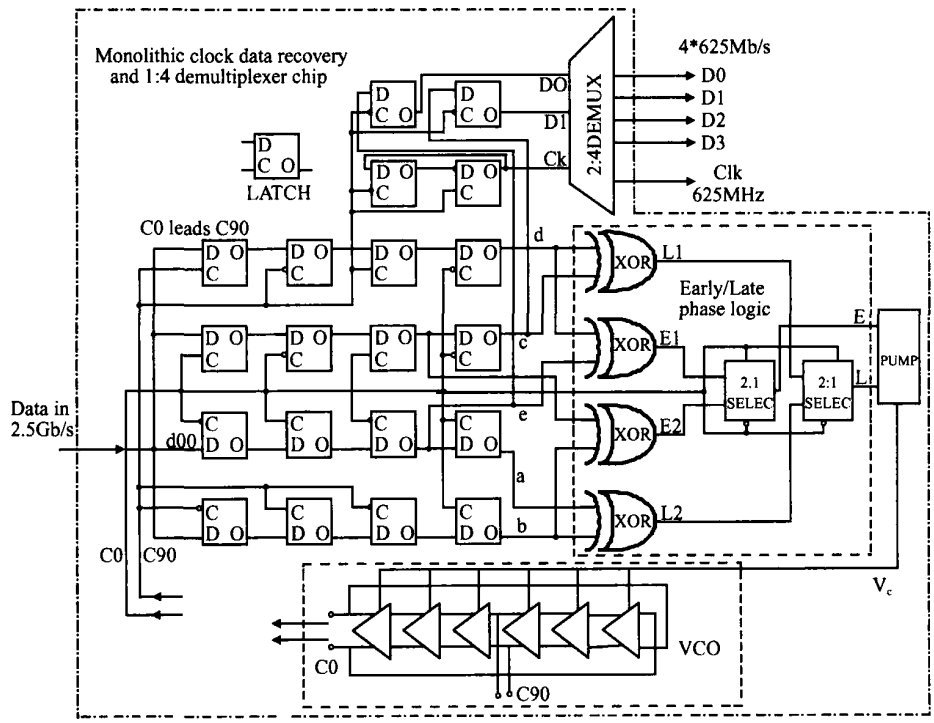

Fig. 1　Monolithic clock data recovery and 1 ∶4 demultiplexer chip architecture

2. 1　PD

The work scheme of the specially designed phase detector is as follows:the transitions of the binary signal are measured as early or late events when compared with the transitions of the clock signal. The sampling diagram is shown in Fig. 2. The frequency of the clock is half of the bit rate of the data. The samples are taken by two orthogonal clocks of C0 and C90. Let samples a and c be taken close to the mid-points A and C of two adjacent bits ,and the sample b at the changeover times between A and C.

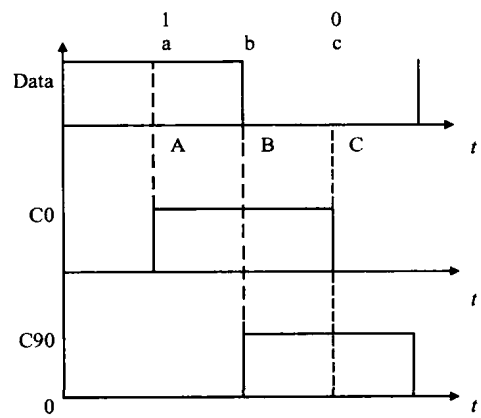

Fig. 2　Sampling diagram

Thus ,the samples a ,b ,and c are related to the early-late situations by the following rules:

(1) if abc = 110 ,the clock is early.

(2) if abc = 100 ,the clock is late.

The structure of the sampling circuit (as shown in Fig. 1) is constructed according to the sampling diagram . The frequency of C0 and C90 being half of the data has two merits: (a) The phase detector can act as a 1 ∶2 demultiplexer ,so the whole system can accomplish 1 ∶4 demulti-

plexing after adding the latter 2 ∶4 demultiplexer and (b) the half-rate scheme makes it possible to upgrade the speed of the clock recovery circuit to a higher bit rate level[3].

2.2 Early-late phase logic circuit

Let E represents early, L represents late and X represents indecision. The eight possible combinations of abc and the conclusion drawn from the four rules are shown in Table 1.

Table 1 Sampling logic

a	b	c	Conclusion
0	0	0	X
0	0	1	E
0	1	0	X
0	1	1	L
1	0	0	L
1	0	1	X
1	1	0	E
1	1	1	X

If ⊕ represents the modulo-2 sum, E and L can be given by

$$E = b \oplus c, \quad L = a \oplus b$$

The early-late phase logic circuit of this paper (in Fig. 1) has simpler logic and less transistor than previous work[4]. It processes these samples and provides an early-late signal to the charge pump. High operation frequency can be achieved by the resistively-loaded MOS current mode logic (MCML) circuit because of its small signal swing. Several basic cells, such as latch, selector, and XOR, all adopt MCML structure.

2.3 VCO and charge pump

VCO adopts 6 stages ring oscillators, as it can offer several advantages over LC oscillators. First, the symmetry of this architectrue ensures that precise in-phase (C0) and quadrature (C90) clocks are generated. In addition to saving chip area, another important benefit of this simple design is its huge tuning range. The control of the VCO is split into a coarse tuning input and a fine tuning input. The fine control is established by the phase detector and the coarse control is a provision for the change of temprature and technology. The logic of delay cell is implemented in resistively-loaded MOS current mode logic in order to reduce switching-related supply noise for its relatively constant current drawn from the power supply (as in Fig. 3). The charge pump also adopts differential structure to alleviate mismatch and the charge-sharing problem (as in Fig. 4)[2].

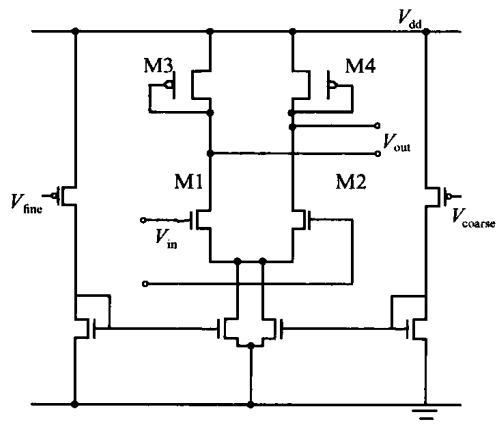

Fig. 3 Delay cell of the VCO

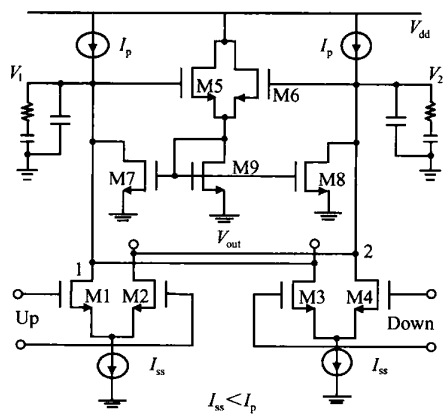

Fig. 4 Charge pump schematic

The closed loop transfer function $H(s)$ of the second-order charge-pump PLL is

$$H(s) = \frac{\frac{I_p K_{vco}}{2\pi C_p} \times (R_p C_p s + 1)}{s^2 + \frac{I_p}{2\pi} K_{vco} R_p s + \frac{I_p}{2\pi C_p} K_{vco}} \quad (1)$$

The natural angular frequency ω_n can be deduced from the closed loop transfer function $H(s)$,

$$\omega_n = \sqrt{\frac{I_p K_{vco}}{2\pi C_p}} \qquad (2)$$

So ,the capacitor C_p of the loop filter can be decreased to a small value ,as to integrated in chip by reducing the current I_p of the charge pump and the gain K_{vco} of the oscillator. The whole CDR-1 ∶4DEMUX chip has no external components and is highly integrated.

3　Simulation and experiment results

The performance of the proposed charge pump phase-locked loops is simulated with a 0. 25μm CMOS process of TSMC. Figure 5 shows the eye-diagram of one recovered and demultiplexed data at 625Mb/ s. The demultiplexed eye is very open and has very low jitter. A photograph of the 0. 97mm × 0. 97mm CDR-1 ∶4DEMUX chip is shown in Fig. 6. The pad configuration used is dictated by the on-wafer probes used for testing. An extensive bottom metal ground plane is included in the layout to increase the capacitance from substrate to ground. The phase noise of the divide-by-2 frequency spectrum of the recovered clock (in Fig. 7) is - 106. 26dBc/ Hz at 100kHz offset from the 625MHz carrier.

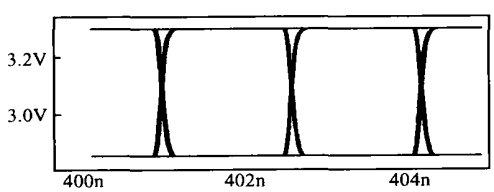

Fig. 5　Eyediagram of one 625Mb/ s data

The tuning range of the VCO coarse control comes up to 400MHz. The CDR circuit exhibits a capture range of 80MHz. Figure 8 shows the jitter histogram of the recovered 625MHz clock is 11. 72ps. The waveforms with a 2. 5Gb/ s input data and four 625Mb/ s output data are shown in Fig. 9. It is shown that the lower speed data have been correctly demultiplexed.

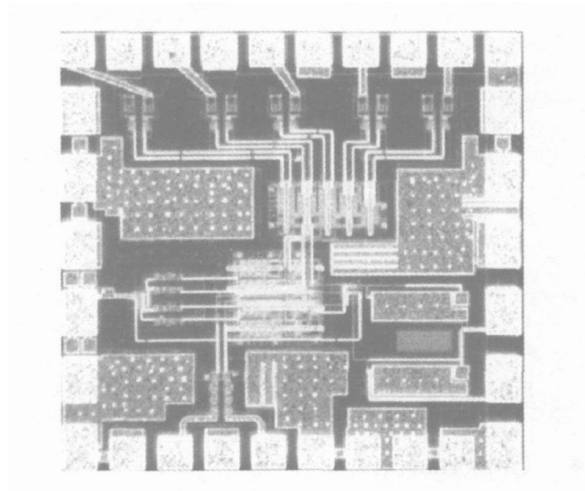

Fig. 6　Chip photograph

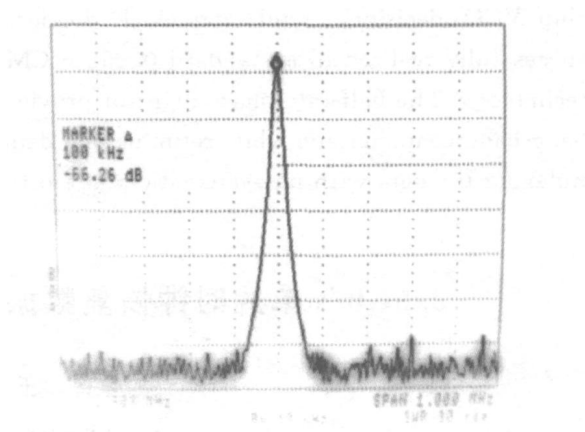

Fig. 7　Divide-by-2 frequency spectrum of the recovered 1. 25GHz clock

Input data	Di :	1110	0101	0001	1010	0111	0100	1101	0010
Output data	D2 :	1	0	0	1	0	0	1	0
	D3 :	0	1	1	0	1	0	1	0
	D1 :	1	1	0	0	1	1	1	0
	D0 :	1	0	0	1	1	0	0	1

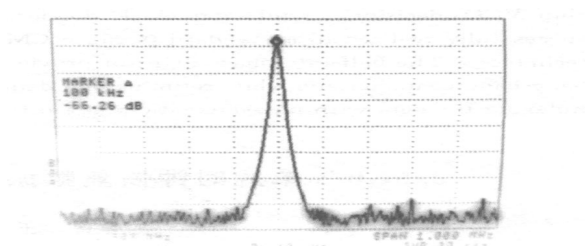

Fig. 8　Jitter histogram of the recovered 625MHz clock

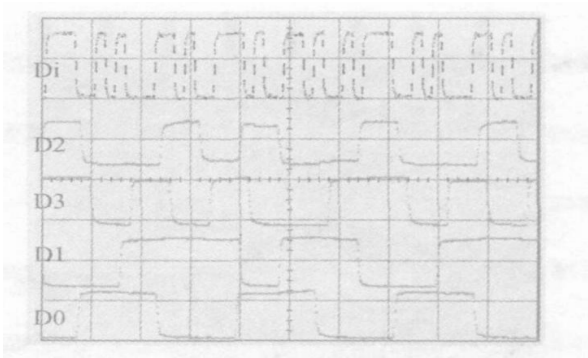

Fig. 9 Waveforms of the input and 4 output data

4 Conclusion

A complex mixed-signal CDR chip with on-chip VCO, decision circuit, and clock dividers is successfully realized in a standard 0.25μm CMOS technology. The half-rate phase detector provides a bang-bang characteristic while retiming and demultiplexing the data with no systematic phase offset. The CDR IC is used as a DEMUX to convert a 2.5Gb/s data signal to four 625Mb/s signals. The high integration, low power dissipation, and low cost of the CMOS process holds great promise for the implementation of optical communication circuits in this technology.

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2.5Gb/s 单片时钟恢复数据判决与 1∶4 分接集成电路的设计*

陈莹梅 王志功 熊明珍 章 丽

(东南大学射频与光电集成电路研究所, 南京 210096)

摘要: 用 0.25μm CMOS 工艺实现一个复杂的高集成度的 2.5Gb/s 单片时钟数据恢复与 1∶4 分接集成电路. 对应于 2.5Gb/s 的 PRBS 数据($2^{31}-1$),恢复并分频后的 625MHz 时钟的相位噪声为 -106.26dBc/Hz @100kHz,同时 2.5Gb/s 的 PRBS 数据分接出 4 路 625Mb/s 数据. 芯片面积仅为 0.97mm ×0.97mm,电源电压 3.3V 时核心功耗为 550mW.

关键词: 光纤传输系统; 时钟恢复电路; 数据判决; 1∶4 分接; 电荷泵锁相环

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陈莹梅 女,博士研究生,讲师,研究方向为超高速集成电路设计.

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