A CMOS Fully Integrated Frequency Synthesizer with Stability Compensation *

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Abstract : A complete closed-loop third-order s-domain model is analyzed for a frequency synthesizer. Based on the model and root-locus technique ,the procedure for parameters design is described ,and the relationship between the process ,voltage ,and temperature variation of parameters and the loop stability is quantitatively analyzed. A variation margin is proposed for stability compensation. Furthermore ,a simple adjustable current cell in the charge pump is proposed for additional stability compensation and a novel VCO with linear gain is adopted to limit the total variation. A fully integrated frequency synthesizer from 1 to 1. 05 GHz with 250 kHz channel resolution is implemented to verify the methods.

Key words : frequency synthesizer ; closed-loop third-order s-domain ; loop parameters ; PVT variation ; stability ; variation margin

EEACC : 1205 ; 2570D

CLC number : TN4 **Document code : A** **Article ID :** 0253-4177(2005)08-1524-08

1 Introduction

Monolithic frequency synthesizers based on charge pump PLL (CPLL) are prevailing in modern communication systems. Loop performances , such as stability ,phase noise (or jitter) ,and switching speed ,are important design criteria and discussed in many publications[1~6]. Synthesizer design is a tradeoff process to derive the parameters according to specifications. Unfortunately ,current , resistor ,and capacitor always vary with process , voltage ,and temperature (PVT). VCO gain is always highly nonlinear. Variation and nonlinearity tend to unstabilize the loop ,especially in strict conditions. In order to have stability ,one way is to sacrifice performance of the phase noise and spur level suppression. The better methods are to use configurable current to compensate the change of division ratio[7] and nonlinearity of VCO gain[4]. However , these methods are of some complexity and not able to compensate for all variation factors.

A CPLL based frequency synthesizer is inherently discrete-time. Fortunately ,accurate z-domain models ,state space analysis[8,9] ,and impulse-invariant transformation[10] ,have proven that if the loop bandwidth is less than 1/20 of the reference clock , s-domain model predicts the same behavior as z-domain models. As a result , s-domain model is also suitable for a CPLL frequency synthesizer. Traditionally ,closed-loop s-domain model is always simplified into second order[1,8]. However , the actual

* Project supported by the Shanghai Science & Technology Committee ,China Under System-Design-Chip (SDC) Program (No. 037062019) and the Shanghai AM(Applied Material) Funds(No. 0425)

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Received 25 November 2004 ,revised manuscript received 13 March 2005

loop is third order or even fourth order. Open-loop s-domain model is discussed in the third order[2]. Although an open-loop s-domain model is simple for analysis, the roughly defined phase margin is indirect and not able to accurately describe the closed-loop performance and predict the effect of the parameters' PVT variation. The complete analysis on the closed-loop third-order s-domain model is still absent up to now.

In this paper, the complete analysis on the closed-loop third-order s-domain is performed to derive the design procedures for loop parameters. The effects of the parameters' PVT variation on the stability is quantitatively analyzed with the aid of the root locus technique. An adjustable current cell in the charge pump is proposed to realize the damping factor control to compensate the total variation of the parameters, which is based on the variation analysis. A novel cross-switched VCO with linear gain is also adopted to reduce the total variation.

2 Closed-loop third-order s-domain analysis and loop parameters

2.1 Closed-loop third-order transfer function analysis

In the typical CPLL frequency synthesizer with continuous-time loop filter, as shown in Fig. 1, the open loop transfer function is

$$H_o(s) = \frac{K_{CP} K_{VCO}}{N} \times \frac{Z(s)}{s} \tag{1}$$

where K_{CP} is the gain of phase detector and charge pump, $Z(s)$ is the impedance of loop filter.

$$K_{CP} = \frac{I_{CP}}{2\pi}, \quad Z(s) = \frac{b}{C_1} \times \frac{s + \omega_z}{s(s + \omega_p)},$$

$$\omega_z = \frac{1}{RC_1}, \quad \omega_p = (b + 1)\omega_z$$

Here b is the ratio between C_1 and C_2. The open loop transfer function can be rewritten as

$$H_o(s) = K' \frac{s + \omega_z}{s^2 (s + \omega_p)} \tag{2}$$

where $K' = \dfrac{K_{CP} K_{VCO} b}{N C_1}$.

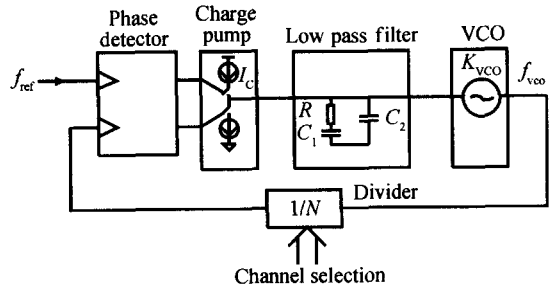

Fig. 1　Architecture of frequency synthesizer

Closed-loop transfer functions have been simplified to second order and discussed in Ref. [1]. However, the simplified analysis will miss some implicit relationships between the parameters and performance. The complete closed-loop third-order transfer function must be considered as following,

$$H(s) = \frac{N H_o(s)}{1 + H_o(s)} = \frac{N K'(s + \omega_z)}{s^3 + \omega_p s^2 + K' s + K' \omega_z}$$

$$= \frac{N K'(s + \omega_z)}{(s^2 + 2\zeta\omega_n s + \omega_n^2)(s + \omega_{p3})} \tag{3}$$

where ω_n is the nature frequency, ζ is the damping factor, ω_{p3} is the closed-loop single pole.

The relationship of zeros and poles between open-loop and closed-loop is summarized as

$$2\zeta\omega_n + \omega_{p3} = \omega_p \tag{4}$$

$$\omega_n^2 + 2\zeta\omega_n\omega_{p3} = K' \tag{5}$$

$$\omega_n^2\omega_{p3} = K'\omega_z \tag{6}$$

According to Eqs. (4)～(6), the analytical equation is derived,

$$2\zeta\omega_n^2 - ((4\zeta^2 - 1)\omega_z + \omega_p)\omega_n + 2\zeta\omega_p\omega_z = 0 \tag{7}$$

Suppose $\omega_n = m\omega_z$, where m is the nature frequency factor. Take it into Eq. (7), and then derive

$$2\zeta m^2 - (4\zeta^2 + b)m + 2\zeta(b + 1) = 0 \tag{8}$$

Solving Eq. (8), m can be expressed as a function of b and ζ, i.e. $m = m(b, \zeta)$.

From Eq. (4), the third pole ω_{p3} in the closed-loop transfer function can be expressed as

$$\omega_{p3} = (b + 1 - 2\zeta m)\omega_z \tag{9}$$

which is often neglected by the second order simplification.

2.2 Loop parameters design

The target of loop parameters design is to achieve the desirable loop performance. With the closed-loop analysis, it is possible to design the damping factor and nature frequency directly. The nature frequency is always dependent on the damping factor; consequently, a damping factor could be set as a target at the beginning of parameter design, for example, $\zeta = 1$. Capacitor ratio b should also be predefined. On the one hand, a small b makes the pole ω_p close to the zero ω_z, and results in the low frequency closed-loop pole ω_{p3}. This can better filter high frequency noise from input and divider, and better attenuate clock injection spurs from the charge pump. On the other hand, b must be larger than 8 for stability[8]. Then, b might be set to 9 or 10 for the best possible noise performance at the beginning.

Taking $\omega_n = m\omega_c$ and $\omega_p = (b+1)\omega_c$ into Eqs. (4) and (5), gain factor K' can be expressed as

$$K' = k(b,\zeta)\omega_c^2 \tag{10}$$

where $k(b,\zeta)$ is also a function of b and ζ, it is expressed as

$$k(b,\zeta) = (1 - 4\zeta^2)m^2 + 2\zeta(b+1)m \tag{11}$$

For $K' = bI_{CP}K_{VCO}/2\pi NC_1$, then $k(b,\zeta)\omega_c^2 = bI_{CP} \times K_{VCO}/2\pi NC_1$, resistor R can be expressed as

$$R = \frac{2\pi Nk(b,\zeta)}{bI_{CP}K_{VCO}}\omega_c \tag{12}$$

Loop bandwidth ω_c is an important parameter. As mentioned early, s-domain model is accurate in the whole bandwidth only if the loop bandwidth is no larger than 1/20 reference frequency[9]. Because it is difficult to design a pretty low noise VCO in CMOS technology, it is preferable to have a high loop bandwidth. High loop bandwidth also has the advantage of a fast switching speed. A good initial loop bandwidth is 1/25 reference frequency. From Eq. (2), let $s = j\omega_c$ and $|H(j\omega_c)| = 1$, with Eq. (10), zero ω_z can be calculated as

$$\omega_z = \frac{1}{n(b,\zeta)}\omega_c \tag{13}$$

where $n(b,\zeta)$ is the function of b and ζ, too. Until now, the procedure to determine the loop parameters is

(P.1) Find K_{VCO} from simulation.

(P.2) Select capacitor ratio b and damping factor ζ_0, then calculate m, n, and k.

(P.3) Select loop bandwidth ω_c according to reference clock, a good start-point: $\omega_c = \omega_{ref}/25$.

(P.4) Calculate zero ω_z, ω_n, and ω_{p3}.

(P.5) Choose charge pump current I_{CP}, and dividing ratio N.

(P.6) Calculate R from Eq. (12), if R is too large, increase the pump current I_{CP} and recalculate R until its value is reasonable.

(P.7) Calculate C_1, C_2, if the value is too large, decrease pump current I_{CP}, and go to P.6.

2.3 Parameters variation, stability, and margins

Basically, loop transfer function changes with N to synthesize various frequencies. A configurable charge pump is used to keep the ratio N/K_{CP} to maintain the loop performance[7]. The undetermined parameters variation still arises from process, temperature, and voltage. Traditionally, phase margin optimization is simple and always used to determine the loop parameters[2]. A primary phase margin should be pre-defined for calculation, which is usually set to about 50°. However, variation of loop parameters changes the phase margin. Phase margin optimization technique cannot predict how much variation it can tolerate. Root locus technique could be adopted to illustrate the influence of parameters' variation. The parameters such as I_{CP}, R, C_1, C_2, and K_{VCO} will vary with PVT variation. What are the influences of the variation?

Figure 2 is the root locus of the loop. Poles migrate with the factor K'. Points B, C are the boundary to avoid under-damping behavior. To margin the loop parameter variation, for example, point A can be selected to identify the system, and the damping factor ζ is 1. If the gain factor K' deviates smaller than the designed value, poles will migrate towards point B and its conjugate pole, as

well as the damping factor becoming smaller. If the gain factor K' deviates larger than the designed value, poles will migrate to point C and the zero through the locus, as well as the damping factor becoming larger at the start and then smaller after passing around point D. When poles exceed the boundary, the loop might become under-damping.

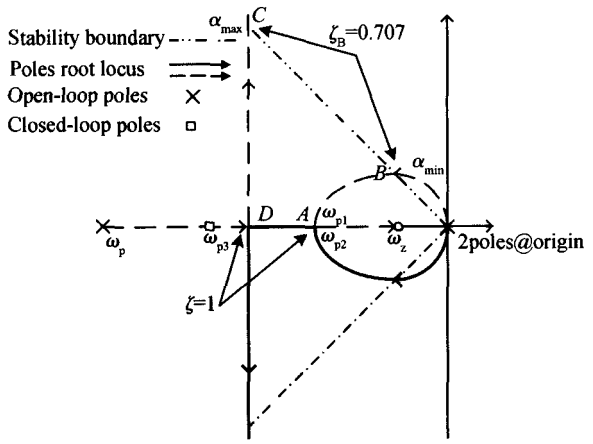

Fig. 2　Root locus plot of loop

With designed damping factor ζ_0, rewrite Eq. (12) to

$$k(b,\zeta_0) = \frac{K_{VCO} I_{CP} b R^2 C_1}{2\pi N} \quad (14)$$

Due to the technology, temperature, and voltage variation, the changes of I_{CP}, K_{VCO}, R, C_1, and C_2 will disturb the closed loop poles. The actual damping factor results in:

$$k(b,\zeta) = \alpha k(b,\zeta_0) = \alpha \times \frac{K_{VCO} I_{CP} b R^2 C_1}{2\pi N} \quad (15)$$

where α is named as variation factor. Now consider the boundary condition: $\zeta_B = 0.707$, which results α_{max} and α_{min}. α_{max} is the top boundary of total parameter variation and α_{min} is the bottom boundary. For example, if $\zeta_0 = 1$ and $b = 9$, then $\alpha_{max} = 1.57$ and $\alpha_{min} = 0.65$, and the loop could tolerate a total 35 % parameters variation at least. Variation margin can be defined as the minimum of $\alpha_{max} - 1$ and $1 - \alpha_{min}$. In fact, there exists an optimum variation margin, which corresponds to an optimum damping factor ζ_{opt} larger than ζ_0. Due to mathematical complexity, optimum damping factor is not discussed here. For a small b, $\zeta_0 = 1$ is acceptable approximation for ζ_{opt}. Quantitative analysis based on third-order model accurately shows the effect of parameters variation on the closed-loop damping factor and stability. Additionally, variation margin increases with b. If the predicted variation margin cannot tolerate the total maximum PVT variation, then b should be increased for the large variation margin.

3　Circuit implementation

3.1　Phase detector

Due to the slow input frequency, a phase detector can be implemented with the most popular D flip-flop tri-state configuration[11]. There are dead-zone elimination delay chain and differential outputs equalization.

3.2　Charge pump with stability compensation current cell and loop filter

A differential charge pump has better supply noise rejection performance and phase noise performance[12]. Figure 3 is the schematic of the charge pump. Due to differential architecture, ideal matched charge pump and loop filter can eliminate the problems by clock feed through and charge injection.

However, the mismatch always exists and the problems with the mismatch should be considered. First, level shifters are used to reduce the swings of switch signals to attenuate the clock feed through. Half reduction of swing improves the performance of reference spur suppression by 6dB. Second, channel charge injection from switch transistors, e. g. PM1 and NM1, can be attenuated with isolation by saturated transistors, e. g. PM3 and NM3.

In section 2, parameters variation has been analyzed. If the total variation exceeds the boundary of stability, i. e. (α_{min}, α_{max}), current adjustment can take the loop back to the stable state. A proposed double-half adjustable current cell is shown in Fig. 4. The current cell consists of four branches, of

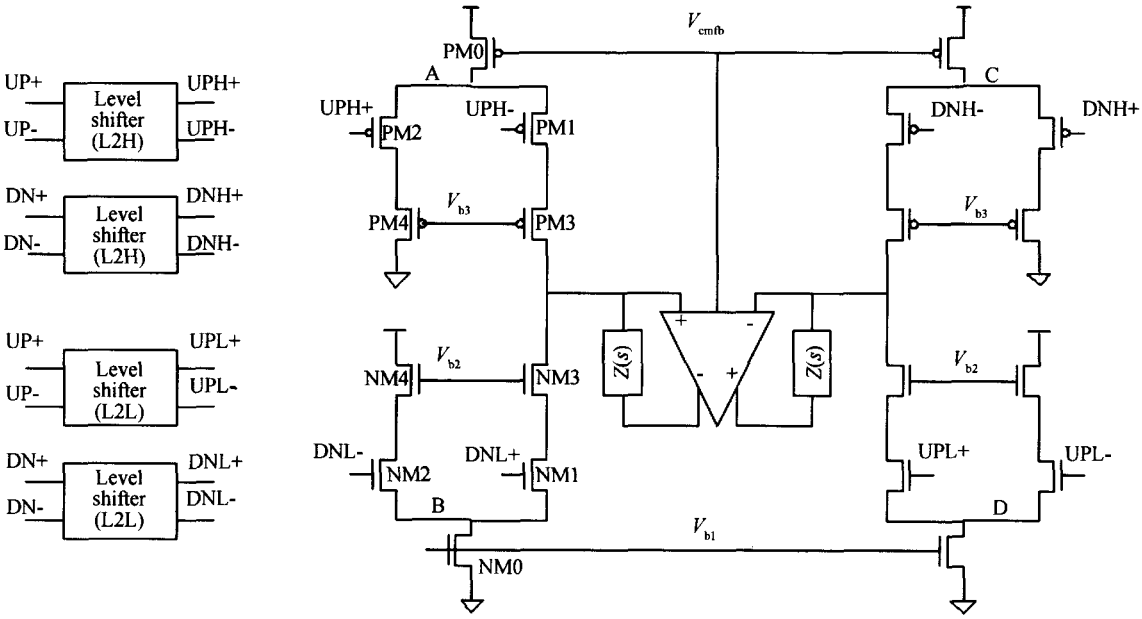

Fig. 3 Differential charge pump schematic

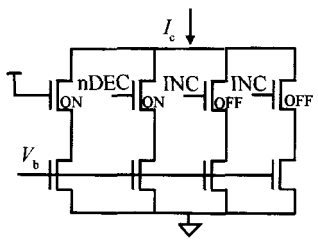

Fig. 4 Proposed current cell with double-half adjustment

which two are ON and two are OFF in default. If α is larger than α_{max}, it should decrease the current I_{CP} by disable (nDEC = 0) one current branch to half the factor α. If α is smaller than α_{min}, then increase I_{CP} by enable (INC = 1) two current branches to double the factor. For example, if α_{min} = 0.5, α_{max} = 1.5, $\Delta K_{VCO}/K_{VCO}$ = 0.2, $\Delta I_c/I_c$ = 0.2, $\Delta R/R$ = 0.2, and $\Delta C_1/C_1$ = 0.1, the worst total negative variation without adjustment according to Eq. (15) is 0.37, which is below α_{min}, and the loop tends to be under-damping. With the current double adjustment, the total variation factor becomes 0.74, which is acceptable. The similar half adjustment is for the worst positive variation. The simple current cell can replace the transistor NM0 and PM0 in Fig. 3. There is also a complex technique that adjusts current to keep the ratio I_{CP}/N as N changes[7]. The obvious improvement here is that extra variation is considered, contributed from not only N but also the charge pump current I_{CP}, loop filter, and VCO gain K_{VCO}.

3.3 Linear gain VCO

VCO comprises complementary cross-coupled negative G_m pairs and LC-tank, as shown in Fig. 5. V_{c_p} and V_{c_n} are differential control nodes to increase the linearity of K_{VCO} by symmetry. The tank consists of inductor, capacitor, and cross-switched varactors. The varactors are realized by MIM capacitors and the cross switches are realized by transistors. Excellent linear property has been demonstrated in Ref. [13]. The better linear VCO gain results in smaller variation and is better for the stability. Phase noise performance can also be improved with inductors L1, L2 and capacitors C1～C3.

3.4 Divider

A divider is implemented in ripple-like local-feedback architecture[14]. The divider has a range from 2^k to 2^{n+1}-1. The most important benefit of the structure is to reuse the 2/3 divider cell. The

cell could be implemented with the true-single-phase-clock (TSPC) logic.

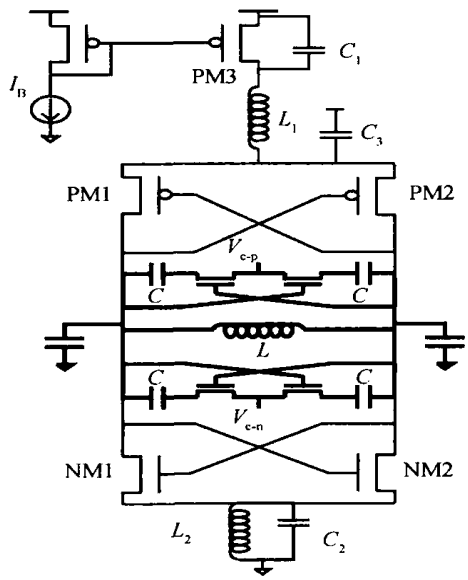

Fig. 5　Differential complementary cross-coupled-begative-G_m VCO with cross-switched varactor

4　Simulation and verification

The fully integrated frequency synthesizer is implemented in 0. 25μm CMOS RF technology. Micrographic is shown in Fig. 6. The synthesized frequency ranges from 1 to 1. 05 GHz with resolution 250 kHz. This results in a large frequency-dividing ratio of about 4000. The parameters are summarized in Table 1.

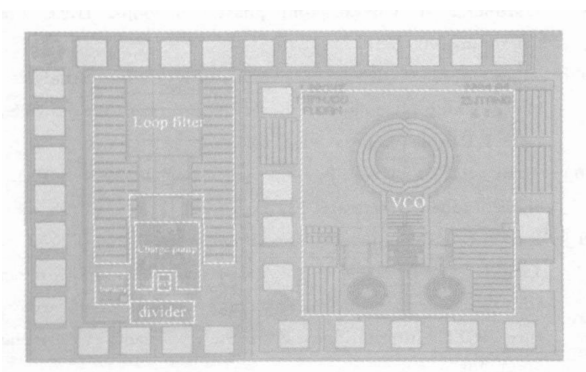

Fig. 6　Micrographic of frequency synthesizer

Table 1　Design parameters summary

K_{VCO}	20～40 MHz/ V
N	4000～4200
I_{CP}	20μA
f_c	10 kHz
b	10
R	460 kΩ
C_1	112 pF
C_2	11. 2 pF
f_{ref}	250 kHz
ζ_0	1
α_{max}	1. 68
α_{min}	0. 63

Damping factor variation is simulated with the technology variations. In typical CMOS technology, suppose $\Delta R/R \approx 0.2$ and $\Delta C/C \approx 0.1$ at the worst corner. Current can always be trimmed externally and of variation limited in 10 %. Due to the nonlinearity of the VCO tuning curve, K_{VCO} varies more widely than other parameters. From LC-VCO analysis, variation of K_{VCO} is within 50 % by careful design[13]. In this example, the design value is set at 30 MHz/ V after simulation. The division ratio N will also contribute to the variation factor. In this verification, the division ratio contributes little to variation factor because of its relative small change. Then, the worst negative variation factor is 0. 26 and the worst positive variation factor is 2. 6. The simulated step responses are shown in Fig. 7, including curves with no variation, worst negative variation, and worst positive variation. Negative variation tends to make the loop under-damping more obviously than positive variation. The reason is that the dominant pole ω_{p3} in positive variation is

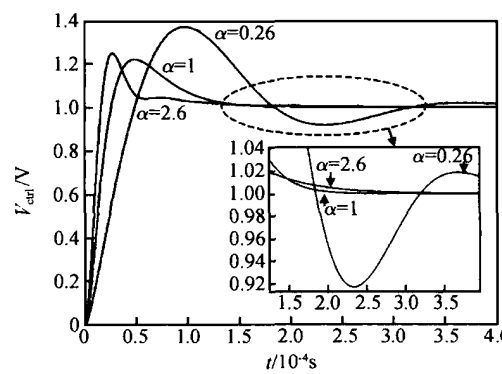

Fig. 7　Step responses for technology variations

real, but not complex, as in negative variation. However, large positive variation is not desired due to the small ripple caused by under-damping. The measured channel switching responses of control voltage are shown in Fig. 8. To verify the variation factor analysis, VCO operates at 1GHz with gain smaller than 30MHz/V. Normally, the charge pump current is trimmed to the designed value by the external reference I_{ref}, when no adjustment is required and the response of the loop is stable because of the variation margin. After the external reference current is set 60% smaller than designed value, the extra negative variation of charge pump current is introduced and the loop goes to under-damping. With the double adjustment of variation factor, the switching response is compensated and more stable than that without adjustment.

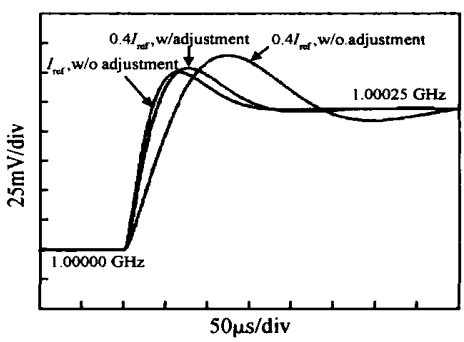

Fig. 8 Channel switching responses of control voltage for variation factor adjustment test, with 60% extra current reduction

5 Conclusion

The complete closed-loop third-order s-domain model is analyzed. Based on the analysis, a procedure for parameter design is proposed for the frequency synthesizer, and the margin for the total parameters' PVT variation is quantitatively analyzed. It is suggested that the damping factor $\zeta_0 = 1$ is a good start to variation toleration. For more variation, a double-half adjustable current cell in the charge pump is proposed to compensate the variation for the stability. Additionally, a novel VCO with linear gain is adopted to limit the total variation, for the stability concerns. The simulation and measurement results well verify the analysis and methods with the example.

Acknowledge The authors would like to thank Li Fuxiao, Chen Zai, and Wang Xiuying for chip package and testing. We would also like to thank Liu Chenbo, Yi Wei, and Jiang Qifeng of Shanghai Research Center for Integrated Circuit Design, China, for the support of MPW service.

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CMOS 集成频率综合器的稳定性补偿*

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摘要：通过分析频率综合器的完整三阶闭环 s 域模型，同时采用根轨迹分析技术，定量分析了工艺、电压和温度引起的环路参数变化对频率综合器稳定性的影响，并提出变化裕量的概念来进行稳定性分析和参数设计. 为了获得更加稳定的系统，在电荷泵中设计了结构简单的电流单元用于补偿额外的参数变化，并采用线性压控增益的 VCO 来减小参数的变化. 最后设计了一个分辨率为 250kHz，频率范围为 1～1.05GHz 的集成频率综合器来验证上述的分析和设计方法.

关键词：频率综合器；闭环三阶 s 域；环路参数；PVT 变化；稳定性；变化裕量

EEACC：1205；2570D

中图分类号：TN4　　**文献标识码**：A　　**文章编号**：0253-4177(2005)08-1524-08

* 上海市科学技术委员会 2003 年度集成电路设计科技专项(批准号：037062019)和上海应用材料研究与发展基金(批准号：0425)资助项目

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2004-11-25 收到，2005-03-13 定稿