A 2.4GHz CMOS Monolithic Transceiver Front-End for IEEE 802.11b Wireless LAN Applications *

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Abstract: A 2.4GHz CMOS monolithic transceiver front-end for IEEE 802.11b wireless LAN applications is presented. The receiver and transmitter are both of superheterodyne structure for good system performance. The front-end consists of five blocks: low noise amplifier, down-converter, up-converter, pre-amplifier, and LO buffer. Their input/output impedance are all on-chip matched to 50Ω except the down-converter which has open-drain outputs. The transceiver RF front-end has been implemented in a 0.18μm CMOS process. When the LNA and the down-converter are directly connected, the measured noise figure is 5.2dB, the measured available power gain 12.5dB, the input 1dB compression point -18dBm, and the third-order input intercept point -7dBm. The receiver front-end draws 13.6mA currents from the 1.8V power supply. When the up-converter and pre-amplifier are directly connected, the measured noise figure is 12.4dB, the power gain is 23.8dB, the output 1dB compression point is 1.5dBm, and the third-order output intercept point is 16dBm. The transmitter consumes 27.6mA current from the 1.8V power supply.

Key words: wireless transceiver; RF; CMOS; LNA; mixer; preamplifier
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1 Introduction

Many novel telecommunication applications have recently emerged in the consumer market. One example is wireless local area networks (WLAN's) in the 2.4GHz range, which can potentially serve as high-speed links with 1 to 55 Mbits data rates for office buildings, hospitals, factories, etc. IEEE 802.11b standard is the most prevalent due to its flexibility and reconfigurability in the 2.4GHz WLAN. The standard is not very stringent and can be realized in various integrated circuit (IC) processes[1]. Although many mature products have emerged in this field, they are all implemented by a SiGe process. This makes the cost high, and more importantly, the products can not be integrated with the base-band digital processor to implement a single chip transceiver. Since the cost is the only obstacle for WLAN transceiver to propagate in the market, the CMOS process must be used for the final single chip transceiver.

This paper presents a 2.4GHz transceiver front-end in CMOS process for IEEE 802.11b WLAN applications. Four crucial blocks (LNA, down-converter, up-converter, and pre-amplifier) are all discussed. The measured results are given to show that the integrated transceiver in CMOS process is feasible for IEEE 802.11b WLAN applications.

2 Design implementations

The transceiver uses the traditional superhete-

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rodyne structure for good system performance[2]. Figure 1 shows its front-end block diagram. The transceiver consists of LNA, down-converter, up-converter, preamplifier, LO buffer, and two off-chip SAW filters. Their input/output impedance are all on-chip matched to 50 Ω except the down-converter which has open-drain outputs. The LNA is to amplify the weak signal while introducing little noise. It has high/low gain modes to adapt the signal strength change. Since the IEEE 802.11b only requires the noise figure of a receiver less than 8.6dB[1], it is not difficult to implement in CMOS process. In addition, the LNA is not required to have very low noise at the expense of low linearity, low integrity, and worse impedance matching, So the attention is placed in the on-chip impedance matching and high linearity with reasonable power consumption instead of low noise. The down-converter is to convert the 2.4GHz signal to an IF signal and the up-converter converts the IF signal to a 2.4GHz RF signal. The mixed products are filtered by the SAW filters and the pure needed signal is processed further. The preamplifier is to amplify the converted RF signal from the up-converter and can be used as the driver stage of the off-chip power amplifier (PA). The LO buffers are also integrated with the converters to relax the requirements on the external VCO.

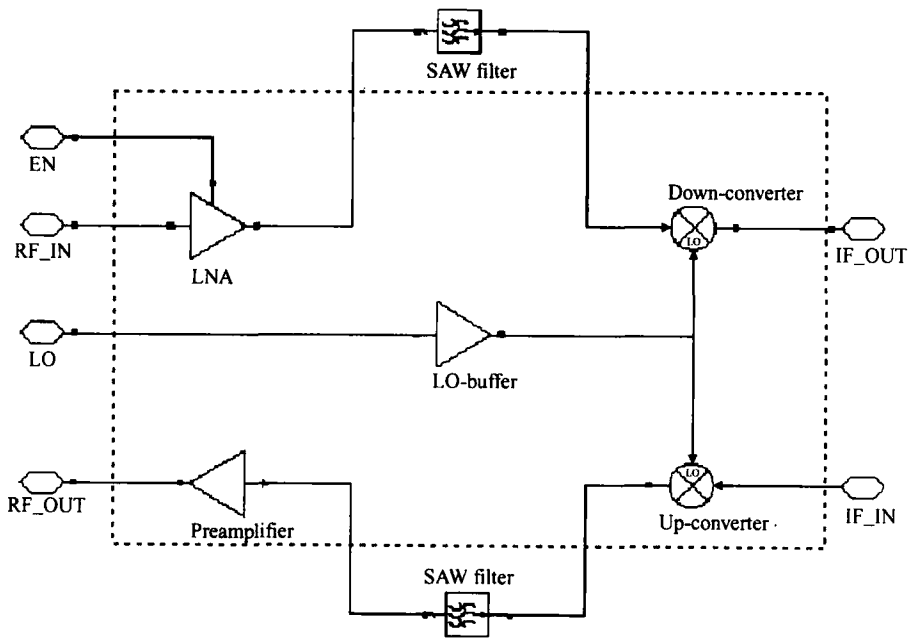

Fig. 1 Block diagram of the 2.4GHz WLAN transceiver front-end

2.1 LNA

The LNA schematic is shown in Fig. 2. EN is the gain mode selection signal to select the LNA gain. If EN is set to ground, the LNA works in high gain mode. Otherwise, if EN is set to V_{DD}, the LNA works in low gain mode which is used in case of strong input signals. The performance is optimized for high gain mode since it is the most used.

In high mode, the LNA is a two-stage structure. The input stage is an inductively degenerated common-source common-gate cascode configuration with LC tuned load. The transistor M1 has an overall effect on the noise performance of the LNA. Its size and bias condition must be optimized under limited power consumption. According to Ref. [3], the width of the optimum device should satisfy the following formula:

$$W_{optP} = \frac{3}{2} \times \frac{1}{\omega L C_{ox} R_s Q_{sP}} \approx \frac{1}{3\omega L C_{ox} R_s}$$

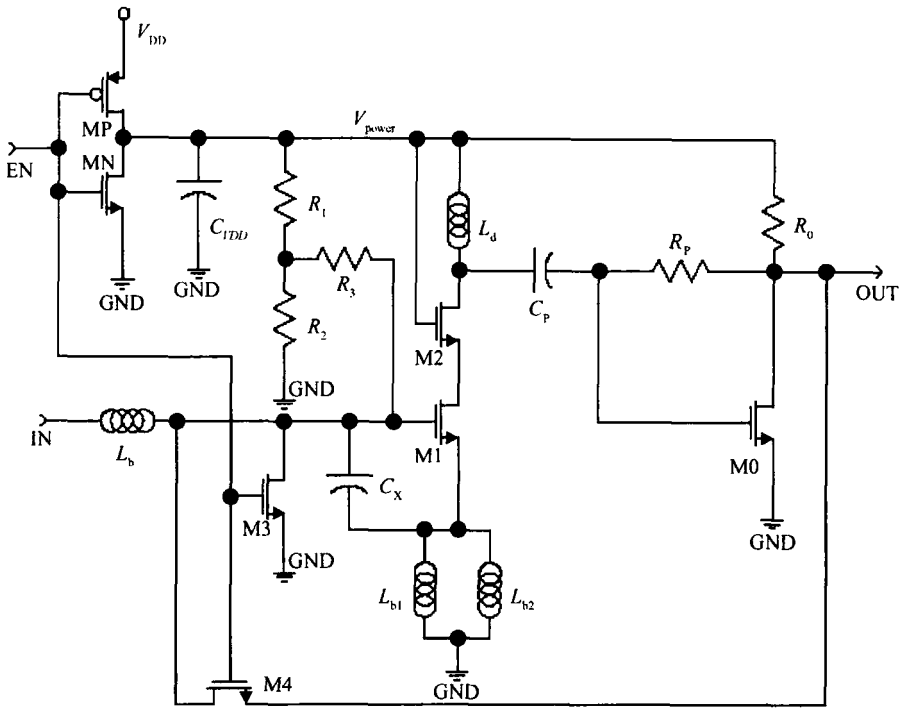

Fig. 2　Schematic of the low noise amplifier

where ω is the operation frequency, L is the device minimum channel length the process allowed, R_s is the source impedance (for most cases), C_{ox} is the capacitance per unit area, and Q_{sp} is a function of C_{gs} (gate-source capacitance).

The input impedance matching circuit utilizes three on-chip spiral inductors, and the quality factor of the degenerated inductor is approximately 9 at 2. 4GHz, but the quality factor of the series inductor L_g is approximately 6. The low quality factor inductors limit the noise performance of LNA. If the loss of L_g could be represented by the series resistors R, $R = \omega L_g / Q \approx 18\Omega$, only the loss would contribute NF by 1. 35dB. In practice, the loss of the inductors limits the noise performance of LNA.

Since only limited discrete inductor models are gotten, two same inductors are shunted to get the expected source-degenerated inductance. This will induce some additional noise since the low quality factor inductor produces noise. The parallel inductors will be replaced by only one inductor after obtaining the accurate inductor model with expected inductance from which it can be expected that the LNA performance would be improved further.

C_x is an on-chip capacitor that improves the LNA linearity. The cascode transistor M2 is used to suppress the parasitic influence of the Miller capacitance of M1 and to increase reverse isolation. The bias is simply set to V_{power} since M2 has little effect on the LNA performance. The bias of M1 is provided by a resistor divider network in which the resistance is large enough to reduce the thermal noise.

The output stage is a shunt feedback transimpedance amplifier (resistors R_p, R_0, and transistor M_0). This is the most commonly used method to realize the broadband output impedance matching while keeping high output linearity[4~7]. The loop gain of the shunt feedback transimpedance amplifier is

$$A_V = \frac{V_{out}}{V_{in}} = \frac{R_L - g_m R_p R_L}{R_L + R_p}$$

where g_m is the transconductance of the transistor M0, R_L is the parallel combination of the output impedance of M0, the resistance R_0, and the input impedance of the off-chip next stage.

The input impedance of the transimpedance amplifier is

$$R_{in} = \frac{R_p}{1 - A_V}$$

If we assume the transconductance of the input stage is G_m and the inductor L_d resonates with the node capacitance at 2.4GHz, the overall gain of the LNA will be $G_m(R_{in} /\!/ R_{L_d})A_V$, where R_{L_d} is the parasitic shunt resistance of the inductor L_d.

The output impedance of the LNA is

$$R_{out} = \frac{R_p + R_{L_d}}{1 + g_m R_{L_d}} /\!/ R_0 /\!/ r_o$$

where r_o is the output impedance of $M0$. R_{out} must be adjusted to 50Ω for output impedance matching.

C_p is an on-chip AC-coupled capacitance to isolate the bias of M0 from the input stage. And the bias of M0 could be adjusted by the resistance R_0.

In low gain mode, the LNA is only a switch and introduces some loss to the strong input RF signals. All DC paths are completely cut-off to lower the power consumption in low gain mode. This is similar to Refs. [6,7].

2.2 Down-converter

The down-converter is the last stage in the receiver front-end. As Reference [8] shows, the last stage in the chain tends to contribute the most to the distortion and it is important to end the chain with a block with high linearity. So the down-converter should have high linearity. Moreover, input impedance matching and low noise figure are required. So the class-AB single-ended input double balanced mixer is used. The mixer is derived from the BJT Micromixer[9] and was first proposed by Orasatti and Huang[6,7]. But in the original form, the bias is provided by the off-chip voltage source[6,7]. Here the on-chip bias is used to improve the symmetry of the mixer as the following discussion.

The schematic of the down-converter is shown in Fig. 3. The g_m of M2 is set to 20mS to realize the wide-band input impedance matching. To maintain the symmetry, the M3 must work in the same state as the M2. The loop consisting of M1, M2, MN1, and MN2 could realize the function. Assume that the sizes of M1 and M2, MN1 and MN2 are respectively the same, the gate-source voltage of M3 will be equal to the gate-source M2 according to translinear principle[10]. This will make M2 and M3 work in the same state and the symmetry is improved compared to the off-chip bias. C_1 and C_2 are the filtered capacitors to reduce the noise induced by the bias circuit. L_1 and L_2 are off-chip choke inductors to provide the DC current for the mixer core. The off-chip converter consists of a LC matching network and differential-single end converter. The on-chip LO buffer is for enhancing the LO driving ability and to reduce the conversion loss of the switch pairs M4～M7. The size of the M4～M7 is optimized for the best noise performance.

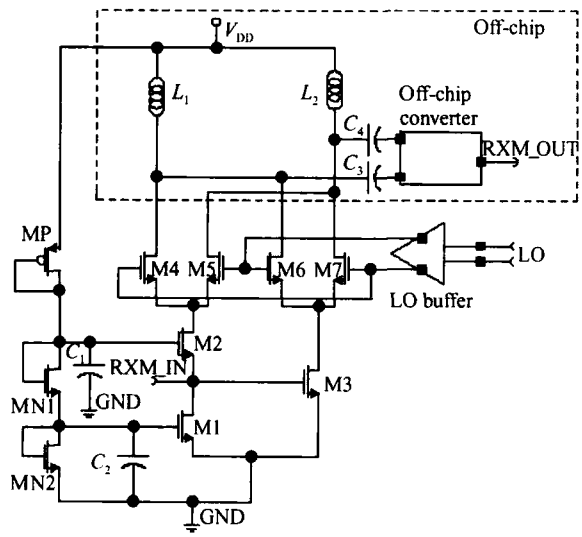

Fig. 3 Schematic of the down-converter

2.3 Up-converter

The up-converter is the first stage of the transmitter front-end. The requirement for the noise figure and linearity is loose compared to that of the down-converter. But the on-chip input/output impedance matching should be realized to reduce the cost of the transmitter system. The presented up-converter is the Gilbert cell multiplier[11] with on-chip input-output impedance matching. Figure 4 shows its schematic.

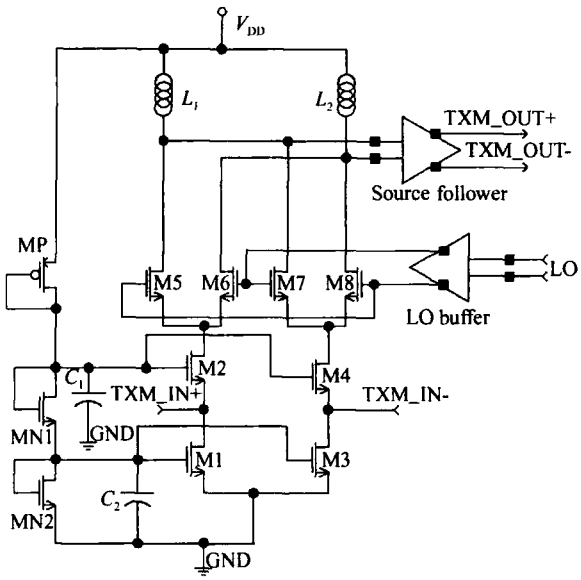

Fig. 4　Schematic of the up-converter

The input stage is a common-gate configuration in which the g_m of M2 and M4 are set to 20mS. The configuration has the advantage that the input impedance matching is realized without any off-chip components. Its bias is provided by the on-chip bias network (MP, MN1, and MN2). C_1 and C_2 are the filtering capacitors to reduce the noise induced by the bias network.

The input IF voltage signals are converted into current signals by the input stage. Then the frequency translation is performed by the commutating switched M5～M8. Since the conversion gain is the conversion transconductance multiplied by the load, the load must be large enough to attain a large conversion gain which is necessary to compress the noise contribution from the following stages. Here we utilize the on-chip LC tuned tank as the load of the converter.

The source follower is added to realize the on-chip 50Ω output impedance matching.

Since the size of the commutating switches has a significant effect on the performance of the converter, the optimization must be performed. The final switch sizes are 130μm ×0. 18μm.

2. 4　Preamplifier

The preamplifier drives the off-chip power amplifier (PA), and its output power must be higher than 1dBm. Since the efficiency is not as critical as the PA, the class-A preamplifier with input/output matching is suitable[6,7]. The schematic is shown in Fig. 5. This is a two-stage class-A implementation. The input stage and its bias network are similar to the LNA. As References [6, 7] show, the M1 should work in overdrive state due to the relatively high input level. The cascode transmitter has been cutoff to ensure that M1 stays in saturation. The on-chip LC resonator is used to improve the available power gain. The source degeneration inductor is provided by the bondwire since the inductance is only 1. 6nH. The shunt capacitance is chosen relatively large to improve the linearity of the first stage and to maintain the source degeneration inductance feasibility.

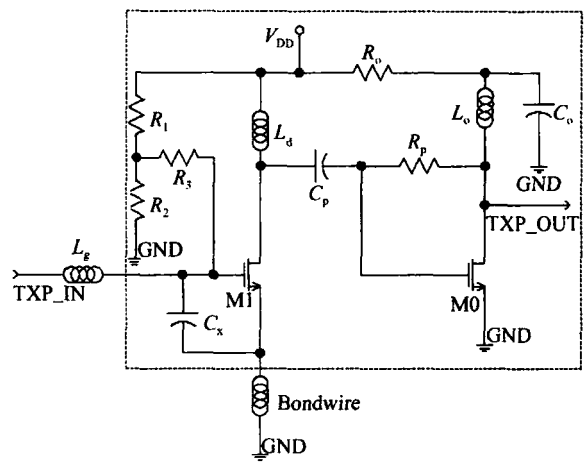

Fig. 5　Schematic of the preamplifier

The output stage is a transimpedance amplifier with a LC resonator which is proposed by Huang, Orsatti, and Piazza[6,7]. The R_0 is relatively small to enhance the drive capability of the output stage. Since the small R_0 makes the high gain very difficult to achieve, the on-chip LC resonator is inserted. It resonates at 2. 4GHz and provides high load impedance. Same as the LNA, the output transimpedance amplifier is self-biased and has an output impedance of 50Ω.

3 Results

The transceiver front-end has been implemented in 0.18μm CMOS process to verify the performance. Figure 6 shows its microphotograph, the die size is 3.4mm^2, most of which is occupied by on-chip spiral inductors. The die shape is not the standard rectangle since the whole die includes many other projects.

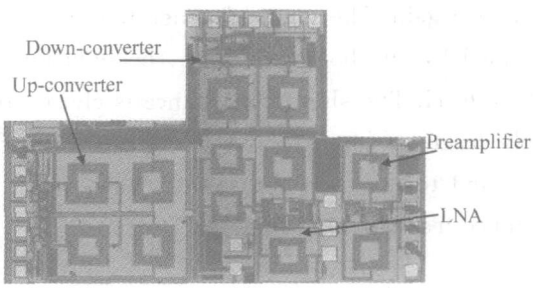

Fig. 6 Microphotograph of the transceiver front-end

The bare die is directly bonded on a printed circuit board with needed external components mounted on it to measure the circuit performance. The measurements have been performed on the individual blocks as well as the complete receiver/transmitter front-end. The SMA connectors, cables, and PCB introduce extra loss. The results given below are calibrated to eliminate their effects.

Figure 7 shows the measured gain and noise figure of the LNA in high gain mode using Agilent N8973A NFA series noise figure analyzer. When operating frequency is 2.40GHz, the power gain is 12dB with a noise figure 4.0dB. At a frequency of 2.25GHz the power gain is 12.9dB with a noise figure 3.5dB. Figure 7 shows the resonant frequency point has some departure from the right frequency range. The reason is that the on-chip inductor model is not very accurate and the couple between the circuit and the substrate at the 2.4GHz frequency range is strong.

The measured S_{11} and S_{22} of the LNA in high gain mode in the frequency range are better than -10dB, -11dB, respectively. So the LNA has good

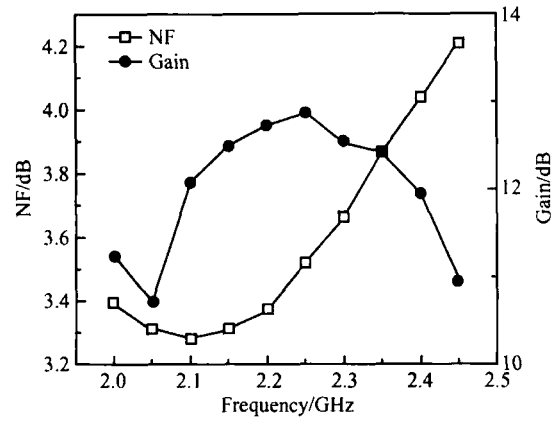

Fig. 7 Gain and noise figure of the LNA in high gain mode measured

input/output impedance matching. In the high gain mode, the measured input 1dB compression point (ICP) is -13dBm and the third-order input intercept point (IIP3) is -2dBm. The LNA in high gain mode draws a 7.94mA current from a 1.8V power supply.

The measured S_{11} of the down-converter is -16dB, the conversion gain is 1.5dB (in the resonating frequency of the IF LC matching circuit), the noise figure is 12.2dB. The down-converter has a high linearity, the measured IIP3 is 4dBm, and the input ICP is -1.5dBm. It draws 5.64mA current from a 1.8V power supply. It must be pointed out that all the measurements are done with 50Ω measurement instruments. If it applies to the system the load will be 200Ω. This will make the conversion gain improve 6dB.

Figure 8 shows the measured noise figure and the gain when the LNA and the down-converter are directly connected. The noise figure of the receiver is 5.20dB and the gain is 12.5dB at the frequency point 2.45GHz. Same as the down-converter, all the measurements are done with 50Ω measurement instruments. If it applies to the system the load will be 200Ω. This will make the conversion gain improve 6dB.

Two in-band signals are applied to the receiver at 2.420 and 2.425GHz to measure the IIP3. The measured IIP3 is shown in Fig. 9. The IIP3 is -7dBm. The measured ICP are -18dBm.

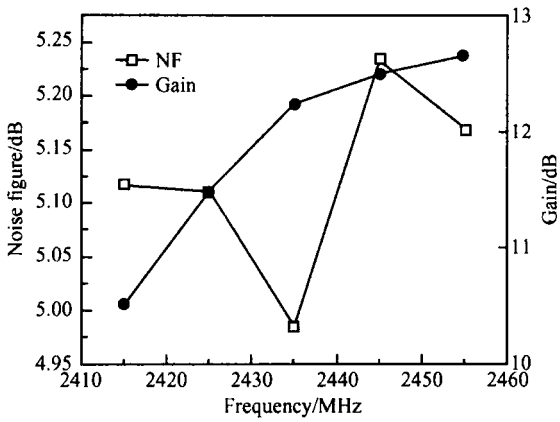

Fig. 8　Noise figure and the gain of the receiver measured

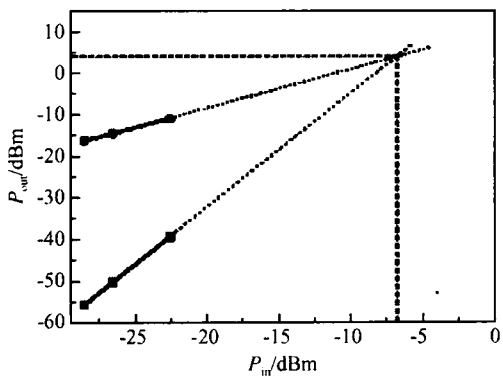

Fig. 9　IIP3 of the receiver measured

The measured parameters of the implemented LNA 's down-converter and receiver front-end are summarized in Table 1. The simulated results are also displayed in the same figure. Differences between the two are due to inaccurate model, the bondwire parasitic inductors, and the PCB loss.

The measured S_{21} parameter of the preamplifier is shown in Fig. 10. The power gain is 18. 8dB at the frequency 2. 45GHz. The measured ICP is shown in Fig. 11. The ICP is approximately - 15dBm, which corresponds to + 2. 3dBm OCP. So the preamplifier could deliver 1. 7mW power to the 50Ω load. The measured third-order output intercept point (OIP3) is 12. 3dBm. The preamplifier draws 20. 2mA current from the 1. 8V power supply.

Table 1　Summary of the measured receiver performance

			Measured results	Simulated results
Receiver front-end	Gain (50Ω load)		12. 7dB (max)	
	NF(50Ω)		5. 23dB (max)	
	ICP		- 18dBm	
	IIP3		- 7dBm	
	Power cons.		13. 6mA ×1. 8V	
LNA	Gain	High gain	12dB (2. 4GHz)	18dB
		Low gain	- 11. 5dB	
	NF (50Ω)	High gain	4. 0dB (2. 4GHz)	2. 0dB
		Low gain	11. 6dB	
	ICP (High gain)		- 13dBm	- 19. 5dBm
	IIP3 (High gain)		- 2dBm	- 8. 8dBm
	S_{11} (High gain)		< - 10dB	- 36dB
	S_{22} (High gain)		< - 11dB	- 14. 7dB
	Power cons.	High gain	7. 9mA ×1. 8V	11. 8mA ×1. 8V
		Low gain	~0	
Down-converter	Conversion gain (50Ω load)		1. 5dB	2. 2dB
	NF(50Ω)		12. 2dB	10. 8dB
	ICP		- 1. 5dBm	- 4. 3dBm
	IIP3		2dBm	4. 5dBm
	S_{11}		- 16dB	- 16. 3dB
	Power cons.		5. 7mA ×1. 8V	6. 5mA ×1. 8V

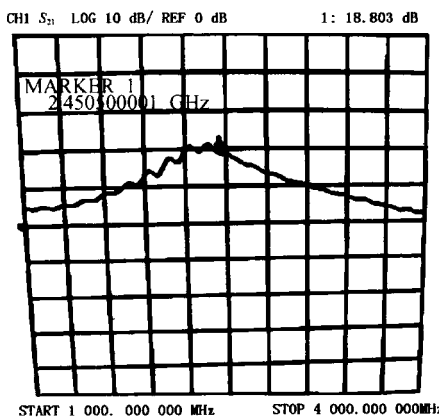

Fig. 10　S_{21} parameter of the preamplifier measured

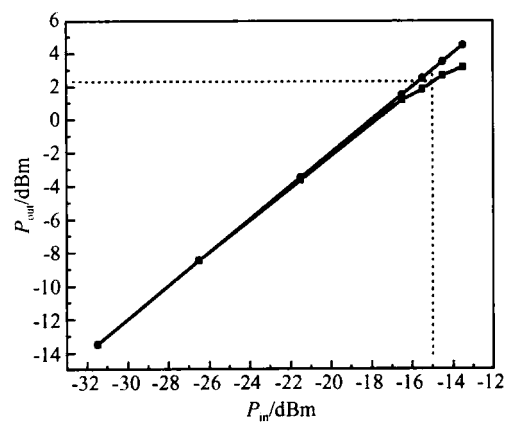

Fig. 11　ICP of the preamplifier measured

The measured conversion gain of the up-converter is 3.9dB with a noise figure 12dB. The measured IIP3 is -5.8dBm and the ICP is -12.5dBm. It draws 7.4mA current from a 1.8V power supply. The input/output impedance of the up-converter are on-chip matched to 50Ω without any external components, and the measured S_{11} and S_{22} parameters are 11.8, 11.9dB, respectively. When the up-converter and the preamplifier are directly connected, the measured noise figure and the gain are 12.4, 23.8dB, respectively. The measured OCP is +1.5dBm and the OIP3 is +16dBm. The transmitter consumes 27.6mA current with a 1.8V power supply. Table 2 summaries the performance of the transmitter front-end. The simulated results are also shown in the same figure, and the differences are due to inaccurate model, the bondwire parasitic inductors, and the PCB loss.

Table 2 Summary of the measured transmitter performance

		Measured results	Simulated results
Transmitter front-end	Output power (ICP)	1.5dBm	
	Gain	23.8dB	
	Noise figure	12.4dB	
	OIP3	16dBm	
	Power cons.	27.6mA ×1.8V	
Preamplifier	Output power (ICP)	2.3dBm	2.4dBm
	Gain	18.8dB	19.8dB
	Noise figure	2.8dB	1.4dB
	OIP3	12.3dBm	12dBm
	Power cons.	20.2mA ×1.8V	26.8mA ×1.8V
Up-converter	Conversion gain	3.9dB	8.8dB
	Noise figure	12dB	9.2dB
	ICP	-12.5dBm	
	IIP3	-5.8dBm	-7.4dBm
	S_{11}	-11.8dB	-23.7dB
	S_{22}	-11.9dB	-20dB
	Power cons.	7.4mA ×1.8V	10.1mA ×1.8V

4 Conclusion

This paper presents a 2.4GHz CMOS monolithic transceiver front-end for IEEE 802.11b wireless LAN applications. The front-end includes five crucial blocks: LNA, down-converter, up-converter, preamplifier, and LO buffer. Their input/output impedance are all on-chip matched to 50Ω except the down-converter which has open-drain outputs. The circuits have been implemented in 0.18μm CMOS process. The measured results show that the deep sub-micrometer CMOS is capable of providing the performance required by IEEE 802.11b WLAN standards. Moreover, the power consumption of the transceiver is low compared to other implementations as the receiver front-end consumes 13.6mA current and the transmitter front-end consumes 27.6mA current with a 1.8V power supply.

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应用于 IEEE 802.11b 无线局域网系统的 2.4GHz CMOS 单片收发机射频前端*

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摘要：实现了一个应用于 IEEE 802.11b 无线局域网系统的 2.4GHz CMOS 单片收发机射频前端，它的接收机和发射机都采用了性能优良的超外差结构. 该射频前端由五个模块组成：低噪声放大器、下变频器、上变频器、末前级和 LO 缓冲器. 除了下变频器的输出采用了开漏级输出外，各模块的输入、输出端都在片匹配到 50Ω. 该射频前端已经采用 0.18μm CMOS 工艺实现. 当低噪声放大器和下变频器直接级联时，测量到的噪声系数约为 5.2dB，功率增益为 12.5dB，输入 1dB 压缩点约为 -18dBm，输入三阶交调点约为 -7dBm. 当上变频器和末前级直接级联时，测量到的噪声系数约为 12.4dB，功率增益约为 23.8dB，输出 1dB 压缩点约为 1.5dBm，输出三阶交调点约为 16dBm. 接收机射频前端和发射机射频前端都采用 1.8V 电源，消耗的电流分别为 13.6 和 27.6mA.

关键词：无线收发机；射频；CMOS；低噪声放大器；混频器；末前级

EEACC：1265B；2570D；C5120

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