Fabrication and Simulation of Silicon-on-Insulator Structure with Si_3N_4 as a Buried Insulator *

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Abstract : In order to minimize the self-heating effect of the classic SOI devices ,SOI structures with Si_3N_4 film as a buried insulator (SOSN) are successfully formed using epitaxial layer transfer technology for the first time. The new SOI structures are investigated with high-resolution cross-sectional transmission electron microscopy and spreading resistance profile. Experiment results show that the buried Si_3N_4 layer is amorphous and the new SOI material has good structural and electrical properties. The output current characteristics and temperature distribution are simulated and compared to those of standard SOI MOSFETs. Furthermore ,the channel temperature and negative differential resistance are reduced during high-temperature operation ,suggesting that SOSN can effectively mitigate the self-heating penalty. The new SOI device has been verified in two-dimensional device simulation and indicated that the new structures can reduce device self-heating and increase drain current of the SOI MOSFET.

Key words : Si_3N_4 ; new SOI structures ; self-heating effects
PACC : 7300 ; 7360J **EEACC :** 4250
CLC number : TN386 **Document code : A** **Article ID :** 0253-4177(2005)09-1722-05

1 Introduction

Silicon-on-insulator (SOI) materials offer several advantages as compared to bulk silicon[1]. However ,due to the poor thermal conductivity of the buried oxide layer and self-heating effect in SOI devices ,the applicability of SOI materials is limited[2,3]. Replacement of the buried silicon dioxide by a better thermal conductor could adequately minimize this effect[4~6]. The thermal conductivity of the silicon nitride (30W/m℃) is almost twenty times higher than that of SiO_2 (1.4W/m℃). In addition ,the physical and chemical properties (such as low etching rate in HF solution) and the good structural quality (100mm wafer without defect) of the Si_3N_4 layer lead to the assumption that Si_3N_4 film is a good candidate for a buried insulator of SOI structures.

Separation by implanted nitrogen (SIMNI) has been adopted to form new SOI structures[7] , however ,there are two disadvantages :first ,the excess nitrogen at the peak of distribution tend to be trapped-out as nitrogen bubbles because of the low diffusivity of nitrogen in nitrogen-rich silicon ; second ,the buried nitride structures have their own problems ,in particular ,due to crystallization of the nitride[8,9]. This leads to either a leaky dielectric or

* Project supported by the National High Technology Research and Development Program of China (Nos. 2003AA302720 ,2004AA302G20) and the Program of Shanghai Nanotechnology Promotion Center (No. 0352nm016)

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Received 19 February 2005 ,revised manuscript received 6 April 2005

gross mechanical failure depending on the implanted dose and annealing conditions. In this work, we have grown high quality monocrystalline silicon on porous silicon using ultra-high vacuum electron beam evaporation. SOI structures with Si_3N_4 as a buried insulator were successfully produced by bonding and etching the remnant porous silicon. The physical and electrical properties of the formed SOI structures were characterized. The new SOI structures are simulated using a two-dimensional simulation program to examine the device temperature distribution and change of terminal current due to self-heating.

2 Experiment and simulation

In the first step 75mm (100) CZ silicon were used, on top of which Si_3N_4 layers approximately 80nm thick were deposited by low-pressure chemical-vapor deposition (LPCVD) at the temperature of 800 ℃.

75mm boron-doped p-Si (100) wafers with a resistivity of 0.003～0.007Ω·cm were anodized in the electrolyte HF∶ethanol = 1∶1 at 4mA/cm^2 to form porous silicon. The single-crystal silicon was then epitaxially grown on porous silicon in an ultra-high vacuum electron beam evaporator with a base vacuum of approximately 10^{-7} Pa. After the epitaxial layer was formed, the wafer was bonded together with a handle wafer deposited with Si_3N_4 films at room temperature. Then the bonded wafer was annealed at 1100 ℃ for 1h in N_2 ambient to increase the bonding strength. Subsequently, the bonded wafers were split into two parts along the porous silicon layer. Finally, the porous silicon was etched away in a diluted HF solution and the final SOI structures were obtained.

In the second step the self-heating effect was addressed by comparing the electrical characteristics and thermal distribution of SOI and SOSN MOSFETS unsing numerical simulation. The analysis was performed using a two-dimensional device simulator called Silvico Atlas running on a SUN workstation.

3 Results and discussion

Our investigation in this paper involves the measuring of structural and electrical properties and the simulation of the output characteristics and temperature distribution.

3.1 Structure

Figure 1(a) shows the cross-sectional transmission electron microscopy (XTEM) images of the SOI structures. The top silicon layer and the buried Si_3N_4 have thickness of 200nm and 80nm respectively in Fig. 1(a). Both the upper and lower interfaces are very flat and steep. These figures show that the interfaces of the SOI structures are

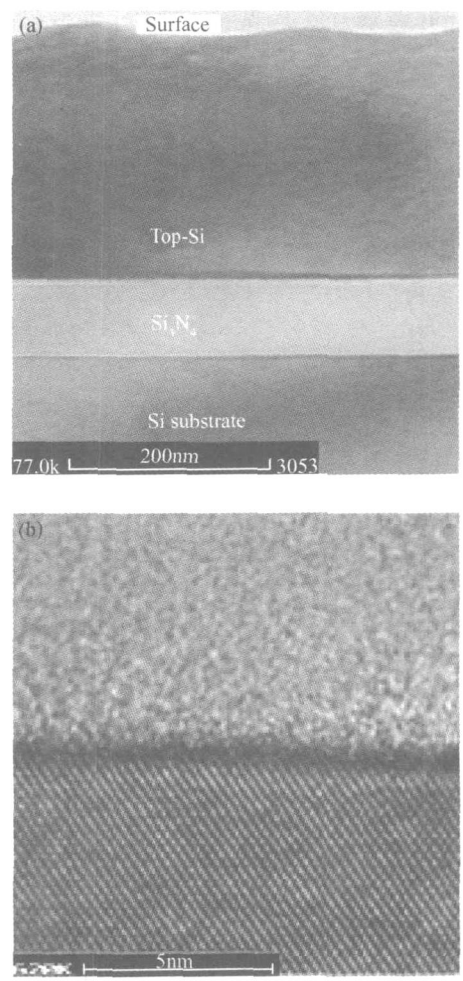

Fig. 1　XTEM image (a) and HRTEM image (b) of the new SOI structures

perfect. From Fig. 1(b), it also can be seen that the buried Si_3N_4 layer is amorphous, and neither voids nor bubbles are detected. It is known that the crystalline quality of the top silicon is very important to SOI materials. These results confirm that the top silicon has almost the same crystalline quality as the substrate silicon.

3.2 Electrical properties

The spreading resistance profile of the SOI sample was measured and the experimental results are shown in Fig. 2. Three layers of the SOI structures including the top silicon, buried Si_3N_4, and silicon substrate can be clearly distinguished. The thickness values of the top silicon and the buried Si_3N_4 shown in this figure are in good agreement with the XTEM results. The very steep slope from top silicon to buried Si_3N_4 at the depth of 210nm in the spreading resistance profile implies sharp interface between the two. The values of spreading resistance show that the top silicon has uniform electrical property and the buried Si_3N_4 layer has very good insulating performance.

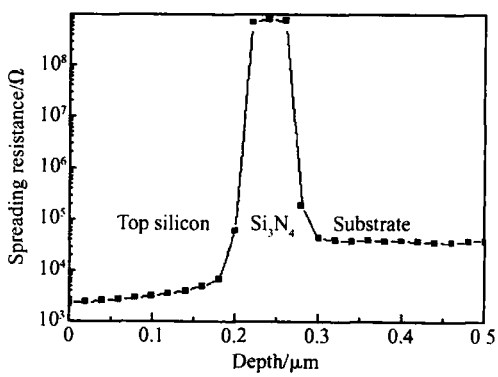

Fig. 2 Spreading resistance profile of the SOI structures

3.3 Output characteristics simulation

In our simulation, two sets of curves are generated for the cases with and without lattice temperature effects. In order to use Atlas to solve these questions a MOS device structure is needed. The details of the relevant geometrical and technological parameters are as follows: Figure 3 shows the structure distribution of the MOSFET device. The device has a $1 \times 10^{16}\ cm^{-3}$ p-type substrate doped and n-type source and drain doping of $2 \times 10^{20}\ cm^{-3}$. The channel effective length is 0.25μm, and the thicknesses of the gate oxide, top silicon, and buried Si_3N_4 are 20, 200, and 100nm, respectively. The geometrical and technological parameters of these devices are identical except for the buried insulator.

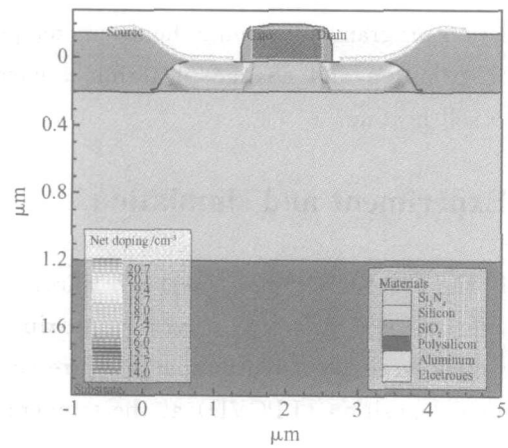

Fig. 3 Structure distribution of the MOSFET device

In this simulation the gate bias is held at 10V because the self-heating effect will be more apparent when the power is high. The drain bias is ramped up from 0 to 5V. In the device modeling the temperature rise due to self-heating can be approximated by rI_dV_{ds} where r is the thermal resistance. The simulation results are shown in Fig. 4. The SOI device shows strong negative differential resistance (NDR) when the self-heating effect is con-

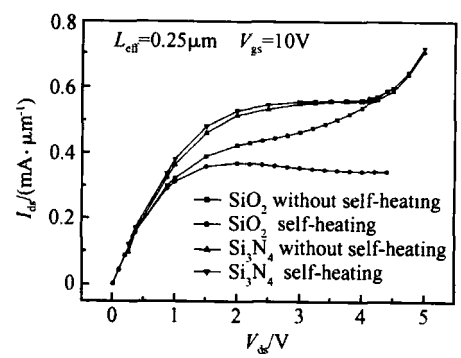

Fig. 4 Simulated output characteristics of SOI and SOSN devices

sidered, however, the SOSN displays weak NDR under the same conditions. It is known that the higher the self-heating effect the more apparent NDR becomes. Thus we examine the self-heating effect by studying the NDR on the curves. It can be concluded that the SOI device is subject to a higher self-heating effect than that of SOSN under the same operating conditions.

3.4 Temperature distribution simulation

The temperature distribution obtained under the same simulation conditions is consistent with the output characteristics. Figure 5(a) exhibits the two-dimensional (2D) temperature distribution of the SOI device. Figure 5(b) exhibits the 2D temperature distribution of the SOSN MOSFET. The temperature in the SOI's substrate is only 300 K,

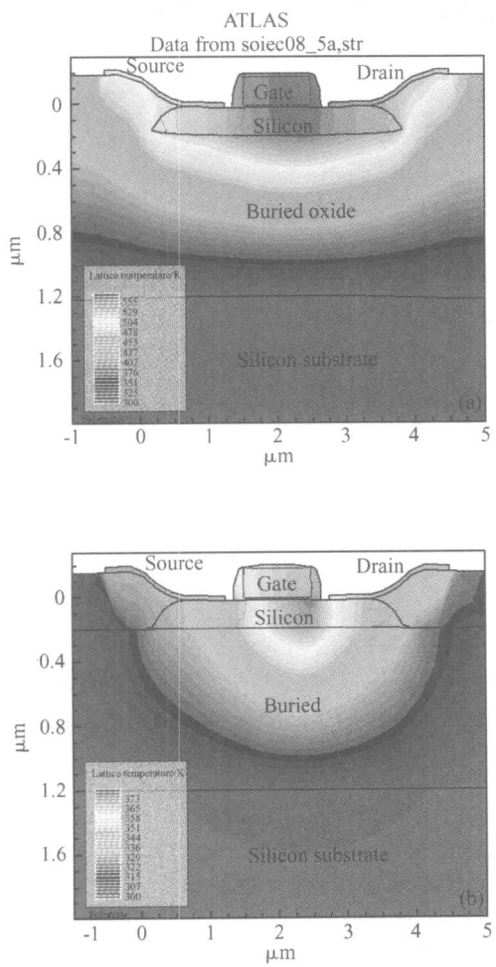

Fig. 5　Simulated temperature distributions of SOI (a) and SOSN (b) devices

but because of self-heating the channel temperature rises to 555 K. The temperature distribution pattern in the SOSN is displayed in Fig. 5(b). The channel temperature in the device decreases significantly to 373 K compared with 555 K in the SOI device, and it is only slightly higher than the substrate temperature. Our results indicate that the influence of self-heating effect in SOI is much more serious than in SOSN. The same conclusion can be drawn based on the aforementioned output characteristics simulation.

4 Conclusion

SOI structures with Si_3N_4 as buried insulating film have been successfully fabricated using epitaxial layer transfer technology. Experimental results show the formed SOI sample has good structural and electrical properties. Furthermore, the channel temperature and NDR in the SOSN devices are reduced suggesting that SOSN can effectively mitigate the self-heating penalty. The new SOI structures can achieve a significant decreased the self-heating effect.

References

[1] Yamaguchi H, Hmi H, Fujino S, et al. Intelligent power IC with partial SOI structure. Jpn J Appl Phys, 1995, 34: 864

[2] Arnod E, Pein H, Herko S P. Comparison of self-heating effects in bulk-silicon and SOI high-voltage devices. Proc IEDM, 1994: 813

[3] Merchant S, Arnold E, Baumgart, et al. Dependence of breakdown voltage on drift length and buried oxide thickness is SOI RESURF LDMOS transistor. Proc 5th ISPSD, 1993: 124

[4] Xie Xinyun, Liu Weili, Men Chuanling, et al. Fabrication of silicon-on-insulator structure with Si_3N_4 as buried insulating films by epitaxial layer transfer. Chinese Journal of Semiconductors, 2003, 24(2): 189 (in Chinese) [谢欣云, 刘卫丽, 门传玲, 等. 多孔硅外延转移技术制备以氮化硅为绝缘埋层的 SOI 新结构. 半导体学报, 2003, 24(2): 189]

[5] Zhu Shiyang, Li Aizhen, Huang Yiping. Transfer of thin epitaxial silicon film by wafer bonding and splitting of double layered porous silicon for SOI fabrication. Chinese Journal of Semiconductors, 2001, 22(12): 1501

[6] Zhu Ming, Chen Peng, Ricky K Y, et al. Numerical study of

self-heating effects of MOSFETs fabricated on SOAN substrate. IEEE Trans Electron Devices ,2004 ,51(6) :901

[7] Reeson KJ. Fabrication of burried layers of SiO_2 and Si_3N_4 using ion beam synthesis. Nuclear Instruments and Methods in Physics Research B ,1987 ,19/20 :269

[8] Petruzzello J ,MeGee T F ,Frommer M H ,et al. Transmission electron microscopy and Auger electron spectroscopy of silicon-on-insulator structures prepared by high-dose implantation of nitrogen. J Appl Phys ,1985 ,58 :4605

[9] Reeson KJ ,Hemment P L F ,Meekison C D ,et al. Buried layers of silicon oxy-nitride fabricated using ion beam synthesis. Nuclear Instruments and Methods in Physics Research B ,1988 ,32 :427

以 Si_3N_4 为埋层的 SOI 结构制备与器件模拟 *

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摘要: 为了减少经典 SOI 器件的自加热效应,首次成功地用外延方法制备以 Si_3N_4 薄膜为埋层的新结构 SOSN,用 HRTEM 和 SRP 表征了 SOI 的新结构. 实验结果显示,Si_3N_4 层为非晶状态,新结构的 SOSN 具有良好的结构和电学性能. 对传统 SOI 和新结构 SOI 的 MOSFETs 输出电流的输出特性和温度分布用 TCAD 仿真软件进行了模拟. 模拟结果表明,新结构 SOSN 的 MOSFET 器件沟道温度和 NDR 效益都得到很大的降低,表明 SOSN 能够有效地克服自加热效应和提高 MOSFET 漏电流.

关键词: Si_3N_4; 新结构 SOI; 自加热效应

PACC: 7300; 7360J **EEACC**: 4250

中图分类号: TB386 **文献标识码**: A **文章编号**: 0253-4177(2005)09-1722-05

* 国家高技术研究发展计划(批准号:2003AA302720 ,2004AA302G20) 和上海纳米技术促进中心 (批准号:0352nm016) 资助项目

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2005-02-19 收到,2005-04-06 定稿