Design of Down Scalers in Mixed-Signal GHz Frequency Synthesizer

Xu Yong[1,2], Wang Zhigong[1], Qiu Yinghua[1], Li Zhiqun[1], Hu Qingsheng[1], and Min Rui[2]

(1 *Institute of RF- & OE-ICs, Southeast University, Nanjing* 210096, *China*)

(2 *Institute of Sciences, PLA University of Science and Technology, Nanjing* 211101, *China*)

Abstract: An optimized method is presented to design the down scalers in a GHz frequency synthesizer. The down scalers are comprised of dual modulus prescaler (DMP) and programmable & pulse swallow divider, different methods of high frequency analog circuit and digital logical synthesis are adopted respectively. Using a DMP high speed, lower jitter and lower power dissipation are obtained, and output frequency of 133.0MHz of the DMP working at divide-by-8 shows an RMS jitter less than 2ps. The flexibility and reusability of the programmable divider is high; its use could be extended to many complicated frequency synthesizers. By comparison, it is a better design on performance of high-frequency circuit and good design flexibility.

Key words: PLL; frequency synthesizer; dual-modulus prescaler; programmable & pulse swallow divider

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1 Introduction

One of the critical RF functions in the transceiver of a wireless LAN is the frequency synthesizer in which down scalers are used intensively. Down scalers are made of digital and analog (operating on RF frequency band) mixed-signal circuits, due to the complexity, high operation frequency, and low power dissipation. Therefore the design of the down scalers is always a challenge. The choice of the dividing architecture is therefore essential for achieving a lower power dissipation, good design flexibility, and high reusability of existing building blocks[1,2]. A modular architecture fulfils these requirements, as will be demonstrated in this paper.

In this paper a down scalers consisting of a DMP and a programmable & pulse swallow divider is designed in a mixed-signal 0.18μm CMOS technology. The former works at high operation frequencies with a lower jitter and lower power dissipation, and the latter is designed in digital logical synthesis for good reusability and high design flexibility.

2 System block of the frequency synthesizer

The block diagram of the PLL-based frequency synthesizer is shown in Fig. 1; the shaded portion indicates the down scalers section. Quarter of the VCO output is divided down in a DMP and then feed back to phase-frequency detector (PFD) through programmable & pulse swallow divider to compare the phase and the frequency. The synthesizer generates frequencies (f_{VCO}) in the range of 4.144 to 4.256GHz in a step of 16MHz. The total divide-ratio changes from 259 to 266 by the step of 1, when the reference clock frequency of phase

Xu Yong male, master, lecturer. His research work focuses on design of RFICs and mixed-signal ICs.

Wang Zhigong male, professor. His research interests include design of ultra-speed ICs, RFICs, MMICs, and OEICs.

Qiu Yinghua male, PhD candidate. His research work focuses on design of RFICs.

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locked loop (PLL) is 4MHz.

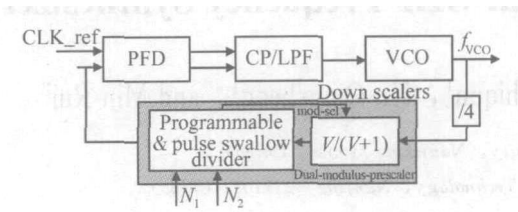

Fig. 1 Block diagram of the PLL-type frequency synthesizer

3 High speed DMP design

In the total synthesizer the DMP block operates on the high frequency band, so an RF design method is adopted. In this paper, a novel D-latch architecture integrated with 'OR' logic is presented. The implemented circuit of the DMP is shown in Fig. 2. Figure 3 shows the circuit schematic of the D-latch integrated with 'OR' logic gates. It is

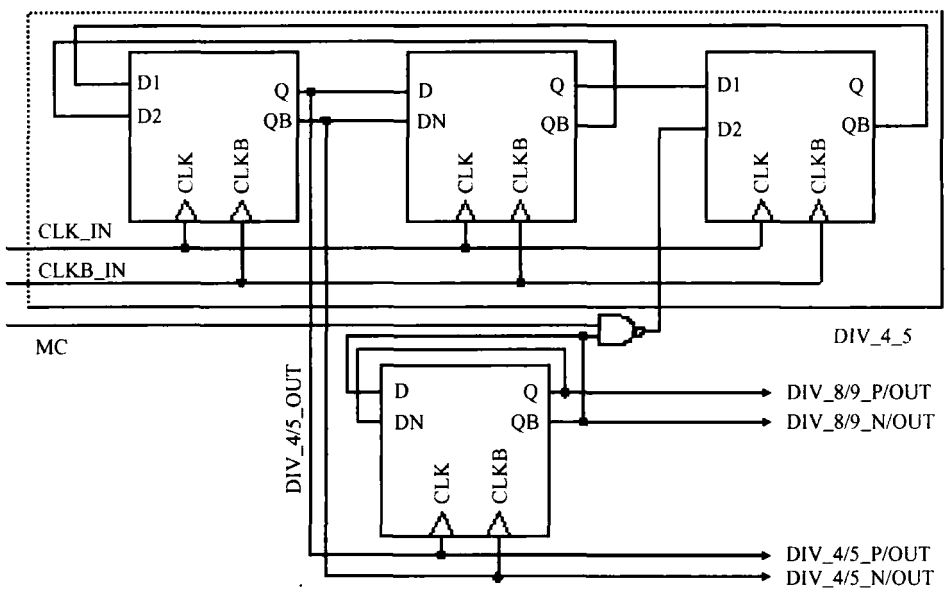

Fig. 2 Block diagram of the high speed dual-modulus prescaler

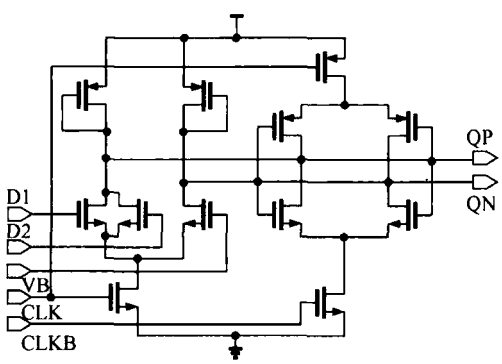

Fig. 3 D-latch architecture with 'OR' logic input

verified that this D-latch can work 20% faster than a normal D-latch[3,4].

The D-flip-flop is made of an improved master/slave SCFL D-latch. Its operation principle and advantages are introduced in detail in Ref. [4]. The primary advantage is higher speed and larger driving capacity. The measured output frequency of 133.0MHz of the DMP working at divide-by-8 shows an RMS jitter less than 2ps (given in Fig. 4 (a)), corresponding to 0.02% of the clock period. The power dissipation of the core part of the dual modulus prescaler is only 3.2mA. An excellent performance of lower jitter and lower power dissipation is achieved. The measured output waveform of the DMP working at divide-by-8 (seen in Fig. 4 (b)) would be translated into programmable & pulse swallow divider.

4 Programmable & pulse swallow divider design[5,6]

There are two counters 'A' & 'B' and a con-

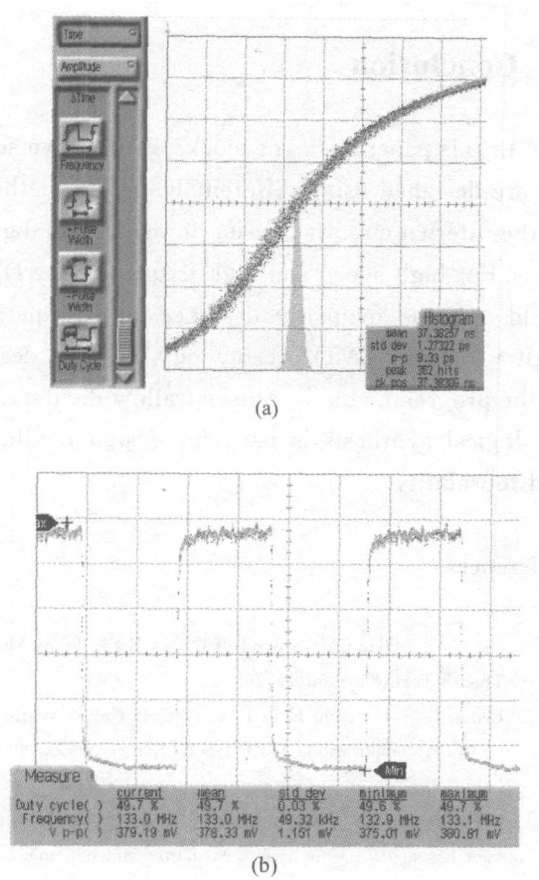

Fig. 4　Measured waveform of the high speed DMP
(a) Measured jitter waveform; (b) Output of the DMP at divide-by-8

trol block in this section. The operation of the total down scalers is as follows. N_2 and N_1 are initialized to counter 'A' & 'B', and both counters begin to count up. At first, the DMP divides the quarter of VCO frequency output by 9 until 'A' counter counts up to N_2, at this point it switches over and divides by 8 until the 'B' counter continues counting up to N_1. Then the two counters are reset and DMP switches back to divide-by-9 at the same time. The flow diagram of the down scalers behavior is shown in Fig. 5.

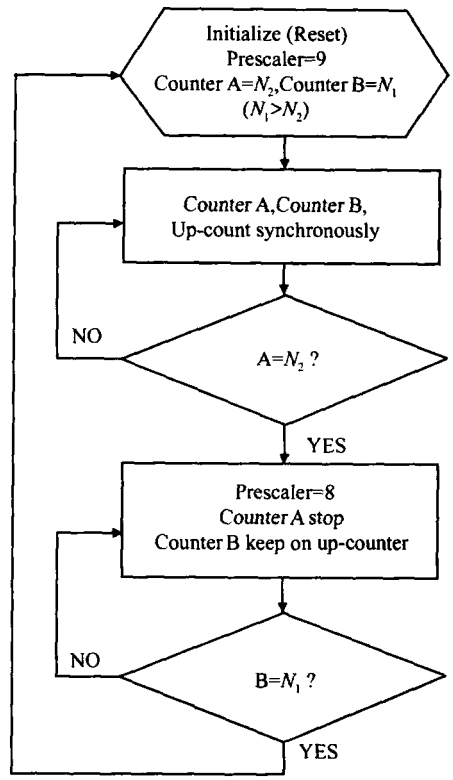

Fig. 5　Behavior flow diagram of down scalers

To get a clear picture of the function of down scalers, an example of post-simulation waveforms of 9-bits programmable divider is given in Fig. 6. There are two counters respectively loaded N_1 (h'1F) and N_2 (h'7) at the beginning. When 'mod_sel' is '1' at first, DMP works at divide-by-9 in N_2 (=7) cycles, and when 'mod_sel' is '0', DMP works at divide-by-8 in ((N_1 + 1) - N_2) (=25) cycles. So total divide-ratio of the down scalers is ((N_1 + 1) - N_2) ×8 + N_2 ×9 = 263. At this time, VCO frequency (f_{VCO}) synthesized by loop circuits

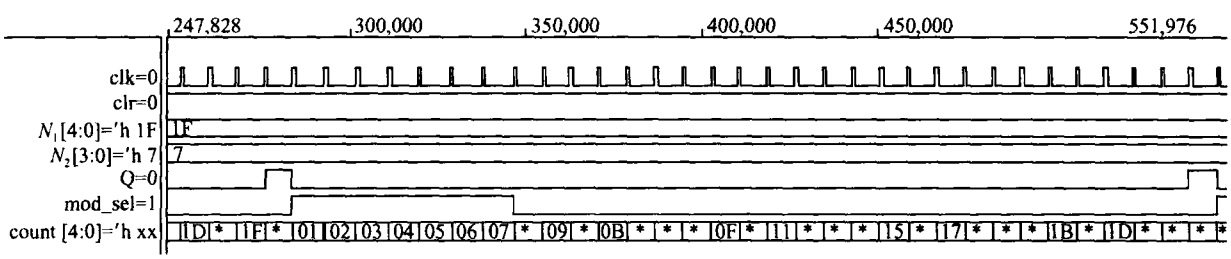

Fig. 6　Post-simulation waveforms of 9-bits programmable divider

is 4MHz ×263 ×4 = 4208MHz for 4MHz reference clock frequency. The other frequency-points needed could be synthesized by changing programmable reloaded data N_1 and N_2.

The greatest advantage of this method is better design flexibility and higher reusability. For example, its use could be extended to a frequency-hopping (FH) synthesizer with thousands of frequency-points which is difficult to manually design. On the other hand, easy optimization of power dissipation, fast design time, and simple layout work are achieved. The microphotograph of the DMP and the magnified layout of the programmable divider made from Apollo P&R is shown in Figs. 7 (a) and (b). The chip area of the DMP is 620μm ×50μm, while the programmable divider is relatively much smaller, only 50μm ×50μm.

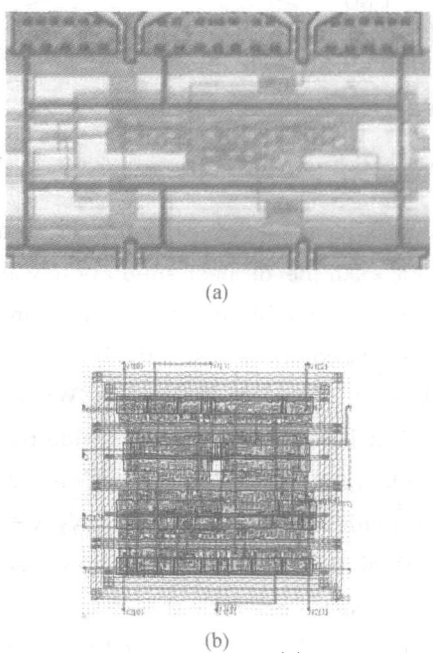

Fig. 7 Layout of down scalers (a) Microphotograph of DMP; (b) Layout of programmable & pulse swallow divider

5 Conclusion

In this paper different blocks of the down scalers are designed using different IC design methods as the internal circuits consist of analog and digital parts. For high speed and high frequency, the DMP could only be manually designed in RF method with a 0.18μm CMOS technology. For the design of the programmable & pulse swallow divider, digital logical synthesis is used for design flexibility and reusability.

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数模混合 GHz 级频率综合器下变频模块设计

徐　勇[1,2]　王志功[1]　仇应华[1]　李智群[1]　胡庆生[1]　闵　锐[2]

(1 东南大学射频与光电集成电路研究所，南京　210096)

(2 解放军理工大学理学院，南京　211101)

摘要：介绍了一种应用于 GHz 级高速频率合成器的数模混合下变频模块. 采用了高速射频双模预分频器与数字逻辑综合生成的可编程吞脉冲分频器相结合的设计方法. 双模预分频实现了高速低抖动低功耗,双模预分频器工作在除 8 状态输出 133MHz 频率时,均方差抖动小于 2ps;可编程吞脉冲分频器算法灵活、设计复用性强,该算法可以灵活运用到许多复杂频率综合系统. 相比较而言,该设计获得了更好的高频电路性能与设计复用性.

关键词：锁相环；频率综合器；双模预分频器；可编程脉冲吞吐分频器

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徐　勇　男,硕士,讲师,主要研究方向为 RFICs 和混合信号 ICs 的设计.

王志功　男,教授,博士生导师,主要研究方向为超速 ICs,RFICs,MMICs 和 OEICs 的设计.

仇应华　男,博士研究生,主要研究方向为 RFICs 的设计.

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