# A 2.4GHz Quadrature Output Frequency Synthesizer

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**Abstract:** A design and implementation for a 2.4GHz quadrature output frequency synthesizer intended for bluetooth in 0.35μm CMOS technology are presented. A differentially controlled quadrature voltage-controlled oscillator (QVCO) is employed to generate quadrature (I/Q) signals. A second-order loop filter, with a unit gain transconductance amplifier having the performance of a third-order loop filter, is exploited for low cost. The measured spot phase noise is -106.15dBc/Hz @1MHz. Close-in phase noise is less than -70dBc/Hz. The synthesizer consumes 13.5mA under a 3.3V voltage supply. The core size is 1.3mm × 0.8mm.

**Key words:** frequency synthesizer; phase locked loop; quadrature VCO; phase noise; bluetooth
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## 1 Introduction

The rapid growth of the wireless communication market has brought a large demand for high performance radio frequency (RF) transceivers. As the most important block in a transceiver, a frequency synthesizer, which can provide a clean, stable, and programmable local oscillator (LO) signal, is greatly desired to be integrated on the chip[1]. However, the noise and interference signals of other blocks in the transceiver, for example a power amplifier, will degrade the performance of the frequency synthesizer. A well-designed, differentially controlled VCO can provide relatively good immunity to such noise or interference[2,3].

For the purpose of image-rejection and sideband-rejection, quadrature signals are used. Poly phase filter is the usual circuit used to generate quadrature signals, but it entails a highly-matched layout for precise quadrature signals generation, which inevitably brings a lot of trouble in the layout design. Moreover, no gain can be obtained since the filter is passive. Another problem is that the buffer inserted between the VCO and the poly phase filter is power hungry[2]. If the frequency range is wide, several stages should be used to get enough poles and zeros, which leads to high circuit complexity. As an alternative solution, a QVCO can provide good quadrature signals in a wide frequency range. Power consumption can be reduced due to the omission of the buffer mentioned above.

The third-order loop filter is attractive for its good spurious suppression, but it brings a lot of difficulties in loop filter design. In this paper, a QVCO and the differentially controlled technique are used simultaneously in the design of a frequency synthesizer for a bluetooth transceiver. And a novel equivalent third-order loop filter is implemented by using a second-order loop filter.

## 2 Circuit design

In wireless communication, phase noise and

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spurious tones of the synthesizer will degrade the channel signal to noise ratio (SNR) and increase the bit error rate (BER) during data transmission. The adjacent channel interference signal will also deteriorate channel SNR through the sideband spectrum of the LO signal. According to the BER requirement ( < 0.1 %) of bluetooth, it's reasonable to assume that the signal to interference ratio (SIR) equals 20dB. Spot phase noise requirements of the synthesizer can be derived based on this assumption, which are listed in Table 3. An integer-N structure is preferred here for its simplicity. To provide good immune ability to the noise or interference from other blocks and substrate, differentially controlled QVCO is used in the loop. Some important loop parameters are listed in Table 1.

Table 1　Loop parameters of frequency synthesizer

| Loop parameter | Value | Sizes of loop filter | Value |
|---|---|---|---|
| Reference clock | 500kHz | *R*1 | 174kΩ * |
| Loop bandwidth | 50kHz | *C*1 | 150pF * |
| Phase margin | 48° | *C*2 | 15.5pF * |
| Current of CP | 30μA * | Input capacitance of VCO | 2.4pF * |
| VCO gain | 520MHz/V * | | |

* Differential value

### 2.1　Quadrature coupling VCO

The VCO is the most important block in a frequency synthesizer. By using two identical differential VCOs, with four couples of coupling transistors as shown in Fig. 1, quadrature output can be obtained. Large-size coupling transistors can be used to obtain precise quadrature signals, but the phase noise performance of the VCO will be worsened a lot at the same time[3]. Here the sizes of coupling transistors are selected to be equal to the sizes of negative resistance transistors. To fulfill differential tuning control, both a pMOS varactor and a nMOS varactor are used in circuit design. Two types of varactors operate in inversion mode. The immune ability to common mode noise is best only when the tuning characteristics of both types of varactors are completely identical. In fact, it is hard to be realized. However, this is not a serious problem, and the simulation shows that the difference is small.

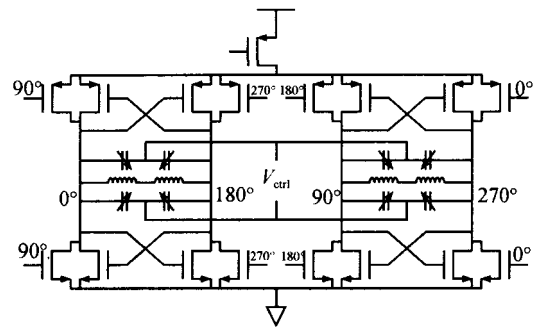



Fig. 1　Circuit diagram of QVCO

The tuning range of the VCO must cover the band from 2.4 to 2.48GHz for bluetooth. Two methods are prevailing to achieve this purpose. One is using a large varactor that can offer enough gain to cover the desired frequency range. The other is taking advantage of a digitally controlled capacitor array (DCCA) to implement the coarse-tuning first, thus allowing for fine-tuning with a smaller varactor later on. The usage of a capacitor array will deteriorate *Q*-factor of the LC tank. A large varactor with a small capacitor array is adopted here to minimize the effect of the capacitor array on the phase noise performance of the VCO.

### 2.2　Differential charge pumps

Differential charge pumps provide good rejection to common mode noise or interference, but generate more output noise. Figure 2 is the circuit diagram of the differential charge pump. A common mode feedback circuit is used to keep the common mode output of differential-control voltage at the level that can ensure the VCO working in the linear

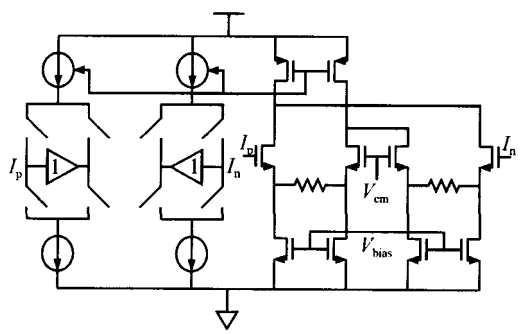



Fig. 2　Circuit diagram of differential charge pump

range of tuning curve. To enlarge the linear feedback range of the common mode feedback circuit, the degeneration resistors are inserted between the sources of the differential input transistors.

### 2.3 Loop filter

Generally, the second-order low pass filter is adopted in most PLLs because of its simplicity. The third-order low pass filter can be used for further spurious suppression, but it brings many difficulties in loop filter design. A large phase margin requires that the third pole be far away from the loop bandwidth, which will attenuate spurious suppression. So a tradeoff is taken between loop phase margin and spurious suppression in the third-order loop filter design. Furthermore, the third-order loop filter consumes more off-chip components. If the loop filter is fully integrated on chip, the large area will be occupied by capacitors used in the loop filter.

As a substituted solution of the third-order loop filter, a second-order loop filter with a unit gain transconductance amplifier is used to cut down application cost. As shown in Fig. 3, a full feedback transconductance amplifier loaded by the input capacitance of the VCO will generate a low frequency pole that can be used to filter out high frequency noise at the control line of the VCO. Using a full-feedback transconductance amplifier instead of a resistor is based on several considerations: (1) The in-band noise of a full-feedback amplifier can be suppressed by the negative feedback loop of the amplifier, which has little effect on the phase noise of synthesizer; (2) The amplifier can provide inverse isolation. Assuming that the transconductance amplifier is ideal, its transconductance is a constant $G_m$. The transfer function of this buffer loaded with the VCO's input capacitance is

$$\frac{V_{out}}{V_{in}} = \frac{1}{\frac{sC_{vco\_input}}{G_m} + 1} \tag{1}$$

As a result, the transfer function of loop filter is now

$$Z(s) = \frac{sC_1R_1 + 1}{s(sR_1C_1C_2 + C_1 + C_2)\left(s\frac{C_{vco\_input}}{G_m} + 1\right)} \tag{2}$$

The third pole is determined only by the transconductance of the amplifier and input capacitance of the VCO. This simplifies the loop filter design compared to a traditional passive third-order loop filter, because the position of the third pole is determined by the values of all the components in a traditional third-order loop filter. It should be mentioned that the input capacitance of the VCO varies about $\pm 10\%$ along the whole tuning range. Meanwhile, considering process variation, enough margins should be kept to make sure that the third pole will never lead the whole loop to be unstable. There is often a forth pole introduced by the transconductance amplifier, which will further degrade the phase margin of the whole loop, assuming that transconductance amplifier has two poles. In general, the first pole is near to the origin and is far away from the unit-gain bandwidth, which provides 90° phase shift. The second pole determines the phase margin of the amplifier:

$$\phi_G = 90^\circ - \arctan\left(\frac{\omega_{unit}}{\omega_2}\right) \tag{3}$$

where $\omega_{unit}$ is the unit gain bandwidth of the amplifier, and $\phi_G$ is the phase margin of the amplifier. Based on Eq. (3), the phase margin of loop can be written as

$$\phi = \arctan\left(\frac{\omega}{\omega_1}\right) - \arctan\left(\frac{\omega}{\omega_2}\right) - \arctan\left(\frac{\omega}{\omega_{unit}}\right) - \arctan\left(\frac{\omega}{\omega_{unit}\tan(\phi_G)}\right) \tag{4}$$

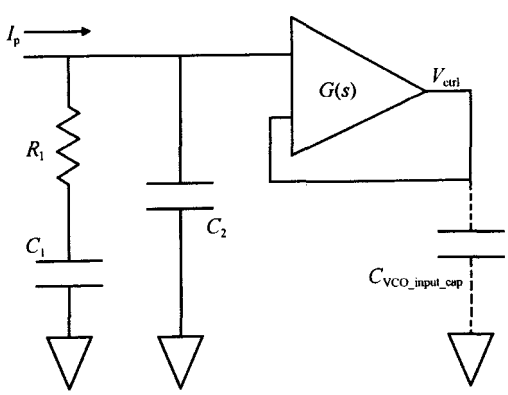



Fig. 3 Topology of a equivalent third order loop filter

where $\omega_z$ is the loop bandwidth of the synthesizer, $\omega_z = 1/R_1 C_1$, and $\omega_p = (C_1 + C_2)/R_1 C_1 C_2$.

## 3 Frequency synthesizer simulation strategy

It is very hard to simulate a frequency synthesizer in full-transistor-level, because the large frequency division ratio makes simulation efficiency very low with a time domain based simulator, such as spectreRF. In this paper another solution is used to predict the phase noise of the frequency synthesizer. A linear phase domain model of the synthesizer is established with the help of Matlab. A similar simulation method is introduced in Ref. [4]. Figure 4 gives the improved linear phase domain model used in this design. Each block's noise can be considered as an additive Gaussian noise source. To simplify the simulation, PFD, charge pump, and loop filter are combined into one block labeled as PFDB, while VCO block consists of the unit gain transconductance amplifier and the QVCO. Each block's noise data are obtained from spectreRF PNoise simulation. The simulated phase noise of the synthesizer is shown in Fig. 5. When doing the phase noise simulation, the output of the synthesizer is tuned to 2.4GHz. An ideal double balance mixer is added after the synthesizer for I/Q mismatch simulation. The simulation results are listed in Table 2 and Table 3.

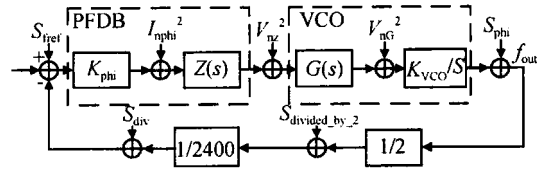



Fig. 4　Linear phase domain model for the frequency synthesizer simulation

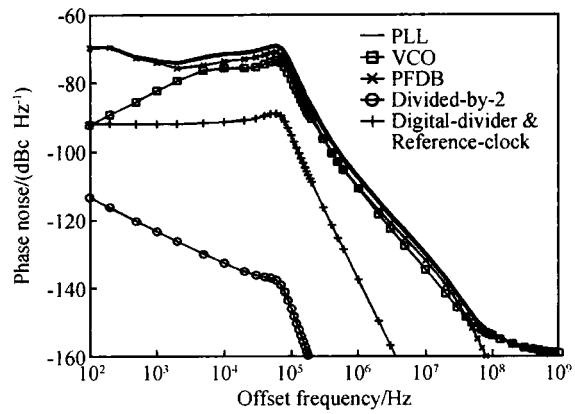



Fig. 5　Simulation results of the synthesizer's phase noise with a linear phase domain model

Table 2　Simulated spot phase noise of a frequency synthesizer at 1MHz offset from carrier

| Module name | Noise of each module | Phase noise at output | Contribution |
|---|---|---|---|
| VCO($S_{phi}$) | -110.85dBc/Hz | -110.85dBc/Hz | 47.75% |
| PFDB($V_{nz}^2$) | $6.56\times10^{-17}V^2$/Hz | -110.475dBc/Hz | 52.06% |
| Divided-by-2($S_{divided\text{-}by\text{-}2}$) | -155.137dBc/Hz | -194.587dBc/Hz | 0.0% |
| Digital divider($S_{div}$) | -168.623dBc/Hz | -137.469dBc/Hz | 0.1% |
| Total | NA | -107.64dBc/Hz | NA |

Table 3　Simulation and measurement results of frequency synthesizer

| | Specification | Simulation | Measurement |
|---|---|---|---|
| Close-in phase noise | NA | < -70dBc/Hz | < -70dBc/Hz |
| Spot phase noise @1MHz | < -80dBc/Hz | -107.64dBc/Hz | -106.15dBc/Hz |
| Spot phase noise @2MHz | < -110dBc/Hz | -114.65dBc/Hz | < -106dBc/Hz * |
| Spot phase noise @3MHz | < -120dBc/Hz | -119dBc/Hz | < -110dBc/Hz * |
| Settling time | <200μs @80MHz | 108μs @80MHz | <120μs @80MHz |
| Locked range of PLL | 2.4～2.48GHz | NA | 2.1～2.45GHz |
| VCO tuning range | NA | 2.1～2.72GHz | 1.98～2.52GHz |
| Phase mismatch(I/Q) | NA | <1° | NA |
| Gain mismatch(I/Q) | NA | <0.15dB | NA |

* The measurement results are deteriorated by the large interference signal located around 2.5MHz

## 4 Measurement results

The frequency synthesizer is implemented in a chartered 0.35μm 2P4M mixed-signal process. The microphotograph of the synthesizer is shown in Fig. 6. The core size is 1.3mm ×0.8mm. The whole synthesizer and VCO buffer consume 13.5mA and 8mA, respectively.

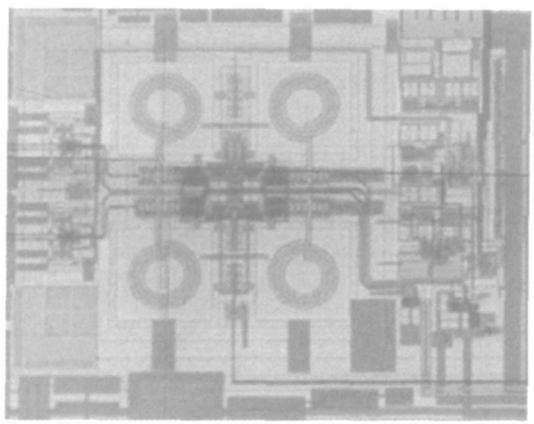


Fig. 6 Microphotograph of the frequency synthesizer

The tuning characteristic of the VCO is measured in a locked PLL loop. The measured VCO gain is 454MHz/V. With the help of a capacitor array, the VCO can cover the band from 1.98GHz to 2.52GHz. But only the linear region (from 2.24 to 2.45GHz in Fig. 7) of the VCO can be used for the synthesizer, which is slightly lower than the bluetooth requirement.

A spectrum analyzer is used to measure the frequency synthesizer. A large spur at 2.5MHz offset from the carrier appears in the output spectrum of the synthesizer. The reason is that a 2.5MHz digital signal led from the synthesizer for test purpose coupling to the control line of VCO through PCB or supply/ground ring of PADs. The measured phase noise of the frequency synthesizer is shown in Fig. 8(a). The low frequency (< 50kHz) phase noise is suppressed about 25dB by the loop, compared to the open-loop phase noise (shown in Fig. 8(b)). The close-in phase noise is about -70dBc/Hz, which matches the simulation results very well. The spot phase noise is -106.15dBc/Hz

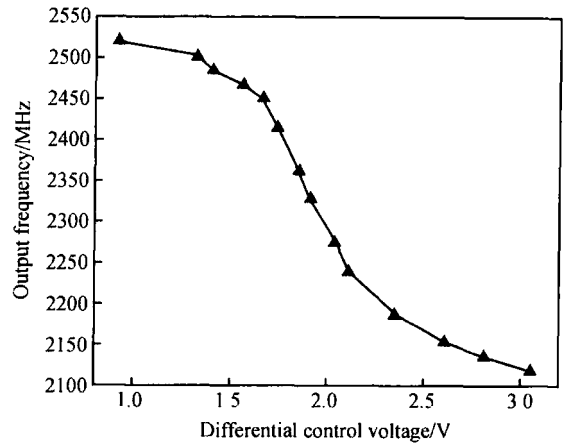
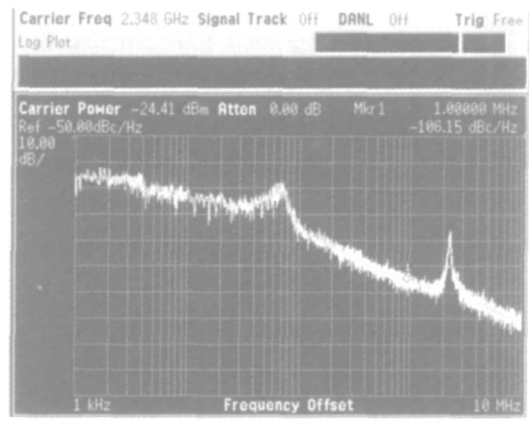
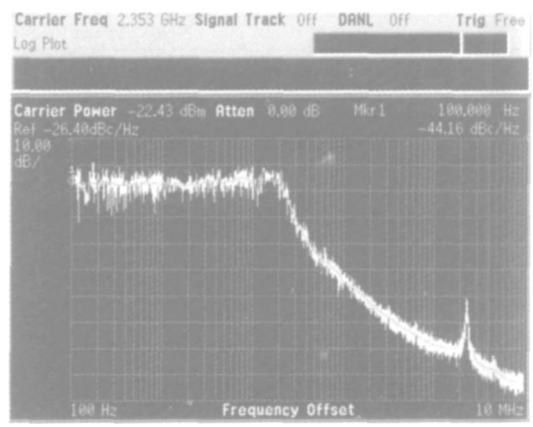



Fig. 7 Tuning characteristic of the VCO when DCCA is biased at its maximum value




(a)




(b)

Fig. 8 (a) Measured closed-loop phase noise of the synthesizer (carrier frequency is 2.348GHz); (b) Measured open-loop phase noise of the synthesizer (carrier frequency is 2.353GHz)

at 1MHz for a carrier frequency of 2.348GHz, which is 1.5dB higher than the simulated value. No significant spur appears at the output spectrum of the synthesizer except the one located at 2.5MHz. Because of the measurement environment limitation, I/Q mismatch is not measured. The measurement results are also listed in Table 3.

## 5 Conclusion

A 2.4GHz integer-*N* frequency synthesizer with quadrature output for bluetooth has been presented. For the purpose of omitting part of the capacitor used in a third order loop filter, a unit gain transconductance amplifier is used with the help of the VCO's input capacitance. An improved linear phase domain model is established here to predict the phase noise performance of the frequency synthesizer, which has been proved to have very good agreement between simulated value and measured value. Some improvements are necessary to fulfill the requirement of bluetooth. A large spur occurs at the output spectrum of the synthesizer, although differential tuning technique is used, which probably is caused by a large VCO gain. This indicates that a smaller VCO gain should be adopted in the further work. The center frequency of the VCO is lower than the desired value because of an insufficient prediction on parasitic capacitance, however this can easily be corrected.

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# 一种 2.4GHz 正交输出频率综合器

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**摘要**: 介绍了一种用于 bluetooth 的基于 0.35μm CMOS 工艺的 2.4GHz 正交输出频率综合器的设计和实现. 采用差分控制正交耦合压控振荡器实现 I/Q 信号的产生. 为了降低应用成本, 利用一个二阶环路滤波器以及一个单位增益跨导放大器来代替三阶环路滤波器. 频率综合器的相位噪声为 -106.15dBc/Hz @1MHz, 带内相位噪声小于 -70dBc/Hz, 3.3V 电源下频率综合器的功耗为 13.5mA, 芯片面积为 1.3mm ×0.8mm.

**关键词**: 频率综合器; 锁相环; 正交压控振荡器; 相位噪声; 蓝牙

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