Design of an OP-AMP Based on a LDO Regulator *

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Abstract: An operational amplifier (OP-AMP) with a ground current of about 0.6μA is presented. Moreover, this amplifier reaps the benefits of incorporating a foldback current limiting circuit, which enables the low-dropout voltage regulator without the need of a special current limiting subblock. Therefore, the object of ultra-low power is realized because of a great reduction in transistors and current limbs.

Key words: operational amplifier; ground current; LDO; foldback current limiter
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1 Introduction

The explosive proliferation of battery-powered equipment in the past decade has accelerated the development of low-power-consumption low-dropout (LDO) voltage regulators. This has intensified the focus of designers on optimizing the performance of the amplifiers[1]. When the load-current is low, which is the normal operating mode for many applications, the ground current becomes an intrinsic factor in determining the lifetime of the battery[2,3].

In this paper, the amplifier incorporating foldback current limiter, whose ground current is only 0.6μA to ensure the LDO regulator to operate at a ground current as low as 2.4μA throughout its load range has a very small number of current paths.

2 Circuit design

2.1 Main structure of the LDO

A low-dropout regulator is a circuit that provides a well specified and stable voltage. The input to output voltage difference of this circuit is low. The main structure of the LDO chip and its typical application circuit we designed is shown in Figs. 1 and 2 respectively. The regulator is basically composed of a pMOS pass transistor, an amplifier with a foldback current limiter, a set of resistive feedback networks Rf1 and Rf2, a load resistor R_L, a voltage reference V_{ref} based on Brokaw cell[4] whose function is to take a scaled-down version of the output and then provide differential signals VR1 and VR2 to the amplifier[5], therefore the amplifier adjusts V_{OUT} via the pMOS pass transistor to a re-

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quired value. C_L is a filtering capacitor with equivalent series resistance R_{ESR}. The value of ESR determines the output performance during the load transient. The smaller the ESR value, the better the performance, with less overshoots and undershoots during the load transient. The LDO features a p-channel MOSFET pass transistor. This provides advantages over similar designs using a pnp pass transistor - on advantage being longer battery life. The p-channel MOSFET requires no base drive, which reduces ground currents considerably.

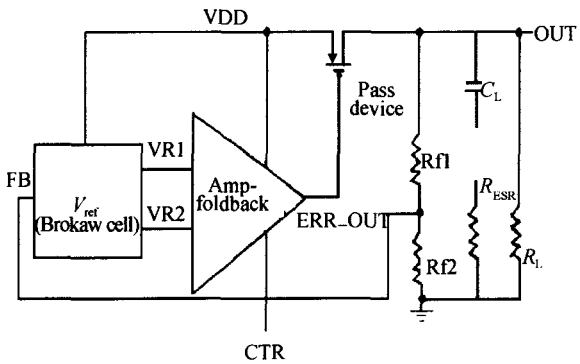

Fig. 1 Main structure of LDO

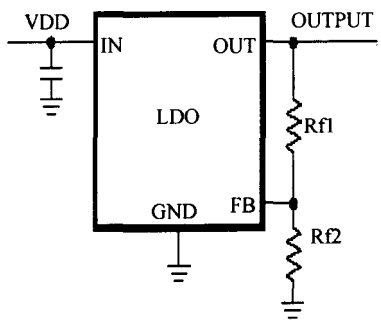

Fig. 2 Typical application circuit

2.2 OP-AMP circuit design

The amplifier we designed incorporates a foldback current limiter - this subblock is abbreviated to amp-foldback (Fig. 3).

As shown in Fig. 3, VR1 and VR2 are the noninverting and inverting inputs of the amplifier respectively. ERR_OUT is the output of the amplifier which controls the gate of pMOS pass device of the LDO. VDD is the power supply. OUT, which controls the gate of MN2, is the output pin of the LDO chip. CTR controls the gates of MN1, MN3, and MN4, offering biasing voltage to the amplifier. VR1 and VR2 are the inputs of the first stage with node A as the output, meanwhile, node A is the input of the second stage with ERR_OUT as the output of the second stage.

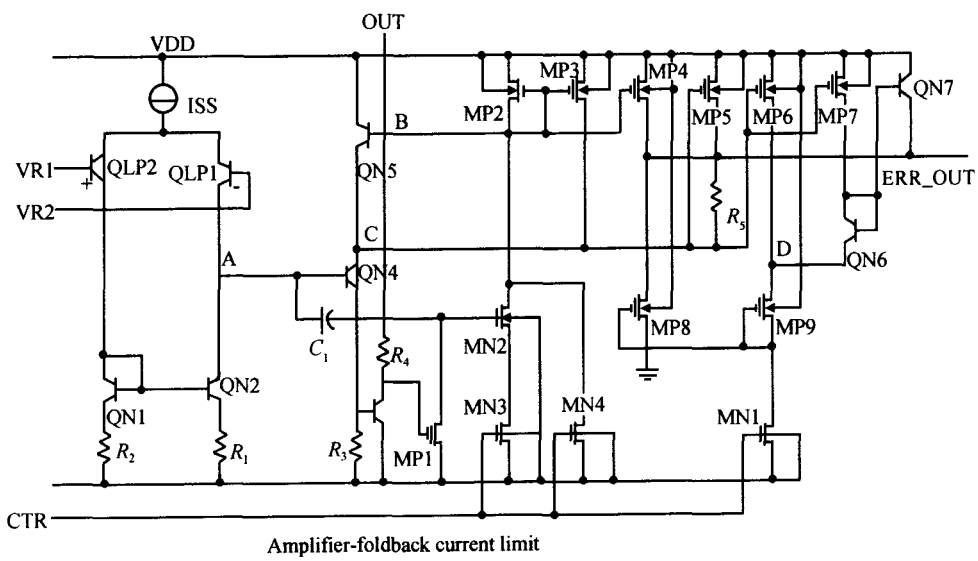

Fig. 3 Amp-foldback subblock schematic

The W/L ratios of MP6 and MP7 are designed equal, since their gate-source voltages are equal, their drain currents will be the same. That is $I_{MP6} = I_{MP7}$, Since $V_{DS\_MP9} = V_{GS\_MP9}$, MP9 will be in saturation and is given by

$$I_{MP9} = I_{MN1} = I_{MP6} + I_{MP7} \quad (1)$$

Thus, I_{MP6} is given by

$$I_{MP6} = \frac{1}{2} I_{MN1} = \frac{1}{4} \mu_0 C_{ox} \frac{W_{MN1}}{L_{MN1}} (V_{CTR} - V_{ThN})^2 \quad (2)$$

Equation (2) indicates that I_{MP6} is fixed, so V_{GS_MP6} keeps constant, which gives rise to a very nearly constant node voltage V_C.

From the above analyses, operational principles of the amplifier can be concluded as follows: if the variation of differential inputs VR1, VR2 causes variation of node voltage V_A then a slight variation of V_C will lead to massive variation of V_{ERR_OUT}, which is the output of the amplifier.

QN5 has been added to balance current. This can be explained as follows: since $V_{DS\_MP2} = V_{GS\_MP2}$, MP2 will be in saturation causing V_{GS_MP2} to be fixed, then voltage on node B V_B maintains constant. When the LDO regulator is in normality and V_{OUT} is large enough to turn MN2 on, I_{MP2} is given by

$$I_{MP2} = I_{MN3} + I_{MN4} \quad (3)$$

Since the W/L ratios of MN3 and MN4 are designed equal, both are one fourth of that of MN1, moreover, $V_{GS\_MN1} = V_{GS\_MN3} = V_{GS\_MN4}$, then

$$I_{MN1} = 2(I_{MN4} + I_{MN3}) \quad (4)$$

From Eqs. (2), (3), and (4), we get

$$I_{MP6} = I_{MP2} \quad (5)$$

Since the W/L ratio of MP6 is designed larger than that of MP2, it can be deduced that $V_C > V_B$, transistor QN5 now being turned off. For node C applying KCL (the base current of QN5 is neglected)

$$I_{E\_QN4} = I_{C\_QN4} = I_{QN5} + I_{MP3} + I_{R5} \quad (6)$$

An increase in the voltage of non-inverting terminal VR1 will increase I_{E_QN4} owing to higher base-emitter voltage of QN4. From above analyses, $I_{QN5} = 0$, MP2 and MP3 are connected as a current mirror, thus I_{MP3} is fixed. For Eq. (6), an increase of I_{R5} is a must. Then V_{ERR_OUT} and V_D will increase (Since $V_{ERR\_OUT} + V_{BE\_QN7} = V_D + V_{BE\_QN6}$, it can be deduced that $V_D \approx V_{ERR\_OUT}$) turning off QN6, QN7 at some point, I_{MP6} will be twice and V_C will decrease instantaneously, and this drop in V_C continues as long as $I_{E\_QN4} > I_{MP3} + I_{R5}$. As a result, QN5 will be turned on, thus Equation (6) is satisfied, which is to say, the current equilibrium point is established.

MN2 and $R5$ are the kernels of the foldback current limiter. The maximum value of the output current is limited by $R5$, and MN2 restricts the short-circuit current to a range that is $\leq$50mA when the OUT terminal of the LDO chip is connected to ground.

When the output current is large enough and results in $V_{ERR\_OUT} < V_C$, then

$$I_{R5} = I_{MP3} - I_{QN4} \leq I_{MP3} - I_{QN4\_min} \quad (7)$$

$$I_{R5\_max} = I_{MP3} - I_{QN4\_min} \quad (8)$$

$$V_{ERR\_OUT} = V_C - I_{R_5} R_5 \geq V_C - (I_{MP3} - I_{QN4\_min}) R_5 \quad (9)$$

$$V_{ERR\_OUT\_min} = V_C - (I_{MP3} - I_{QN4\_min}) R_5 \quad (10)$$

When the LDO is under normal operating conditions, V_{OUT} is large enough to turn MN2 on, MP2 and MP3 are connected as a current mirror and the width-to-length ratios of them are designed 1 ∶2, thus $I_{MP3} = 2I_{MP2} = 2(I_{MN3} + I_{MN4})$. When Equation (10) is satisfied, gate voltage of pMOS pass element of the LDO (V_{ERR_OUT}) reaches its minimum value, leading to the maximum output current. At this time, if R_{LOAD} further continues to decrease, V_{OUT} will continually drop, turning MN2 off at some point, thus I_{MP3} is reduced by half, which is to say, $I_{MP3} = 2I_{MN4}$. From Eq. (10), $V_{ERR\_OUT\_min}$ increases, leading to a decrease in maximum output current. Finally, the maximum value of the output current is limited to a range that is $\leq$50mA when the OUT terminal of the LDO chip is connected to ground.

3 Simulated results

Figure 4(a) is the layout of the LDO including proposed operational amplifier. The AMP-Foldback circuit in Fig. 3 is simulated at $V_{DD} = V_{OUT} + 1$.

Meanwhile the LDO regulator with this kind of amplifier is tested. The gain result is shown in Fig. 4(b), which is only 60dB but already meets the required transient response, stability, and load regulation characteristics of the LDO wholechip. The phase margin of the amplifier is about 45. Figure 4(c) shows the simulation result of the foldback current limiter. The steady output of the LDO under normal operating conditions is 1.8V, when the load current decreases to the point where MN2 will be turned off, restricting the short-circuit current to 43mA. When OUT is shorted to ground, the short-circuit current is 42.81mA (Fig. 4(d)). As shown in Figs. 4(e) and (f), at a 20mA load current, the ground currents consumed by the amplifier and by the LDO regulator are 0.57 and 2.21μA respectively. Obviously, high current efficiency is achieved especially at a low output current.

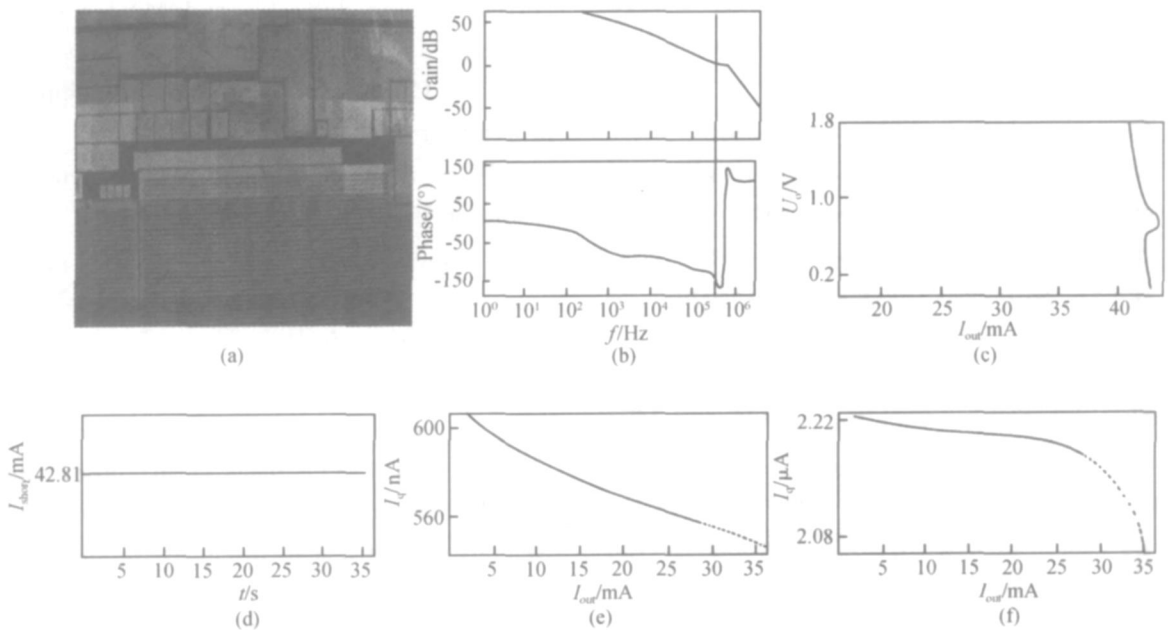

Fig. 4 (a) Layout of the LDO including proposed operational amplifier; (b) Gain and phase of the amplifier; (c) Simulation result of the foldback current limit; (d) Simulation result of the short-circuit current; (e) Ground current of the amplifier subblock versus load current; (f) Ground current of the LDO wholechip versus load current

4 Conclusion

In this paper, we combine an amplifier and a foldback current limiter into a single circuit with a minimum number of current limbs making it a candidate for an ultra-low power LDO.

References

[1] Yin T, Zhu Z M, Yang Y T, et al. Analysis of bulk-driven MOSFET and design of ultra-low voltage operational amplifier. Chinese Journal of Semiconductors, 2005, 26(1): 158 (in Chinese) [尹韬, 朱樟明, 杨银堂, 等. 衬底驱动 MOSFET 特性分析及超低压运算放大器设计. 半导体学报, 2005, 26(1): 158]

[2] Lau S K, Leung K N, Mok P K T. Analysis of low-dropout regulator topologies for low-voltage regulation. IEEE International Conference on Electron Devices and Solid-State Circuits, 2003: 379

[3] Rincon-Mora A, Allen P E. A low-voltage, low quiescent current, low drop-out regulator. IEEE J Solid-State Circuits, 1998, SC-33(1): 36

[4] Hastings R A. Brokaw transconductance operational transconductance amplifier-based micropower low drop out voltage regulator having counterphase compensation. US Patent Application, No. 09/470910, filed December 23, 1999

[5] Brokaw A P. Stable low dropout voltage regulator controller. US Patent Application. No. 647241, filed May 9, 1996

一种基于 LDO 线性稳压器的放大器设计 *

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摘要: 设计了一种地电流约为 0. 6μA 的基于低压差线形稳压器的放大器电路. 此放大器的突出优点是与 foldback 限流保护电路融合在一起,使得芯片不需要专门的限流模块,大大减少了电流支路,实现超低功耗.

关键词: 运算放大器; 地电流; LDO; foldback 过流保护

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