A Linear CMOS OTA and Its Application to a 3.3V 20MHz High-Q g_m-C Bandpass Filter *

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Abstract: A design of a linear and fully-balanced operational transconductance amplifier (OTA) with improved high DC gain and wide bandwidth is presented. Derivative from a single common-source field effect transistor (FET) cascade and its DC *I-V* characteristics, the third-order coefficient g_3 has been well compensated with a parallel FET operated in the triode region, which has even-odd symmetries between the boundary of the saturation and triode region. Therefore, for high linearity, a simple solution is obtained to increase input signal amplitude in saturation for the application of OTA continuous-time filters. A negative resistance load (NRL) technique is used for the compensation of parasitic output resistance and an achievement of a high DC-gain of the OTA circuits without extra internal nodes. Additionally, derivations from the ideal -90° phase of the g_m-*C* integrator mainly due to a finite DC gain and parasitic poles will be avoided in the frequency range of interest. HSPICE simulation shows that the total harmonic distortion at $1V_{p\text{-}p}$ is less than 1% from a single 3.3V supply. As an application of the VHF CMOS OTA, a second-order OTA-C bandpass filter is fabricated using a 0.18μm CMOS process with two kinds of gate-oxide layers, which has achieved a center frequency of 20MHz, a 3dB-bandwidth of 180kHz, and a quality factor of 110.

Key words: linear OTA; high DC-gain; high *Q*; bandpass filter
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1 Introduction

In recent years, development of sophisticated analog and digital circuits fabricated on a single chip has resulted in the implementation of a single-chip mixed analog/digital system. Active filters have been implemented with various degrees of integration. Many design techniques have been proposed for realizing monolithic continuous-time filters. For high-frequency application, the transconductance-capacitor (g_m-*C*) approach is well-known where the basic block is a continuous-time integrator. Excess phase shifts in the integrator will have great influence on the frequency response of high-frequency filters. A linearized operational transconductance amplifier (OTA) cell is designed and optimized for integrator phase error cancellation[1~5].

In order to achieve high output resistance and to increase the voltage gain of the OTA, a negative conductance is used to cancel its positive output conductance, which can also compensate for the loss introduced by the finite output impedance of the OTA implemented in the continuous-time filter, thus the quality factor (*Q*) is increased. Negative resistance load (NRL) realized high-gain OTA

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with large gain-bandwidth-products (GBW) and avoided excess phase shifts from ideal - 90° phase of the integrator[6~8]. Compared with other commonly used gain enhancement techniques, NRL has fewer poles and consumes less power. In this paper, a simple OTA has been proposed with enhanced DC gain and improved linearity.

2 High-gain OTA with NRL

The design of analog signal processing systems is increasingly based on OTAs because of their fast speed in comparison with conventional low output impedance operational amplifiers (OpAmp), and their bias dependence transconductance tenability. However, the range of linear operation of OTAs has been restricted seriously, and has been investigated in the literature for several decades[9,10]. In this paper we combine a novel technique proposed in Refs. [11,12] to linearize the input differential pair with NRL to reduce non-zero integrator phase shift due to the internal low impedance and parasitic capacitance of the OTA. Figure 1 shows the proposed OTA which consists of a negative resistance load (M5, M6, M7, M8) and a differential transconductance cell (M1, M2, M3, M4, M33, M44) that is firstly proposed by Youn *et al*.[12] to improve the linearity of low noise amplifiers. The nonlinearity of a circuit mainly comes from the nonlinearity of MOSFETs which can be characterized by Taylor expansion in the range of interest:

$$y(t) = g_1 x(t) + g_2 x^2(t) + g_3 x^3(t) + \cdots \quad (1)$$

where $x(t)$ and $y(t)$ are the input voltage V_{gs} and channel current I_{ds} of MOSFETs, respectively. For small x, $y(t) \approx g_1 x$, indicating that g_1 can be the small signal gain. g_2, g_3 are the successive derivatives of DC *I-V* characteristics. The third-order coefficient g_3 is the major source of the harmonic distortion of differential OTAs because the differential structure cancels out all the even order harmonics. M33 and M44 play the roles of eliminating g_3.

Figure 2 shows the output drain-source current and its 3rd-order coefficient g_3 of the simple cascade circuit. The MOSFET *I-V* curve (Fig. 2) shows asymmetry in the saturation and triode region of the 3rd-order derivative. According to this characteristic of the cascade circuit, we can add a MOSFET working in the triode region to cancel out the nonlinearity of the original MOSFET. For realization, a branch circuit (M3 and M33) parallel with MOSFET M1 is used to compensate the nonlinearity of the original cascade circuit, where M33 is operated in the saturation region and M3 is operated in the triode region when the amplitude of the input signal is small. M2, M44, and M4 are matched to M1, M33, and M3, respectively.

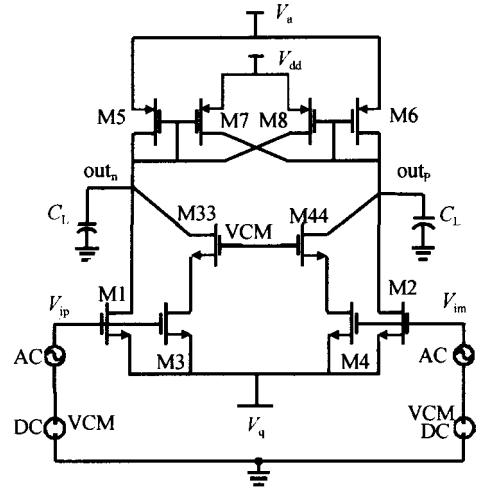

Fig. 1　Proposed OTA with NRL

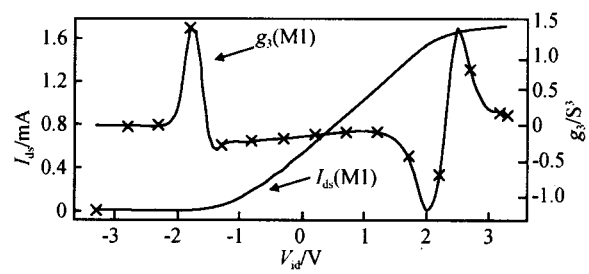

Fig. 2　M1 *I-V* DC curve and its 3rd-order derivative

Figure 3 shows the three-order derivative of M1 and M3 respectively, where M1 firstly comes into the saturation region and then M3 follows M1 into the saturation region. However, when the input signal is large, M3 enters the triode region and

M1 is still in the saturation region. At the vicinity of the common mode input voltage (CMIV), the 3rd-order derivatives of M1 and M3 can cancel out each other, therefore the linearity of the OTA has been improved with a decreased 3rd-order derivative. Figure 4 shows the transconductance (g_m) simulation result of the linearized OTA with NRL. As V_q varies from 0 to 0.3V, g_m adjustment in range from 30.8 to 22.2μs is obtained for single power supply of 3.3V.

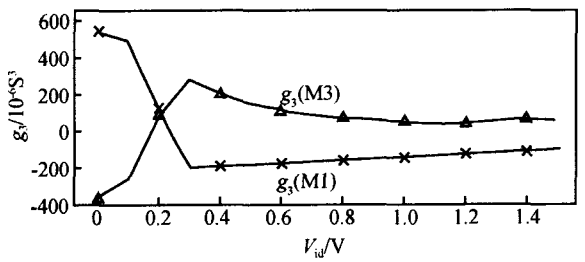

Fig. 3 3rd-order derivatives of M1 and M3

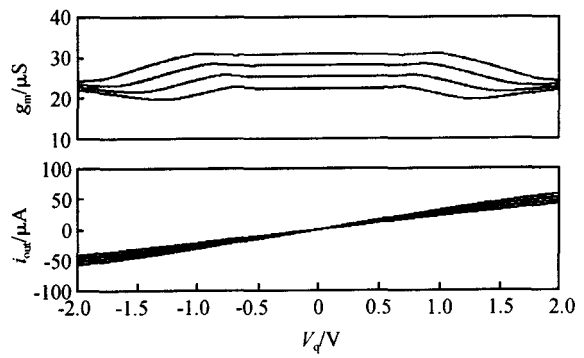

Fig. 4 OTA output currents and g_m at different V_q

An ideal transconductance amplifier is an infinite bandwidth voltage controlled current source with an infinite input and output impedance. However, the output impedance of a real g_m cell is always finite and the real g_m cell is then a two-pole system and the dominant pole is no longer at zero. Meanwhile, a non-zero integrator phase shift caused by internal low impedance and parasitic capacitance will make the actual frequency response deviate from the ideal case, especially for high-Q system which will become unstable in the extreme case if the excess phase shift is not reduced. Recently, a number of researchers have investigated techniques based on the negative resistance load[13,14]. We can represent the building block circuit of Fig. 1 with its small-signal macro-model including parasitic output resistance R_p in parallel with a negative resistance R_n, which is shown in Fig. 5. From the macro-model, we can obtain the transfer function of the OTA,

$$A(s) = \frac{V_{out}}{V_{in}} = -\frac{g_m}{\frac{1}{R_p} + \frac{1}{R_n} + s(C_l + C_p)} \quad (2)$$

where C_l, C_p are the load capacitor and parasitic capacitor, respectively, R_n, R_p will be described in the following description.

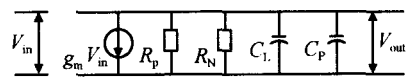

Fig. 5 Small signal equivalent circuit of Fig. 1

Using the standard square-law model of MOS devices in the NRL subcircuit of Fig. 1, the differential output current can be described as

$$i_{out} = I_{outn} - I_{outp} = -2k_p(V_{dd} - V_a)(V_{outp} - V_{outn}) \quad (3)$$

where $k_p = 0.5\mu_p C_{ox} W/L$ is the OTA parameter.

Then the output equivalent transconductance is

$$g_{mn} = \frac{\partial i_{out}}{\partial V_{out}} = -2k_p(V_{dd} - V_a) \quad (4)$$

Thus, the negative resistance R_N can be written as

$$R_N = 1/g_{mn} = -1/2k_p(V_{dd} - V_a) = -\frac{1}{g_{m8} - g_{m5}} \quad (5)$$

where g_{m8}, g_{m5} are the tranconductances of M8 and M5, respectively. If at the output terminal the sum of output resistances is close to the negative resistance, theoretically infinite output resistance and voltage gain will be obtained. From the circuit of Fig. 1, output transconductance approaches the sum of M1, M33, M5, and M8, when all of the four MOSFETs work in the saturation region where M3 works in the triode region. Thus the output conductance of the OTA can be approximated as,

$$R_p = 1/g_{ds} = \frac{1}{g_{ds1} + g_{ds33} + g_{ds5} + g_{ds8}} \quad (6)$$

From Eq. (2) ,we can obtain infinite DC gain of the OTA under the condition $R_p = -R_n$. However ,if $R_p < R_n$,the system will be unstable due to a right-half-plane pole , known as " overcompensated ". From Eqs. (4) and (5) ,the unstable state can be avoided if and only if the following inequation holds.

$$V_a \geq V_{dd} - \frac{1}{2k_p R_p} \quad (7)$$

Figure 6 shows the AC response of the proposed OTA circuit with sweeping V_a voltage from 3. 25 to 3. 3V. For simplicity , gain and phase slope curves versus different V_a voltages are shown in Fig. 7. According to Eqs. (4) and (7) ,the negative transconductance has a direct proportion nexus with the difference between supply voltage V_{dd} and V_a ; the result plot shown in Fig. 7 is a bilateral symmetry curve at $V_a = 3.28$V. When $V_a > 3.28$V ,the system will remain stable due to the negative phase slope[15]. HSPICE simulation shows the output resistance is 171MΩ and gain is 83dB at CMIV = 1. 65V and $V_a = 3.28$V.

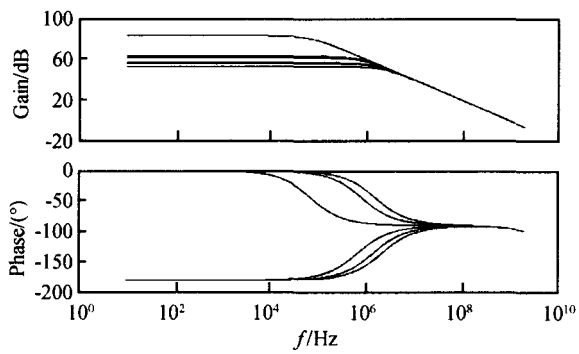

Fig. 6　OTA output gain and phase with NRL

The simulated total harmonic distortion (THD) for the proposed circuit of Fig. 1 is depicted in Fig. 8. HSPICE simulation shows that the THD is less than 1 % when the input voltage ranges within $1V_{p\text{-}p}$ and CMIV ranges from 1. 65V to 2. 65V. The marker diamond ,real line ,dashed line , and marker plus sign represent THD curves at CMIV of 1. 65 ,2 ,2. 35 ,and 2. 65 ,respectively.

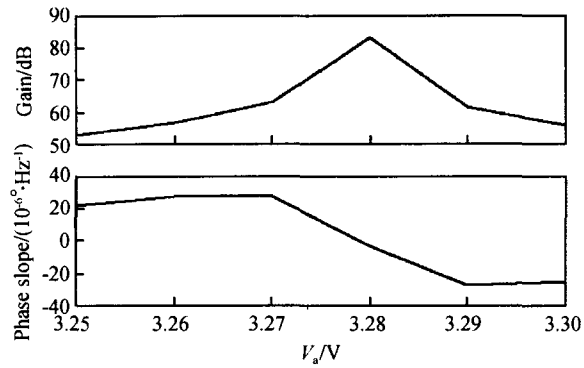

Fig. 7　OTA output gain and phase slope versus different V_a

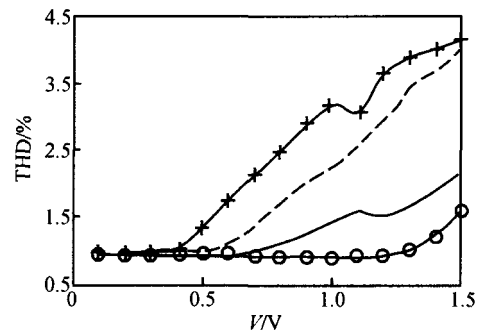

Fig. 8　OTA total harmonic distortion for different VCM

3　High-Q bandpass filter design

Figure 9 shows the structure of a single biquad bandpass filter while OTA g_{m2} and g_{m3} implement an active gyrator and g_{m1} , C_1 and C_2 form an integrator[16]. The equivalent inductance L_{eq} of gyrator is given by

$$L_{eq} = \frac{C_2}{g_{m2}\, g_{m3}} \quad (8)$$

and the center frequency ω_0 is given by

$$\omega_0 = \frac{1}{\sqrt{LC}} = \sqrt{\frac{g_{m2}\, g_{m3}}{C_1\, C_2}} \quad (9)$$

An approach to compensate the finite output impedance of OTA is to parallel a negative g_m cell with the g_m cell. The resulted output impedance is

$$R_0 = \frac{1}{g_{0i} - g_{m-}} \quad (10)$$

where g_{0i} is the output impedance of the i-th OTA, g_{m-} is the output impedance of the negative g_m cell itself. For high Q application, the transfer function can be approximated as

$$H(s) = \frac{V_{bp}}{V_{in}} = \frac{sg_{m1}C_1}{s^2 + s/C_1R_0 + g_{m2}g_{m3}/C_1C_2} \quad (11)$$

Q value is

$$Q = \frac{\omega_0}{BW} = \omega_0 C_1 R_0 = g_{m2,3} R_0 \quad (12)$$

Figure 10 shows the HSPICE simulated amplitude-frequency and phase-frequency response of the bandpass filter implemented by the proposed linear OTA with NRL. The simulation was performed at 20MHz center frequency and quality factor was 110 where C_1, C_2 are equal to 0.29pF.

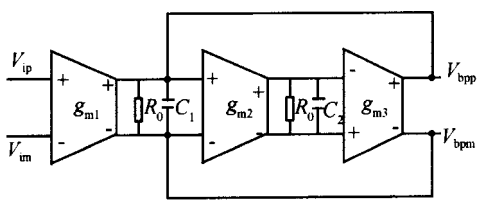

Fig. 9 Biquad bandpass filter

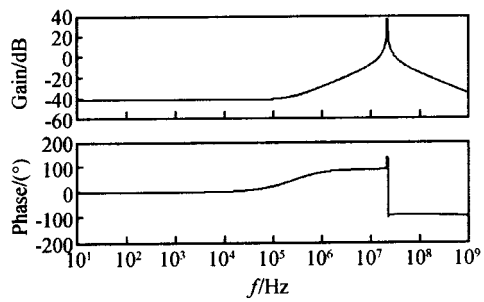

Fig. 10 Biquad bandpass implementing negative resistance load OTA

4 Conclusion

This paper has presented the design and implementation of the high-gain linear OTA which can operate at a very high frequency and low power supply voltage. The resulting bandpass filter exhibits a high-Q, large voltage gain, and good linearity at the several tens MHz region.

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应用于高 Q 跨导-电容带通滤波器的线性跨导运放设计

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摘要：设计了一种具有高的直流增益的宽带线性全差分跨导运放.一方面,并联一个工作在线性区的场效应管来补偿直流三阶系数,得到了一种应用于连续时间滤波器、增加跨导器饱和区输入信号幅度的简单方法.另一方面,结合负电阻电路提高了输出阻抗,实现高的直流增益而不需要额外的内部结点,并减小了因有限直流增益和寄生电容引起的相位偏差.将此全差分跨导运放应用于 0.18μm CMOS 工艺二阶带通滤波器,在 3.3V 电源电压、输入峰峰值 1V 时,HSPICE 仿真结果的总谐波失真小于 40dB,中心频率为 20MHz,3dB 带宽为 0.18MHz,即 *Q* 为 110.

关键词：线性跨导运放；高直流增益；高品质因数；带通滤波器

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